Infineon Technologies - MB90F352SPFM-GS-117E1 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 15x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-QFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f352spfm-gs-117e1

■ PRODUCT LINEUP 2

Parameter \ Part Number	MB90351A, MB90352A	MB90351TA, MB90352TA	MB90351AS, MB90352AS	MB90351TAS, MB90352TAS	MB90V340A-101	MB90V340A-102
CPU	F^2MC-16LX CPU					
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)					
ROM	MASK ROM 64Kbytes : MB90351A(S), MB90351TA(S) 128Kbytes : MB90352A(S), MB90352TA(S)				External	
RAM	4 Kbytes				30 Kbytes	
Emulator-specific power supply*	—				Yes	
Sub clock pin (X0A, X1A) (Max 100 kHz)	Yes		No		No	Yes
Clock monitor function	No					
Low voltage/CPU operation detection reset	No	Yes	No	Yes	No	
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter 4.5 V to 5.5 V : at using external bus				5 V ± 10%	
Operating temperature range	−40 °C to +125 °C				—	
Package	LQFP-64				PGA-299	
UART	2 channels				5 channels	
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device					
I^2C (400 Kbps)	1 channel				2 channels	
A/D Converter	15 channels				24 channels	
	10-bit or 8-bit resolution Conversion time : Min 3 µs includes sample time (per one channel)					
16-bit Reload Timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.					
16-bit I/O Timer (2 channels)	I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1. I/O Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.				I/O Timer 0 corresponds to ICU 0/1/2/3, OCU 0/1/2/3. I/O Timer 1 corresponds to ICU 4/5/6/7, OCU 4/5/6/7.	
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)					

(Continued)

■ PRODUCT LINEUP 4

Part Number / Parameter	MB90356A, MB90357A	MB90356TA, MB90357TA	MB90356AS, MB90357AS	MB90356TAS, MB90357TAS	MB90V340A-103	MB90V340A-104
CPU	F²MC-16LX CPU					
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)					
ROM	MASK ROM 64Kbytes : MB90356A(S), MB90356TA(S) 128Kbytes : MB90357A(S), MB90357TA(S)				External	
RAM	4 Kbytes				30 Kbytes	
Emulator-specific power supply*	—				Yes	
Sub clock pin (X0A, X1A)	Yes		No (internal CR oscillation can be used as sub clock)		No (internal CR oscillation can be used as sub clock)	Yes
Clock monitor function	Yes					
Low voltage/CPU operation detection reset	No	Yes	No	Yes	No	
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter 4.5 V to 5.5 V : at using external bus				5 V ± 10%	
Operating temperature range	−40 °C to +125 °C				—	
Package	LQFP-64				PGA-299	
UART	2 channels				5 channels	
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device					
I²C (400 Kbps)	1 channel				2 channels	
A/D Converter	15 channels				24 channels	
	10-bit or 8-bit resolution Conversion time : Min 3 µs includes sample time (per one channel)					
16-bit Reload Timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.					
16-bit I/O Timer (2 channels)	I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1. I/O Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.				I/O Timer 0 corresponds to ICU 0/1/2/3, OCU 0/1/2/3. I/O Timer 1 corresponds to ICU 4/5/6/7, OCU 4/5/6/7.	
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)					

(Continued)

Pin No. LQFP64*	Pin name	Circuit type	Function
39	P17	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD15		Input/output pin for external bus address data bus bit 15. This function is enabled when external bus is enabled.
40 to 43	P20 to P23	G	General purpose I/O ports. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pins are enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
	A16 to A19		Output pins for A16 to A19 of the external address data bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins A16 to A19.
	PPG9 (8) , PPGB (A) , PPGD (C) , PPGF (E)		Output pins for PPGs
44	P24	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
	A20		Output pin for A20 of the external address data bus. When the corresponding bit in the external address output control register (HACR) is 0, the pin is enabled as high address output pin A20.
	IN0		Data sample input pin for input capture ICU0
51	P25	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
	A21		Output pin for A21 of the external address data bus. When the corresponding bit in the external address output control register (HACR) is 0, the pin is enabled as high address output pin A21.
	IN1		Data sample input pin for input capture ICU1
	ADTG		Trigger input pin for A/D converter
52	P44	H	General purpose I/O port
	SDA0		Serial data I/O pin for I^2C 0
	FRCK0		Input pin for the 16-bit I/O Timer 0
53	P45	H	General purpose I/O port
	SCL0		Serial clock I/O pin for I^2C 0
	FRCK1		Input pin for the 16-bit I/O Timer 1

(Continued)

Pin No. LQFP64*	Pin name	Circuit type	Function
54	P30	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	ALE		Address latch enable output pin. This function is enabled when external bus is enabled.
	IN4		Data sample input pin for input capture ICU4
55	P31	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	$\overline{RD}$		Read strobe output pin for data bus. This function is enabled when external bus is enabled.
	IN5		Data sample input pin for input capture ICU5
56	P32	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the $\overline{WR}$/$\overline{WRL}$ pin output disabled.
	$\overline{WR}$/$\overline{WRL}$		Write strobe output pin for the data bus. This function is enabled when both the external bus and the $\overline{WR}$/$\overline{WRL}$ pin output are enabled. $\overline{WRL}$ is used to write-strobe 8 lower bits of the data bus in 16-bit access. $\overline{WR}$ is used to write-strobe 8 bits of the data bus in 8-bit access.
	INT10R		External interrupt request input pin for INT10
57	P33	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode, in external bus 8-bit mode or with the $\overline{WRH}$ pin output disabled.
	$\overline{WRH}$		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{WRH}$ output pin is enabled.
58	P34	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the hold function disabled.
	HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
	OUT4		Waveform output pin for output compare OCU4
59	P35	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the hold function disabled.
	$\overline{HAK}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
	OUT5		Waveform output pin for output compare OCU5
60	P36	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the external ready function disabled.
	RDY		Ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
	OUT6		Waveform output pin for output compare OCU6

(Continued)

4. Precautions for when not using a sub clock signal

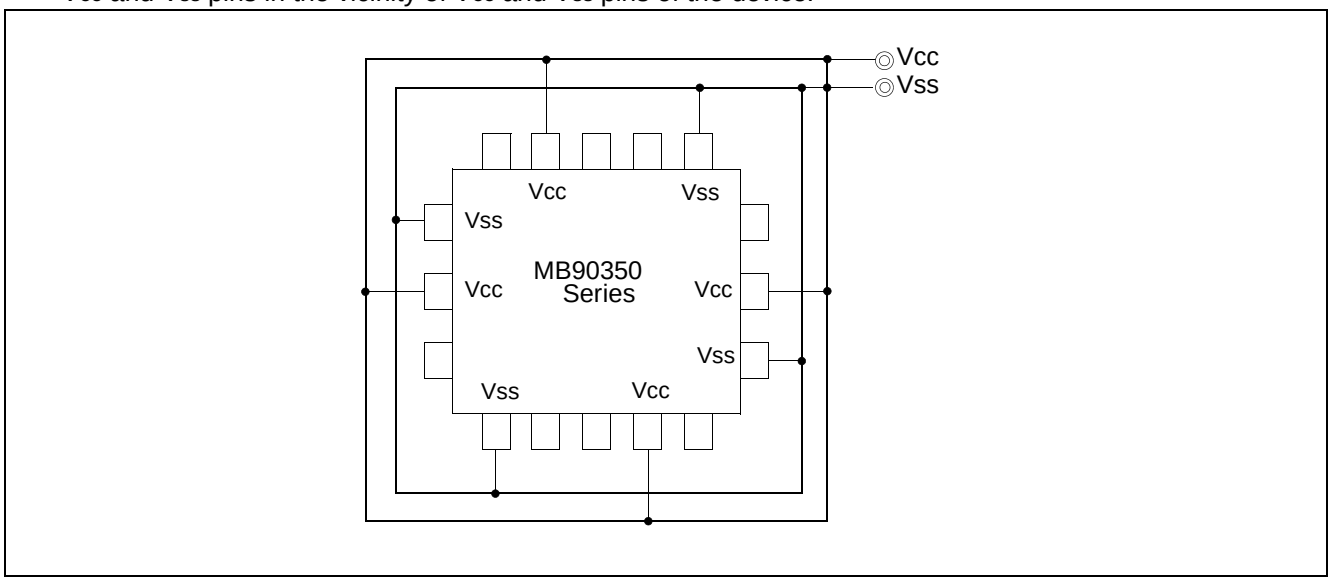
If you do not connect pins X0A and X1A to an oscillator, use pull-down handling on the X0A pin, and leave the X1A pin open.

5. Notes on during operation of PLL clock mode

If the PLL clock mode is selected, the microcontroller attempts to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

6. Power supply pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected inside of the device to prevent such malfunctioning as latch up.
  To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally.
  Connect V_{CC} and V_{SS} pins to the device from the current supply source at a low impedance.
- As a measure against power supply noise, connect a capacitor of about 0.1 µF as a bypass capacitor between V_{CC} and V_{SS} pins in the vicinity of V_{CC} and V_{SS} pins of the device.



7. Pull-up/down resistors

The MB90350 series does not support internal pull-up/down resistors (Port 0 to Port 3: built-in pull-up resistors). Use external components where needed.

8. Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board artwork surrounding X0 and X1 pins with a ground area for stabilizing the operation.

Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

9. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH) and analog inputs (AN0 to AN14) after turning-on the digital power supply (V_{CC}) .

Turn-off the digital power after turning off the A/D converter power supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

10. Connection of Unused Pins of A/D Converter if A/D Converter is used

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

11. Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 µs or more (0.2 V to 2.7 V) .

12. Stabilization of power supply voltage

A sudden change in the power supply voltage may cause the device to malfunction even within the specified V_{CC} power supply voltage operating range. Therefore, the V_{CC} power supply voltage should be stabilized.

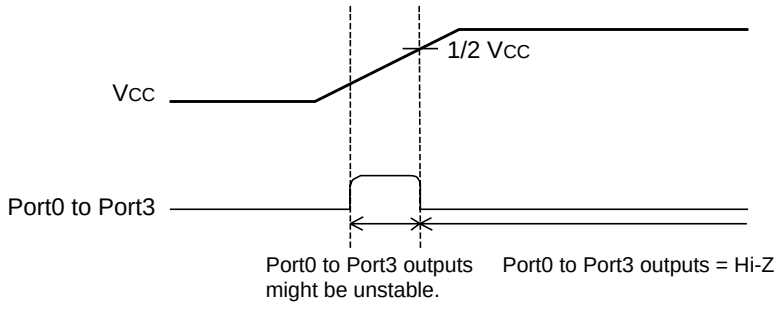
For reference, the power supply voltage should be controlled so that V_{CC} ripple variations (peak-to-peak value) at commercial frequencies (50 Hz to 60 Hz) fall below 10% of the standard V_{CC} power supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

13. Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, turn on the power again.

14. Port 0 to port 3 output during Power-on (External-bus mode)

As shown below, when power is turned on in external-bus mode, there is a possibility that output signal of Port 0 to Port 3 might be unstable.



15. Notes on using CAN Function

To use CAN function, please set “1” to DIRECT bit of CAN direct mode register (CDMR).
If DIRECT bit is set to “0” (initial value), wait states will be performed when accessing CAN registers.

Note : Please refer to section “22.15 CAN Direct Mode Register” in Hardware Manual of MB90350 series for detail of CAN direct mode register.

16. Flash security Function

The security byte is located in the area of the flash memory.
If protection code 01_H is written in the security byte, the flash memory is in the protected state by security.
Therefore please do not write 01_H in this address if you do not use the security function.
Please refer to following table for the address of the security byte.

	Flash memory size	Address for security bit
MB90F352(S) MB90F352A(S) MB90F352TA(S) MB90F357A(S) MB90F357TA(S)	Embedded 1 Mbit Flash Memory	FE0001$_H$

17. Correspondence with T_A = +105 °C or more

If used exceeding T_A = +105 °C, please contact Fujitsu sales representatives for reliability limitations.

18. Low voltage/CPU operation reset circuit

The low voltage detection reset circuit is a function that monitors power supply voltage in order to detect when a voltage drops below a given voltage level. When a low voltage condition is detected, an internal reset signal is generated.
The CPU operation detection reset circuit is a 20-bit counter that uses oscillation as a count clock and generates an internal reset signal if not cleared within a given time after startup.

(1) Low voltage detection reset circuit

Detection voltage
4.0 V ± 0.3 V

When a low voltage condition is detected, the low voltage detection flag (LVRC : LVRF) is set to “1” and an internal reset signal is output.
Because the low voltage detection reset circuit continues to operate even in stop mode, detection of a low voltage condition generates an internal reset and releases stop mode.
During an internal RAM write cycle, low voltage reset is generated after the completion of writing. During the output of this internal reset, the reset output from the low voltage detection reset circuit is suppressed.

(2) CPU operation detection reset circuit

The CPU operation detection reset circuit is a counter that prevents program runaway. The counter starts automatically after a power-on reset, and must be continually cleared within a given time. If the given time interval elapses and the counter has not been cleared, a cause such as infinite program looping is assumed and an internal reset signal is generated. The internal reset generated from the CPU operation detection circuit has a width of 5 machine cycles.

Interval time
$2^{20}/F_C$ (approx. 262 ms*)

* : This value assumes the interval time at an oscillation clock frequency of 4 MHz.
During recovery from standby mode, the detection period is the maximum interval plus 20 µs.

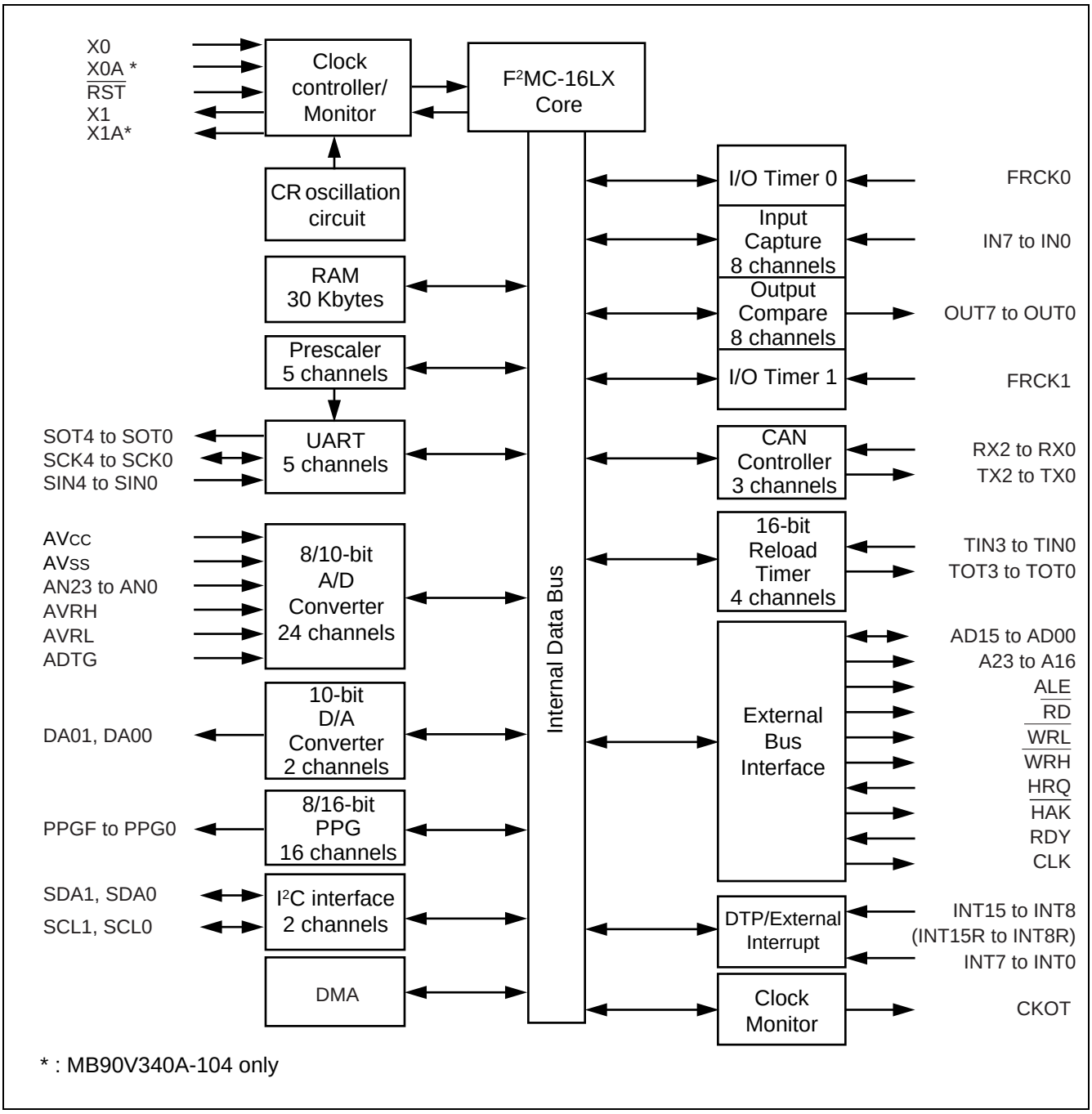
This circuit does not operate in modes where CPU operation is stopped.
The CPU operation detection reset circuit counter is cleared under any of the following conditions.

- “0” writing to CL bit of LVRC register
- Internal reset
- Main oscillation clock stop
- Transit to sleep mode
- Transit to timebase timer mode and watch mode

19. Internal CR oscillation circuit

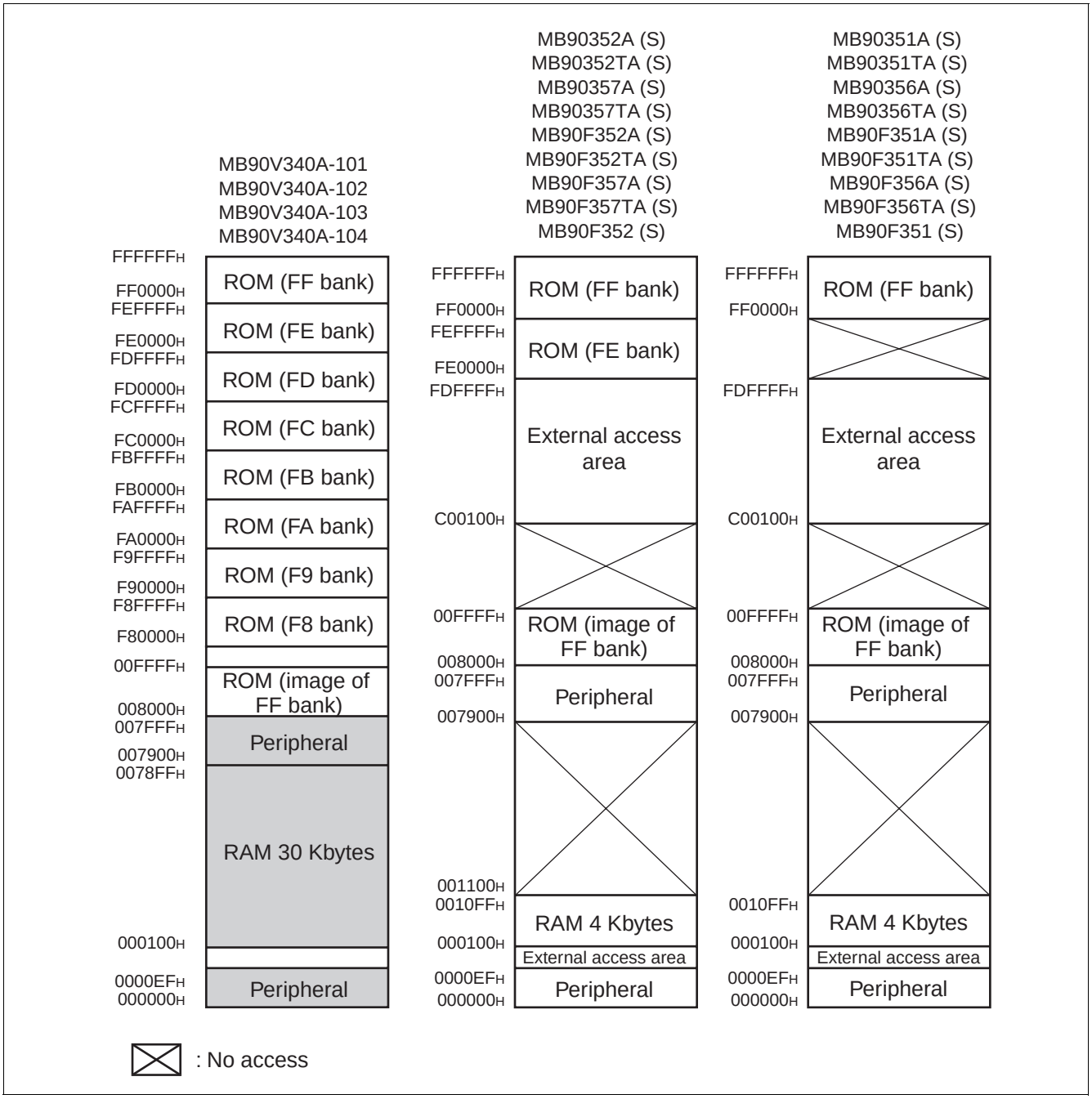
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Oscillation frequency	f_{RC}	50	100	200	kHz
Oscillation stabilization wait time	tstab	—	—	100	µs

- MB90V340A-103/104



* : MB90V340A-104 only

■ MEMORY MAP



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referenced without using the far specification in the pointer declaration.
For example, an attempt to access 00C000H accesses the value at FFC000H in ROM.
The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.
The image between FF8000H and FFFFFFH is visible in bank 00, while the image between FF0000H and FF7FFFH is visible only in bank FF.

■ I/O MAP

Address	Register	Abbreviation	Access	Resource name	Initial value
00_H	Port 0 Data Register	PDR0	R/W	Port 0	$XXXXXXXX_B$
01_H	Port 1 Data Register	PDR1	R/W	Port 1	$XXXXXXXX_B$
02_H	Port 2 Data Register	PDR2	R/W	Port 2	$XXXXXXXX_B$
03_H	Port 3 Data Register	PDR3	R/W	Port 3	$XXXXXXXX_B$
04_H	Port 4 Data Register	PDR4	R/W	Port 4	$XXXXXXXX_B$
05_H	Port 5 Data Register	PDR5	R/W	Port 5	$XXXXXXXX_B$
06_H	Port 6 Data Register	PDR6	R/W	Port 6	$XXXXXXXX_B$
07_H to $0A_H$	Reserved				
$0B_H$	Port 5 Analog Input Enable Register	ADER5	R/W	Port 5, A/D	11111111_B
$0C_H$	Port 6 Analog Input Enable Register	ADER6	R/W	Port 6, A/D	11111111_B
$0D_H$	Reserved				
$0E_H$	Input Level Select Register 0	ILSR0	R/W	Ports	00000000_B
$0F_H$	Input Level Select Register 1	ILSR1	R/W	Ports	00000000_B
10_H	Port 0 Direction Register	DDR0	R/W	Port 0	00000000_B
11_H	Port 1 Direction Register	DDR1	R/W	Port 1	00000000_B
12_H	Port 2 Direction Register	DDR2	R/W	Port 2	$XX000000_B$
13_H	Port 3 Direction Register	DDR3	R/W	Port 3	00000000_B
14_H	Port 4 Direction Register	DDR4	R/W	Port 4	$XX000000_B$
15_H	Port 5 Direction Register	DDR5	R/W	Port 5	$X0000000_B$
16_H	Port 6 Direction Register	DDR6	R/W	Port 6	00000000_B
17_H to 19_H	Reserved				
$1A_H$	SIN input Level Setting Register	DDRA	W	UART2, UART3	$X00XXXXX_B$
$1B_H$	Reserved				
$1C_H$	Port 0 Pull-up Control Register	PUCR0	R/W	Port 0	00000000_B
$1D_H$	Port 1 Pull-up Control Register	PUCR1	R/W	Port 1	00000000_B
$1E_H$	Port 2 Pull-up Control Register	PUCR2	R/W	Port 2	00000000_B
$1F_H$	Port 3 Pull-up Control Register	PUCR3	R/W	Port 3	00000000_B
20_H to 37_H	Reserved				
38_H	PPG 4 Operation Mode Control Register	PPGC4	W, R/W	16-bit Programmable Pulse Generator 4/5	$0X000XX1_B$
39_H	PPG 5 Operation Mode Control Register	PPGC5	W, R/W		$0X000001_B$
$3A_H$	PPG 4/5 Count Clock Select Register	PPG45	R/W		$000000X0_B$
$3B_H$	Address Detect Control Register 1	PACSR1	R/W	Address Match Detection 1	00000000_B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
7950H	Serial Mode Register 3	SMR3	W, R/W	UART3	00000000B
7951H	Serial Control Register 3	SCR3	W, R/W		00000000B
7952H	Reception/Transmission Data Register 3	RDR3/ TDR3	R/W		00000000B
7953H	Serial Status Register 3	SSR3	R,R/W		00001000B
7954H	Extended Communication Control Register 3	ECCR3	R,W, R/W		000000XXB
7955H	Extended Status/Control Register 3	ESCR3	R/W		00000100B
7956H	Baud Rate Generator Register 30	BGR30	R/W		00000000B
7957H	Baud Rate Generator Register 31	BGR31	R/W		00000000B
7958H, 7959H	Reserved				
7960H	Clock Monitor Function Control Register	CSVCR	R, R/W	Clock Monitor	00011100B
7961H to 796DH	Reserved				
796EH	CAN Direct Mode Register	CDMR	R/W	CAN Clock Sync	XXXXXXX0B
796FH	Reserved				
7970H	I²C Bus Status Register 0	IBSR0	R	I²C Interface 0	00000000B
7971H	I²C Bus Control Register 0	IBCR0	W,R/W		00000000B
7972H	I²C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000B
7973H		ITBAH0	R/W		00000000B
7974H	I²C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111B
7975H		ITMKH0	R/W		00111111B
7976H	I²C 7-bit Slave Address Register 0	ISBA0	R/W		00000000B
7977H	I²C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111B
7978H	I²C data register 0	IDAR0	R/W		00000000B
7979H, 797AH	Reserved				
797BH	I²C Clock Control Register 0	ICCR0	R/W	I²C Interface 0	00011111B
797CH to 79A1H	Reserved				
79A2H	Flash Write Control Register 0	FWR0	R/W	Dual Operation Flash	00000000B
79A3H	Flash Write Control Register 1	FWR1	R/W		00000000B
79A4H	Sector Change Setting Register	SSR0	R/W		00XXXXX0B
79A5H to 79C1H	Reserved				

(Continued)

■ CAN CONTROLLERS

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmitting of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbps to 2 Mbps (when input clock is at 16 MHz)

List of Control Registers

Address CAN1	Register	Abbreviation	Access	Initial Value
000080_H	Message buffer enable register	BVALR	R/W	00000000_B
000081_H				00000000_B
000082_H	Transmit request register	TREQR	R/W	00000000_B
000083_H				00000000_B
000084_H	Transmit cancel register	TCANR	W	00000000_B
000085_H				00000000_B
000086_H	Transmission complete register	TCR	R/W	00000000_B
000087_H				00000000_B
000088_H	Receive complete register	RCR	R/W	00000000_B
000089_H				00000000_B
$00008A_H$	Remote request receiving register	RRTRR	R/W	00000000_B
$00008B_H$				00000000_B
$00008C_H$	Receive overrun register	ROVRR	R/W	00000000_B
$00008D_H$				00000000_B
$00008E_H$	Reception interrupt enable register	RIER	R/W	00000000_B
$00008F_H$				00000000_B

(Continued)

(Continued)

(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

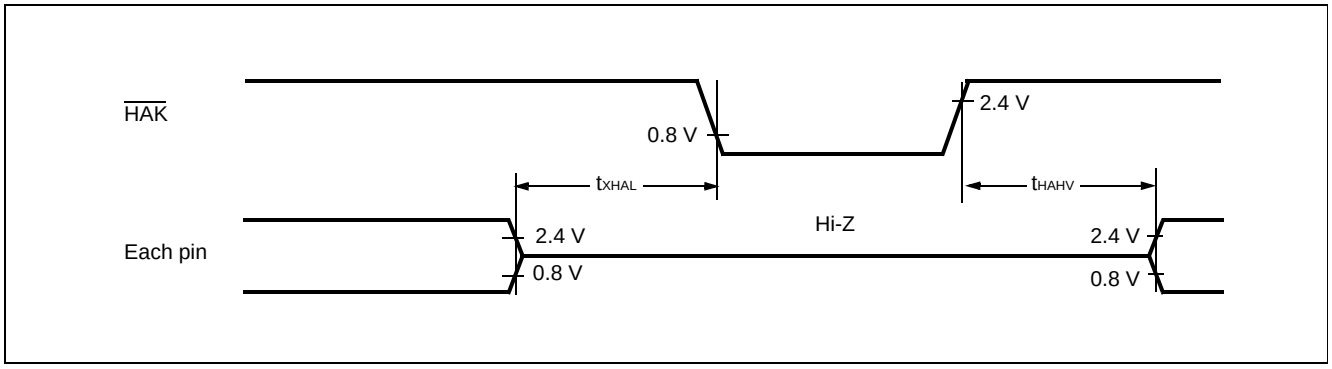
Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCT}	V_{CC}	V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock monitor function, At watch mode T_A = +25°C	—	25	150	µA	MB90F356A MB90F357A MB90356A MB90357A
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At watch mode T_A = +25°C	—	25	150	µA	MB90F356AS MB90F357AS MB90356AS MB90357AS
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock monitor function, At watch mode T_A = +25°C	—	60	140	µA	MB90F351TA MB90F352TA MB90F356TA MB90F357TA MB90351TA MB90352TA MB90356TA MB90357TA
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock monitor function, At watch mode T_A = +25°C	—	80	250	µA	MB90F356TA MB90F357TA MB90356TA MB90357TA
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At watch mode T_A = +25°C	—	80	250	µA	MB90F356TAS MB90F357TAS MB90356TAS MB90357TAS
	I_{CCH}		V_{CC} = 5.0 V, At Stop mode, T_A = +25°C	—	7	25	µA	Devices without “T”-suffix
				—	60	130	µA	Devices with “T”-suffix
Input capacity	C_{IN}	Other than C, AV_{CC}, AV_{SS}, AVRH, V_{CC}, V_{SS},	—	—	5	15	pF	

(8) Hold Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ $\overline{HAK}$ ↓ time	t_{XHAL}	$\overline{HAK}$	—	30	t_{CP}	ns	
$\overline{HAK}$ ↑ time ⇒ Pin valid time	t_{HAHV}	$\overline{HAK}$		t_{CP}	2 t_{CP}	ns	

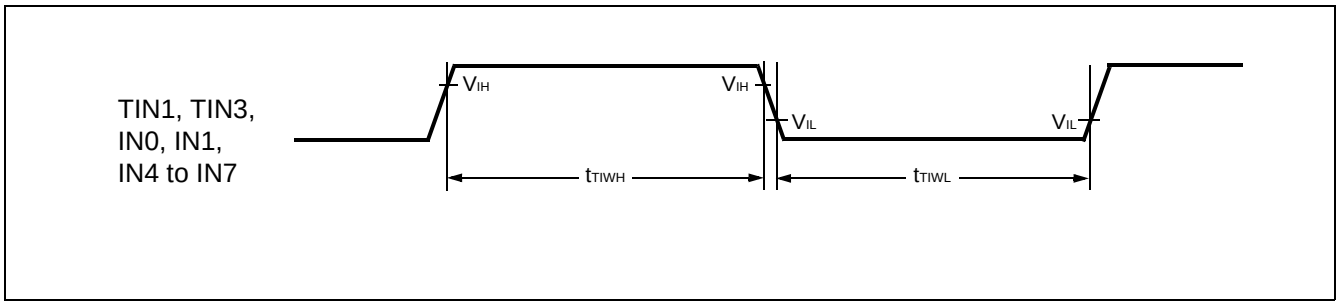
Note : There is more than 1 machine cycle from when HRQ pin reads in until the $\overline{HAK}$ is changed.



(11) Timer Related Resource Input Timing

(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

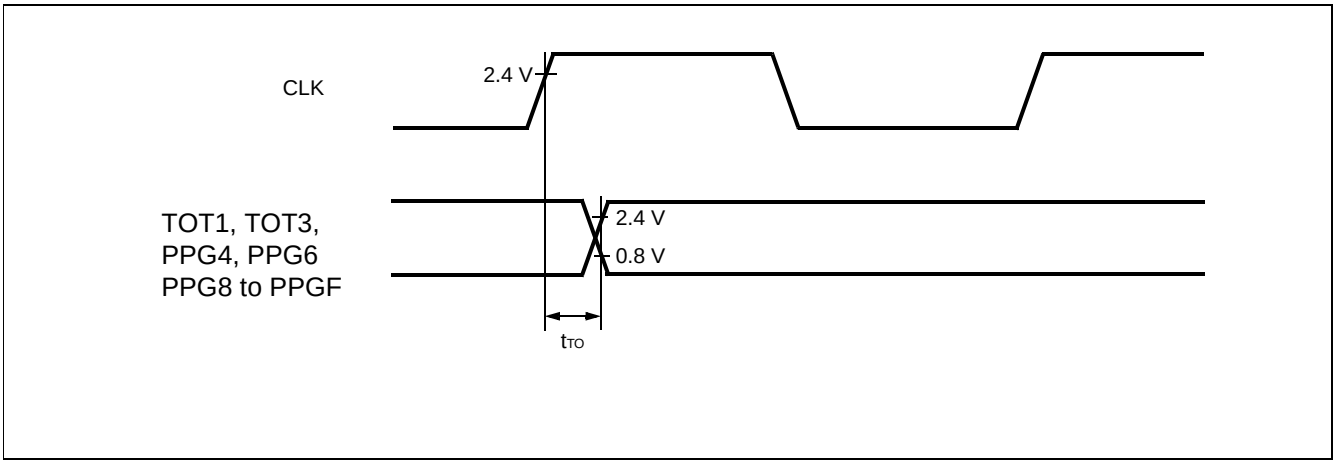
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	TIN1, TIN3, IN0, IN1, IN4 to IN7	—	4 t_{CP}	—	ns	



(12) Timer Related Resource Output Timing

(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
CLK ↑ ⇒ T_{OUT} change time	t_{TO}	TOT1, TOT3, PPG4, PPG6, PPG8 to PPGF	—	30	—	ns	



(13) I²C Timing

(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	Standard-mode		Fast-mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
Hold time for (repeated) START condition SDA↓→SCL↓	t_{HDSTA}		4.0	—	0.6	—	µs
"L" width of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
"H" width of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up time for a repeated START condition SCL↑→SDA↓	t_{SUSTA}		4.7	—	0.6	—	µs
Data hold time SCL↓→SDA↓↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs
Data set-up time SDA↓↑→SCL↑	t_{SUDAT}		250*5	—	100*5	—	ns
Set-up time for STOP condition SCL↑→SDA↑	t_{SUSTO}		4.0	—	0.6	—	µs
Bus free time between STOP condition and START condition	t_{BUS}		4.7	—	1.3	—	µs

*1 : R,C : Pull-up resistor and load capacitor of the SCL and SDA lines.

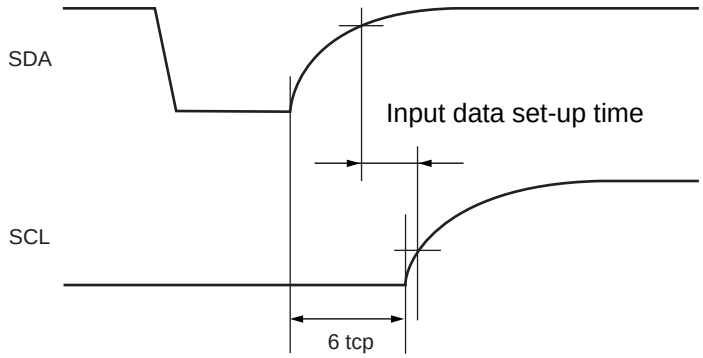
*2 : The maximum t_{HDDAT} has only to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.

*3 : A Fast-mode I²C -bus device can be used in a Standard-mode I²C-bus system, but the requirement t_{SUDAT} ≥ 250 ns must then be met.

*4 : For use at over 100 kHz, set the machine clock to at least 6 MHz.

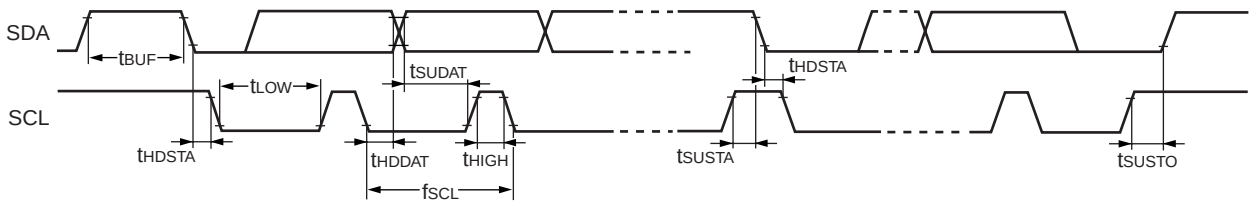
*5 : Refer to "• Note of SDA, SCL set-up time".

• Note of SDA, SCL set-up time



Note : The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.
Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.

- Timing definition

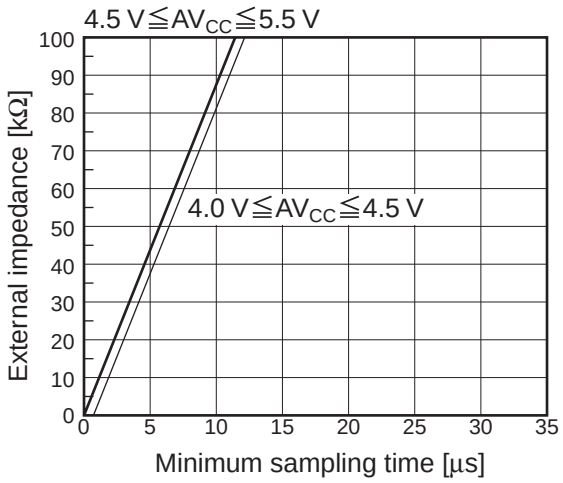


• Flash memory device

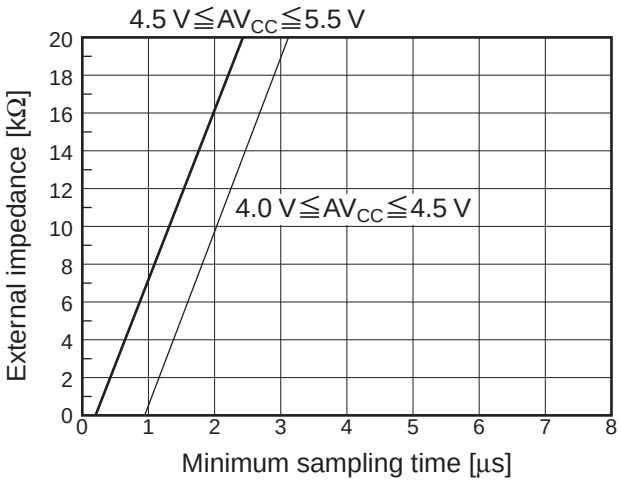
· Relation between External impedance and minimum sampling time

(MB90F352(S), MB90F351A(S), MB90F352A(S), MB90F351TA(S), MB90F352TA(S), MB90F356A(S), MB90F357A(S), MB90F356TA(S), MB90F357TA(S))

[External impedance = 0 kΩ to 100 kΩ]



[External impedance = 0 kΩ to 20 kΩ]

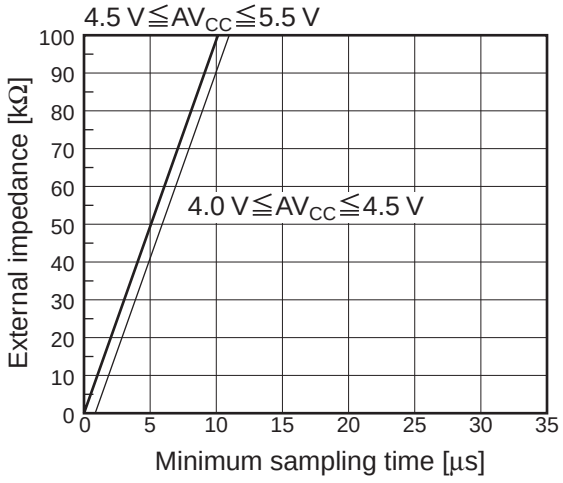


• MASK ROM device

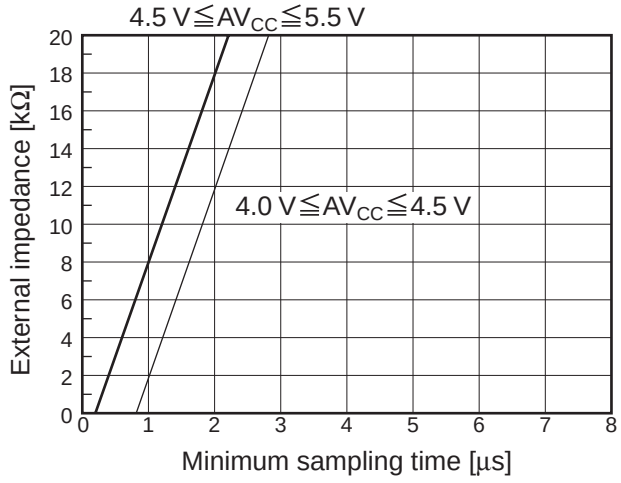
· Relation between External impedance and minimum sampling time

(MB90V340A-101/102/103/104, MB90351A(S), MB90352A(S), MB90351TA(S), MB90352TA(S), MB90356A(S), MB90357A(S), MB90356TA(S), MB90357TA(S))

[External impedance = 0 kΩ to 100 kΩ]



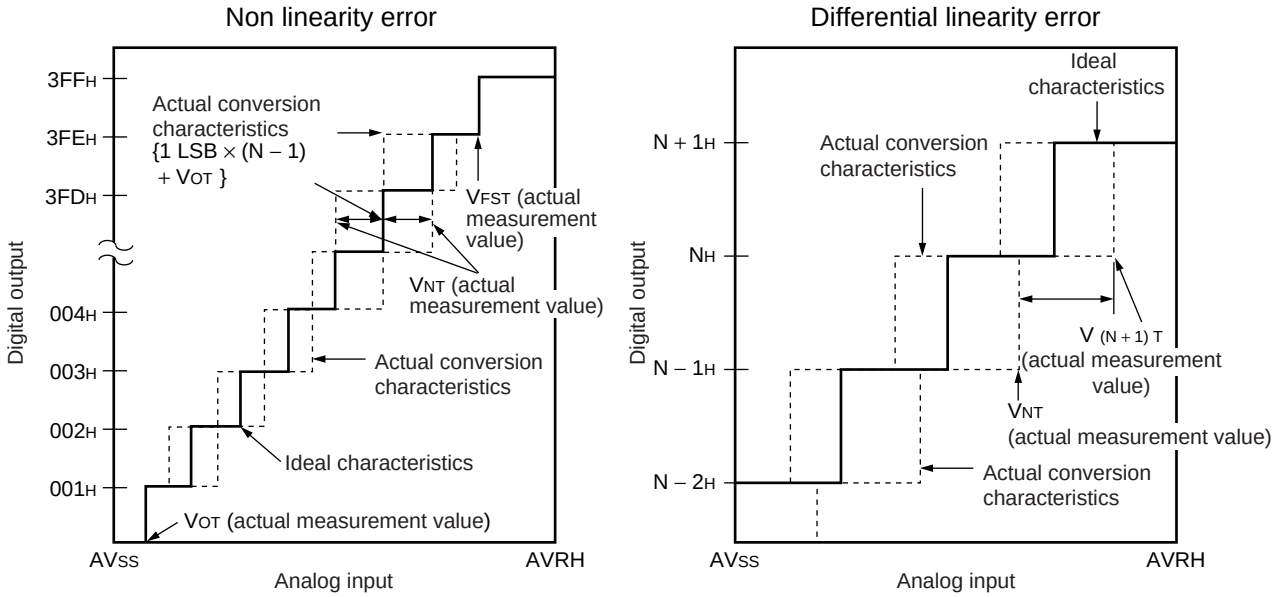
[External impedance = 0 kΩ to 20kΩ]



• **About the error**

Values of relative errors grow larger, as |AVRH – AVSS| becomes smaller.

(Continued)



$$\text{Non linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB [LSB]}$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

N : A/D converter digital output value
V_{OT} : Voltage at which digital output transits from “000_H” to “001_H.”
V_{FST} : Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”