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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 15x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-QFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f352spfm-gs-118e1

■ FEATURES

- **Clock**
  - Built-in PLL clock frequency multiplication circuit
  - Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 6 times of oscillation clock (for 4 MHz oscillation clock, 4 MHz to 24 MHz).
  - Operation by sub clock (up to 50 kHz : 100 kHz oscillation clock divided by two) is allowed. (devices without S-suffix only)
  - Minimum execution time of instruction : 42 ns (when operating with 4-MHz oscillation clock, and 6-time multiplied PLL clock).
  - Built-in clock modulation circuit
- **16 Mbytes CPU memory space**
  - 24-bit internal addressing
- **Clock monitor function (MB90x356x and MB90x357x only)**
  - Main clock or sub clock is monitored independently.
  - Internal CR oscillation clock (100 kHz typical) can be used as sub clock.
- **Instruction system best suited to controller**
  - Wide choice of data types (bit, byte, word, and long word)
  - Wide choice of addressing modes (23 types)
  - Enhanced multiply-divide instructions with sign and RETI instructions
  - Enhanced high-precision computing with 32-bit accumulator
- **Instruction system compatible with high-level language (C language) and multitask**
  - Employing system stack pointer
  - Enhanced various pointer indirect instructions
  - Barrel shift instructions
- **Increased processing speed**
  - 4-byte instruction queue
- **Powerful interrupt function**
  - Powerful 8-level, 34-condition interrupt feature
  - Up to 8 channels external interrupts are supported.
- **Automatic data transfer function independent of CPU**
  - Extended intelligent I/O service function (EI^{2}OS) : up to 16 channels
  - DMA : up to 16 channels
- **Low power consumption (standby) mode**
  - Sleep mode (a mode that halts CPU operating clock)
  - Main timer mode (a timebase timer mode switched from the main clock mode)
  - PLL timer mode (a timebase timer mode switched from the PLL clock mode)
  - Watch mode (a mode that operates sub clock and watch timer only)
  - Stop mode (a mode that stops oscillation clock and sub clock)
  - CPU intermittent operation mode
- **Process**
  - CMOS technology

(Continued)

■ PACKAGES AND PRODUCT CORRESPONDENCE

Package	MB90V340A -101 -102 -103 -104	MB90F351 MB90F351S MB90F352 MB90F352S	MB90F351A (S) , MB90F351TA (S) MB90F352A (S) , MB90F352TA (S) MB90F356A (S) , MB90F356TA (S) MB90F357A (S) , MB90F357TA (S) MB90351A (S) , MB90351TA (S) MB90352A (S) , MB90352TA (S) MB90356A (S) , MB90356TA (S) MB90357A (S) , MB90357TA (S)
PGA-299C-A01	◯	×	×
FPT-64P-M09 (12 mm □, 0.65 mm pitch)	×	◯	×
FPT-64P-M23 (12 mm □, 0.65 mm pitch)	×	×	◯
FPT-64P-M24 (10 mm □, 0.50 mm pitch)	×	×	◯*

* : This device is under development.
◯ : Yes, × : No

Note : Refer to “■ PACKAGE DIMENSIONS” for detail of each package.

Pin No. LQFP64*	Pin name	Circuit type	Function
24 to 31	P00 to P07	G	General purpose I/O ports. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD00 to AD07		Input/output pins of external address data bus lower 8 bits. This function is enabled when the external bus is enabled.
	INT8 to INT15		External interrupt request input pins for INT8 to INT15
32	P10	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD08		Input/output pin for external bus address data bus bit 8. This function is enabled when external bus is enabled.
	TIN1		Event input pin for reload timer1
33	P11	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD09		Input/output pin for external bus address data bus bit 9. This function is enabled when external bus is enabled.
	TOT1		Output pin for reload timer1
34	P12	N	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD10		Input/output pin for external bus address data bus bit 10. This function is enabled when external bus is enabled.
	SIN3		Serial data input pin for UART3
	INT11R		External interrupt request input pin for INT11
35	P13	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD11		Input/output pin for external bus address data bus bit 11. This function is enabled when external bus is enabled.
	SOT3		Serial data output pin for UART3
36	P14	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD12		Input/output pin for external bus address data bus bit 12. This function is enabled when external bus is enabled.
	SCK3		Clock input/output pin for UART3
37	P15	N	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD13		Input/output pin for external bus address data bus bit 13. This function is enabled when external bus is enabled.
38	P16	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD14		Input/output pin for external bus address data bus bit 14. This function is enabled when external bus is enabled.

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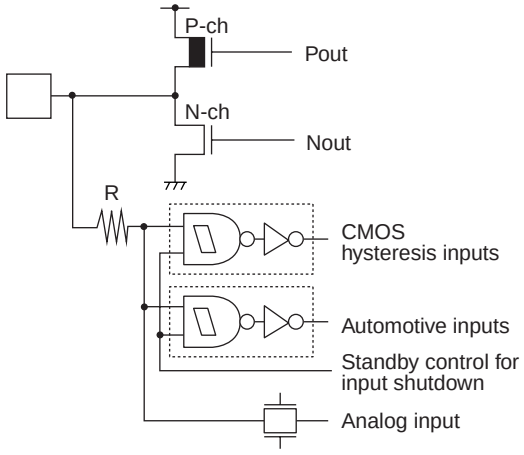
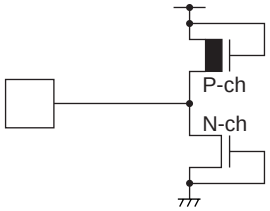
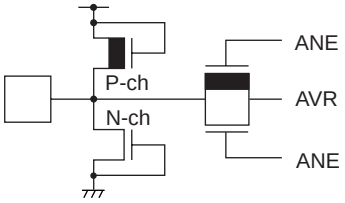
Type	Circuit	Remarks
I		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis inputs (With the stand-by-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • A/D analog input
K		• Power supply input protection circuit
L		• A/D converter reference voltage power supply input pin, with the protection circuit • Flash memory devices do not have a protection circuit against V_{CC} for pin AVRH.

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■ HANDLING DEVICES

Special care is required for the following when handling the device :

- Preventing latch-up
- Treatment of unused pins
- Using external clock
- Precautions for when not using a sub clock signal
- Notes on during operation of PLL clock mode
- Power supply pins (V_{CC}/V_{SS})
- Pull-up/down resistors
- Crystal Oscillator Circuit
- Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs
- Connection of Unused Pins of A/D Converter
- Notes on Energization
- Stabilization of power supply voltage
- Initialization
- Port0 to port3 output during Power-on (External-bus mode)
- Notes on using CAN Function
- Flash security Function
- Correspondence with T_A = + 105 °C or more
- Low voltage/CPU operation detection reset circuit
- Internal CR oscillation circuit

1. Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pin and V_{SS} pin.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

In using the devices, take sufficient care to avoid exceeding maximum ratings.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

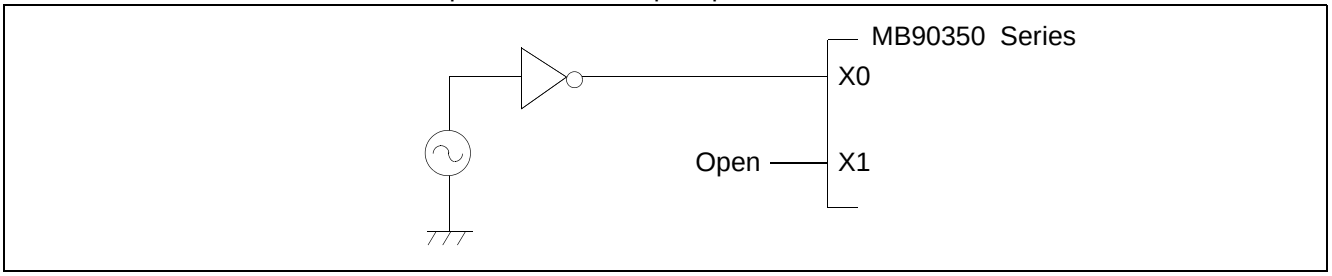
2. Handling unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ .

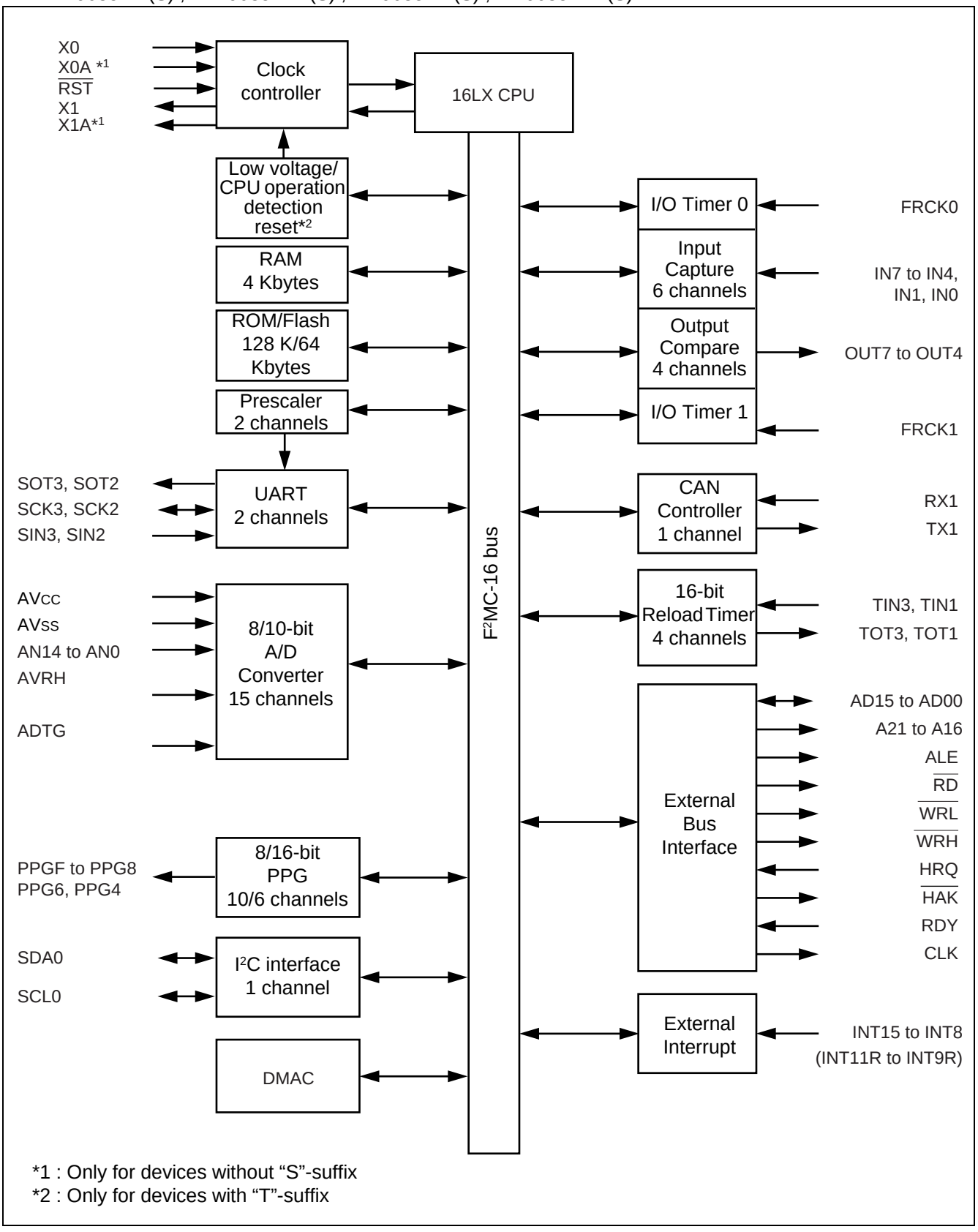
Unused I/O pins should be set to the output state and can be left open, or the input state with the above described connection.

3. Using external clock

To use external clock, drive the X0 pin and leave X1 pin open.



- MB90F352 (S) , MB90F351 (S) , MB90F352A (S) , MB90F352TA (S) , MB90F351A (S) , MB90F351TA (S) , MB90352A (S) , MB90352TA (S) , MB90351A (S) , MB90351TA (S)



*1 : Only for devices without “S”-suffix
*2 : Only for devices with “T”-suffix

Address	Register	Abbreviation	Access	Resource name	Initial value
CA$_H$	External Interrupt Enable Register 1	ENIR1	R/W	External Interrupt 1	00000000$_B$
CB$_H$	External Interrupt Source Register 1	EIRR1	R/W		XXXXXXXX$_B$
CC$_H$	External Interrupt Level Register 1	ELVR1	R/W		00000000$_B$
CD$_H$	External Interrupt Level Register 1	ELVR1	R/W		00000000$_B$
CE$_H$	External Interrupt Source Select Register	EISSR	R/W		00000000$_B$
CF$_H$	PLL/Sub clock Control register	PSCCR	W	PLL	XXXX0000$_B$
D0$_H$	DMA Buffer Address Pointer L	BAPL	R/W	DMA	XXXXXXXX$_B$
D1$_H$	DMA Buffer Address Pointer M	BAPM	R/W		XXXXXXXX$_B$
D2$_H$	DMA Buffer Address Pointer H	BAPH	R/W		XXXXXXXX$_B$
D3$_H$	DMA Control Register	DMACS	R/W		XXXXXXXX$_B$
D4$_H$	I/O Register Address Pointer L	IOAL	R/W		XXXXXXXX$_B$
D5$_H$	I/O Register Address Pointer H	IOAH	R/W		XXXXXXXX$_B$
D6$_H$	Data Counter L	DCTL	R/W		XXXXXXXX$_B$
D7$_H$	Data Counter H	DCTH	R/W		XXXXXXXX$_B$
D8$_H$	Serial Mode Register 2	SMR2	W,R/W	UART2	00000000$_B$
D9$_H$	Serial Control Register 2	SCR2	W,R/W		00000000$_B$
DA$_H$	Reception/Transmission Data Register 2	RDR2/ TDR2	R/W		00000000$_B$
DB$_H$	Serial Status Register 2	SSR2	R,R/W		00001000$_B$
DC$_H$	Extended Communication Control Register 2	ECCR2	R,W, R/W		000000XX$_B$
DD$_H$	Extended Status/Control Register 2	ESCR2	R/W		00000100$_B$
DE$_H$	Baud Rate Generator Register 20	BGR20	R/W		00000000$_B$
DF$_H$	Baud Rate Generator Register 21	BGR21	R/W		00000000$_B$
E0$_H$ to EF$_H$	Reserved				
F0$_H$ to FF$_H$	External area				
7900$_H$ to 7907$_H$	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
792C$_H$	Input Capture Register 6	IPCP6	R	Input Capture 6/7	XXXXXXXX$_B$
792D$_H$	Input Capture Register 6	IPCP6	R		XXXXXXXX$_B$
792E$_H$	Input Capture Register 7	IPCP7	R		XXXXXXXX$_B$
792F$_H$	Input Capture Register 7	IPCP7	R		XXXXXXXX$_B$
7930$_H$ to 7937$_H$	Reserved				
7938$_H$	Output Compare Register 4	OCCP4	R/W	Output Compare 4/5	XXXXXXXX$_B$
7939$_H$	Output Compare Register 4	OCCP4	R/W		XXXXXXXX$_B$
793A$_H$	Output Compare Register 5	OCCP5	R/W		XXXXXXXX$_B$
793B$_H$	Output Compare Register 5	OCCP5	R/W		XXXXXXXX$_B$
793C$_H$	Output Compare Register 6	OCCP6	R/W	Output Compare 6/7	XXXXXXXX$_B$
793D$_H$	Output Compare Register 6	OCCP6	R/W		XXXXXXXX$_B$
793E$_H$	Output Compare Register 7	OCCP7	R/W		XXXXXXXX$_B$
793F$_H$	Output Compare Register 7	OCCP7	R/W		XXXXXXXX$_B$
7940$_H$	Timer Data Register 0	TCDT0	R/W	I/O Timer 0	00000000$_B$
7941$_H$	Timer Data Register 0	TCDT0	R/W		00000000$_B$
7942$_H$	Timer Control Status Register 0	TCCSL0	R/W		00000000$_B$
7943$_H$	Timer Control Status Register 0	TCCSH0	R/W		0XXXXXXX$_B$
7944$_H$	Timer Data Register 1	TCDT1	R/W	I/O Timer 1	00000000$_B$
7945$_H$	Timer Data Register 1	TCDT1	R/W		00000000$_B$
7946$_H$	Timer Control Status Register 1	TCCSL1	R/W		00000000$_B$
7947$_H$	Timer Control Status Register 1	TCCSH1	R/W		0XXXXXXX$_B$
7948$_H$	Timer Register 0/Reload Register 0	TMR0/ TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXX$_B$
7949$_H$			R/W		XXXXXXXX$_B$
794A$_H$	Timer Register 1/Reload Register 1	TMR1/ TMRLR1	R/W	16-bit Reload Timer 1	XXXXXXXX$_B$
794B$_H$			R/W		XXXXXXXX$_B$
794C$_H$	Timer Register 2/Reload Register 2	TMR2/ TMRLR2	R/W	16-bit Reload Timer 2	XXXXXXXX$_B$
794D$_H$			R/W		XXXXXXXX$_B$
794E$_H$	Timer Register 3/Reload Register 3	TMR3/ TMRLR3	R/W	16-bit Reload Timer 3	XXXXXXXX$_B$
794F$_H$			R/W		XXXXXXXX$_B$

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Address	Register	Abbreviation	Access	Resource name	Initial value
79C2H	Setting Prohibited				
79C3H to 79DFH	Reserved				
79E0H	Detect Address Setting Register 0	PADR0	R/W	Address Match Detection 0	XXXXXXXXB
79E1H	Detect Address Setting Register 0	PADR0	R/W		XXXXXXXXB
79E2H	Detect Address Setting Register 0	PADR0	R/W		XXXXXXXXB
79E3H	Detect Address Setting Register 1	PADR1	R/W		XXXXXXXXB
79E4H	Detect Address Setting Register 1	PADR1	R/W		XXXXXXXXB
79E5H	Detect Address Setting Register 1	PADR1	R/W		XXXXXXXXB
79E6H	Detect Address Setting Register 2	PADR2	R/W		XXXXXXXXB
79E7H	Detect Address Setting Register 2	PADR2	R/W		XXXXXXXXB
79E8H	Detect Address Setting Register 2	PADR2	R/W		XXXXXXXXB
79E9H to 79EFH	Reserved				
79F0H	Detect Address Setting Register 3	PADR3	R/W	Address Match Detection 1	XXXXXXXXB
79F1H	Detect Address Setting Register 3	PADR3	R/W		XXXXXXXXB
79F2H	Detect Address Setting Register 3	PADR3	R/W		XXXXXXXXB
79F3H	Detect Address Setting Register 4	PADR4	R/W		XXXXXXXXB
79F4H	Detect Address Setting Register 4	PADR4	R/W		XXXXXXXXB
79F5H	Detect Address Setting Register 4	PADR4	R/W		XXXXXXXXB
79F6H	Detect Address Setting Register 5	PADR5	R/W		XXXXXXXXB
79F7H	Detect Address Setting Register 5	PADR5	R/W		XXXXXXXXB
79F8H	Detect Address Setting Register 5	PADR5	R/W		XXXXXXXXB
79F9H to 7BFFH	Reserved				
7C00H to 7CFFH	Reserved for CAN Interface 1. Refer to “■ CAN CONTROLLERS”				
7D00H to 7DFFH	Reserved for CAN Interface 1. Refer to “■ CAN CONTROLLERS”				
7E00H to 7FFFH	Reserved				

Notes :
- Initial value of “X” represents unknown value.
- Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results reading “X”.

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Address CAN1	Register	Abbreviation	Access	Initial Value
007D00H	Control status register	CSR	R/W, W R/W, R	0XXXX0X1B 00XXX000B
007D01H				
007D02H	Last event indicator register	LEIR	R/W	000X0000B XXXXXXXXB
007D03H				
007D04H	Receive/transmit error counter	RTEC	R	00000000B 00000000B
007D05H				
007D06H	Bit timing register	BTR	R/W	11111111B X1111111B
007D07H				
007D08H	IDE register	IDER	R/W	XXXXXXXXB XXXXXXXXB
007D09H				
007D0AH	Transmit RTR register	TRTRR	R/W	00000000B 00000000B
007D0BH				
007D0CH	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXXB XXXXXXXXB
007D0DH				
007D0EH	Transmit interrupt enable register	TIER	R/W	00000000B 00000000B
007D0FH				
007D10H	Acceptance mask select register	AMSR	R/W	XXXXXXXXB XXXXXXXXB
007D11H				
007D12H				XXXXXXXXB XXXXXXXXB
007D13H				
007D14H	Acceptance mask register 0	AMR0	R/W	XXXXXXXXB XXXXXXXXB
007D15H				
007D16H				XXXXXXXXB XXXXXXXXB
007D17H				
007D18H	Acceptance mask register 1	AMR1	R/W	XXXXXXXXB XXXXXXXXB
007D19H				
007D1AH				XXXXXXXXB XXXXXXXXB
007D1BH				

(Continued)

Address CAN1	Register	Abbreviation	Access	Initial Value
007C40H	ID register 8	IDR8	R/W	XXXXXXXXB XXXXXXXXB
007C41H				
007C42H				XXXXXXXXB XXXXXXXXB
007C43H				
007C44H	ID register 9	IDR9	R/W	XXXXXXXXB XXXXXXXXB
007C45H				
007C46H				XXXXXXXXB XXXXXXXXB
007C47H				
007C48H	ID register 10	IDR10	R/W	XXXXXXXXB XXXXXXXXB
007C49H				
007C4AH				XXXXXXXXB XXXXXXXXB
007C4BH				
007C4CH	ID register 11	IDR11	R/W	XXXXXXXXB XXXXXXXXB
007C4DH				
007C4EH				XXXXXXXXB XXXXXXXXB
007C4FH				
007C50H	ID register 12	IDR12	R/W	XXXXXXXXB XXXXXXXXB
007C51H				
007C52H				XXXXXXXXB XXXXXXXXB
007C53H				
007C54H	ID register 13	IDR13	R/W	XXXXXXXXB XXXXXXXXB
007C55H				
007C56H				XXXXXXXXB XXXXXXXXB
007C57H				
007C58H	ID register 14	IDR14	R/W	XXXXXXXXB XXXXXXXXB
007C59H				
007C5AH				XXXXXXXXB XXXXXXXXB
007C5BH				
007C5CH	ID register 15	IDR15	R/W	XXXXXXXXB XXXXXXXXB
007C5DH				
007C5EH				XXXXXXXXB XXXXXXXXB
007C5FH				

■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt cause	EI²OS corresponding	DMA ch number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	N	—	#08	FFFFDC$_H$	—	—
INT9 instruction	N	—	#09	FFFFD8$_H$	—	—
Exception	N	—	#10	FFFFD4$_H$	—	—
Reserved	N	—	#11	FFFFD0$_H$	ICR00	0000B0$_H$
Reserved	N	—	#12	FFFFCC$_H$		
CAN 1 RX / Input Capture 6	Y1	—	#13	FFFFC8$_H$	ICR01	0000B1$_H$
CAN 1 TX/NS / Input Capture 7	Y1	—	#14	FFFFC4$_H$		
I²C	N	—	#15	FFFFC0$_H$	ICR02	0000B2$_H$
Reserved	N	—	#16	FFFFBC$_H$		
16-bit Reload Timer 0	Y1	0	#17	FFFFB8$_H$	ICR03	0000B3$_H$
16-bit Reload Timer 1	Y1	1	#18	FFFFB4$_H$		
16-bit Reload Timer 2	Y1	2	#19	FFFFB0$_H$	ICR04	0000B4$_H$
16-bit Reload Timer 3	Y1	—	#20	FFFFAC$_H$		
PPG 4/5	N	—	#21	FFFFA8$_H$	ICR05	0000B5$_H$
PPG 6/7	N	—	#22	FFFFA4$_H$		
PPG 8/9/C/D	N	—	#23	FFFFA0$_H$	ICR06	0000B6$_H$
PPG A/B/E/F	N	—	#24	FFFF9C$_H$		
Timebase Timer	N	—	#25	FFFF98$_H$	ICR07	0000B7$_H$
External Interrupt 8 to 11	Y1	3	#26	FFFF94$_H$		
Watch Timer	N	—	#27	FFFF90$_H$	ICR08	0000B8$_H$
External Interrupt 12 to 15	Y1	4	#28	FFFF8C$_H$		
A/D Converter	Y1	5	#29	FFFF88$_H$	ICR09	0000B9$_H$
I/O Timer 0 / I/O Timer 1	N	—	#30	FFFF84$_H$		
Input Capture 4/5	Y1	6	#31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 4/5	Y1	7	#32	FFFF7C$_H$		
Input Capture 0/1	Y1	8	#33	FFFF78$_H$	ICR11	0000BB$_H$
Output Compare 6/7	Y1	9	#34	FFFF74$_H$		
Reserved	N	10	#35	FFFF70$_H$	ICR12	0000BC$_H$
Reserved	N	11	#36	FFFF6C$_H$		
UART 3 RX	Y2	12	#37	FFFF68$_H$	ICR13	0000BD$_H$
UART 3 TX	Y1	13	#38	FFFF64$_H$		

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*1: This parameter is based on V_{SS} = AV_{SS} = 0 V

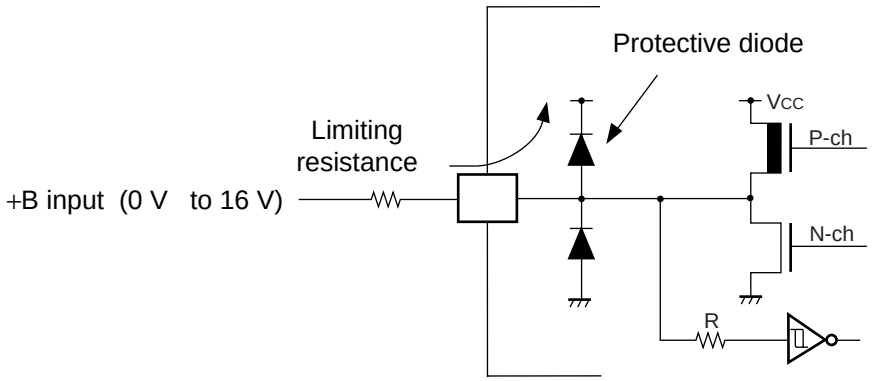
*2: Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4: Applicable to pins: P00 to P07, P10 to P17, P20 to P25, P30 to P37, P40 to P45, P50 to P56, P60 to P67

*5: • Applicable to pins: P00 to P07, P10 to P17, P20 to P25, P30 to P37, P40 to P45, P50 to P56 (for evaluation device : P50 to P55) , P60 to P67
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Sample recommended circuits:

• Input/output equivalent circuits



*6 : If used exceeding T_A = +105 °C, be sure to contact Fujitsu for reliability limitations.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

3. DC Characteristics

(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, $f_{CP} \leq$ 24 MHz, $V_{SS} = AV_{SS}$ = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, $f_{CP} \leq$ 16 MHz, $V_{SS} = AV_{SS}$ = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, $f_{CP} \leq$ 24 MHz, $V_{SS} = AV_{SS}$ = 0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage (At V_{CC} = 5 V ± 10%)	V_{IHS}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Pin inputs if CMOS hysteresis input levels are selected (except P12, P15, P44, P45, P50)
	V_{IHA}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Pin inputs if AUTOMOTIVE input levels are selected
	V_{IHT}	—	—	2.0	—	V_{CC} + 0.3	V	Pin inputs if TTL input levels are selected
	V_{IHS}	—	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P12, P15, P50 inputs if CMOS input levels are selected
	V_{IHI}	—	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P44, P45 inputs if CMOS hysteresis input levels are selected
	V_{IHR}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{IHM}	—	—	V_{CC} – 0.3	—	V_{CC} + 0.3	V	MD input pin
Input L voltage (At V_{CC} = 5 V ± 10%)	V_{ILS}	—	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Pin inputs if CMOS hysteresis input levels are selected (except P12, P15, P44, P45, P50)
	V_{ILA}	—	—	V_{SS} – 0.3	—	0.5 V_{CC}	V	Pin inputs if AUTOMOTIVE input levels are selected
	V_{ILT}	—	—	V_{SS} – 0.3	—	0.8	V	Pin inputs if TTL input levels are selected
	V_{ILS}	—	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	P12, P15, P50 inputs if CMOS input levels are selected
	V_{ILI}	—	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	P44, P45 inputs if CMOS hysteresis input levels are selected
	V_{ILR}	—	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{ILM}	—	—	V_{SS} – 0.3	—	V_{SS} + 0.3	V	MD input pin
Output H voltage	V_{OH}	Normal outputs	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
Output H voltage	V_{OHI}	I^2C current outputs	V_{CC} = 4.5 V, I_{OH} = –3.0 mA	V_{CC} – 0.5	—	—	V	

(Continued)

(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output L voltage	V_{OL}	Normal outputs	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
Output L voltage	V_{OLI}	I^2C current outputs	V_{CC} = 4.5 V, I_{OL} = 3.0 mA	—	—	0.4	V	
Input leak current	I_{IL}	—	V_{CC} = 5.5 V, V_{SS}<V_I<V_{CC}	– 1	—	1	µA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P25, P30 to P37, $\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	Except Flash memory devices
Power supply current	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internal frequency : 24 MHz, At normal operation.	—	48	60	mA	
			V_{CC} = 5.0 V, Internal frequency : 24 MHz, At writing FLASH memory.	—	53	65	mA	Flash memory devices
			V_{CC} = 5.0 V, Internal frequency : 24 MHz, At erasing FLASH memory.	—	58	70	mA	Flash memory devices
	I_{CCS}		V_{CC} = 5.0 V, Internal frequency : 24 MHz, At Sleep mode.	—	25	35	mA	
	I_{CTS}		V_{CC} = 5.0 V, Internal frequency : 2 MHz, At Main Timer mode	—	0.3	0.8	mA	Devices without “T”-suffix
				—	0.4	1.0	mA	Devices with “T”-suffix
	$I_{CTSPLL6}$		V_{CC} = 5.0 V, Internal frequency : 24 MHz, At PLL Timer mode, external frequency = 4 MHz	—	4	7	mA	
	I_{CCL}		V_{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock monitor function, At sub clock operation T_A = +25°C	—	70	140	µA	MB90F351 MB90F352 MB90F351A MB90F352A MB90F356A MB90F357A MB90351A MB90352A MB90356A MB90357A

(Continued)

(5) Bus Timing (Read)

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 10$	—	ns	
Valid address ⇒ ALE ↓ time	t_{AVLL}	ALE, A21 to A16, AD15 to AD00		$t_{CP}/2 - 20$	—	ns	
ALE ↓ ⇒ Address valid time	t_{LLAX}	ALE, AD15 to AD00		$t_{CP}/2 - 15$	—	ns	
Valid address ⇒ $\overline{RD}$ ↓ time	t_{AVRL}	A21 toA16, AD15 to AD00, $\overline{RD}$		$t_{CP} - 15$	—	ns	
Valid address ⇒ Valid data input	t_{AVDV}	A21 to A16, AD15 to AD00		—	$5\ t_{CP}/2 - 60$	ns	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		$(n^*+3/2)\ t_{CP} - 20$	—	ns	
$\overline{RD}$ ↓ ⇒ Valid data input	t_{RLDV}	$\overline{RD}$, AD15 to AD00		—	$(n^*+3/2)\ t_{CP} - 50$	ns	
$\overline{RD}$ ↑ ⇒ Data hold time	t_{RHDX}	$\overline{RD}$, AD15 to AD00		0	—	ns	
$\overline{RD}$ ↑ ⇒ ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE		$t_{CP}/2 - 15$	—	ns	
$\overline{RD}$ ↑ ⇒ Address valid time	t_{RHAX}	$\overline{RD}$, A21 to A16		$t_{CP}/2 - 10$	—	ns	
Valid address ⇒ CLK ↑ time	t_{AVCH}	A21 to A16, AD15 to AD00, CLK		$t_{CP}/2 - 16$	—	ns	
$\overline{RD}$ ↓ ⇒ CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK		$t_{CP}/2 - 15$	—	ns	
ALE ↓ ⇒ $\overline{RD}$ ↓ time	t_{LLRL}	ALE, $\overline{RD}$		$t_{CP}/2 - 15$	—	ns	

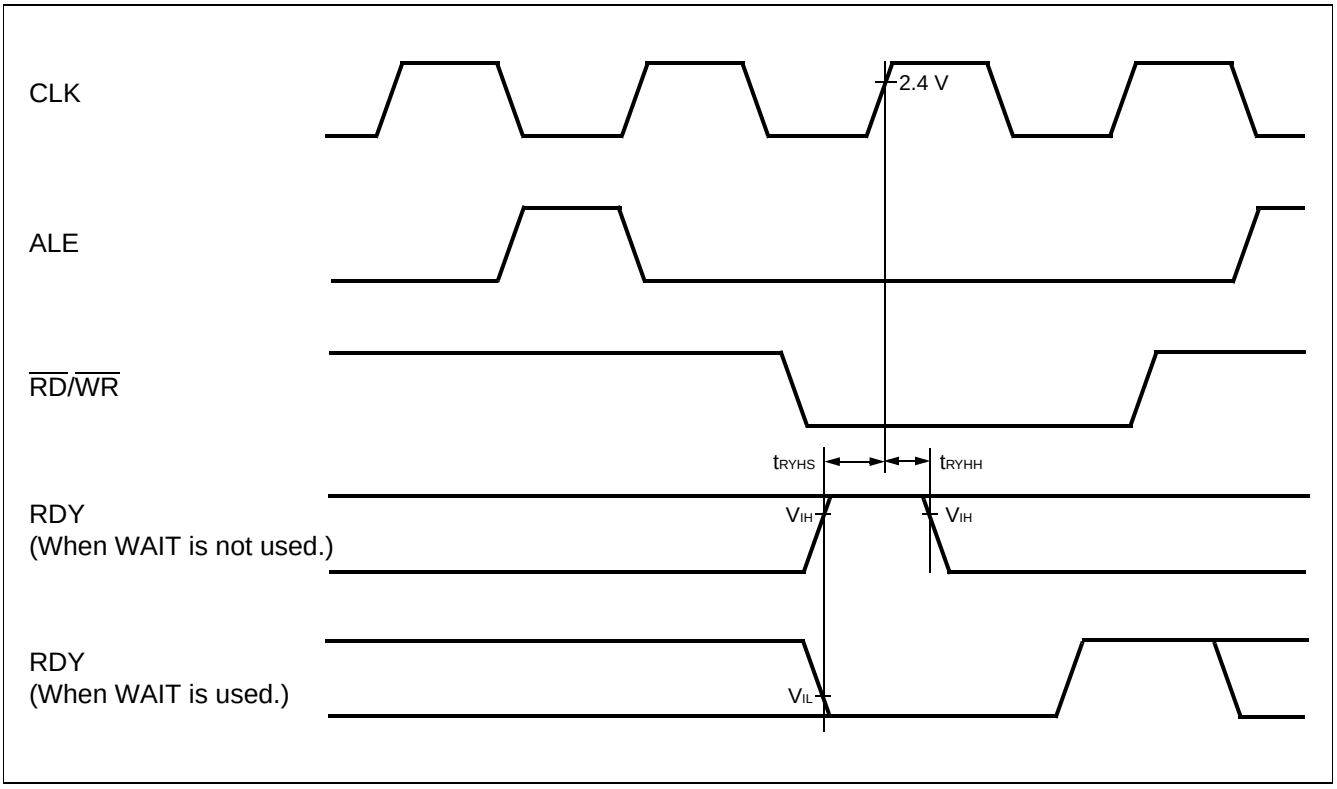
* : n: number of ready cycles

(7) Ready Input Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
RDY set-up time	t_{RYHS}	RDY	—	45	—	ns	f_{CP} = 16 MHz
				32	—	ns	f_{CP} = 24 MHz
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note : If the RDY set-up time is insufficient, use the auto-ready function.

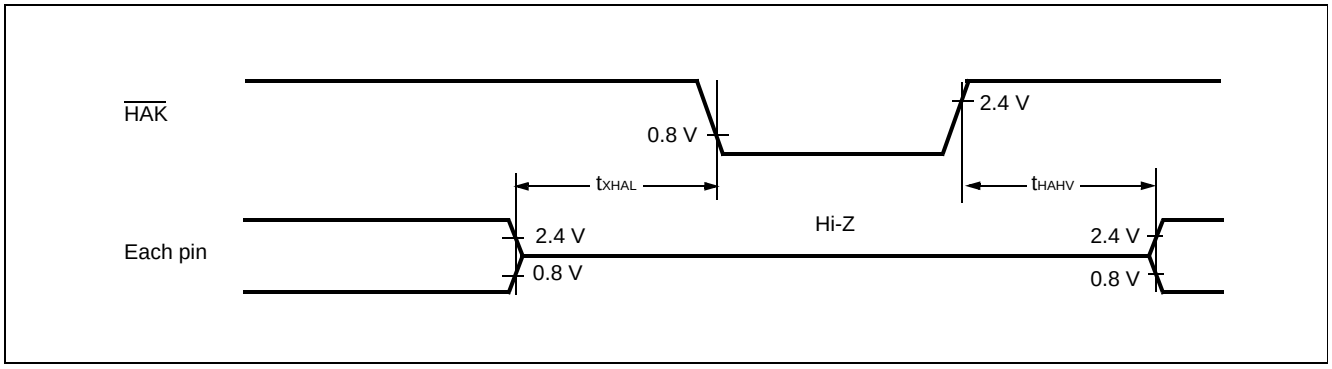


(8) Hold Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ $\overline{HAK}$ ↓ time	t_{XHAL}	$\overline{HAK}$	—	30	t_{CP}	ns	
$\overline{HAK}$ ↑ time ⇒ Pin valid time	t_{HAHV}	$\overline{HAK}$		t_{CP}	2 t_{CP}	ns	

Note : There is more than 1 machine cycle from when HRQ pin reads in until the $\overline{HAK}$ is changed.

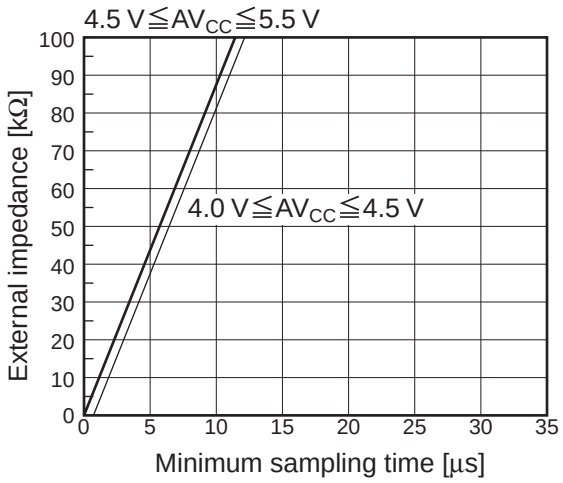


• Flash memory device

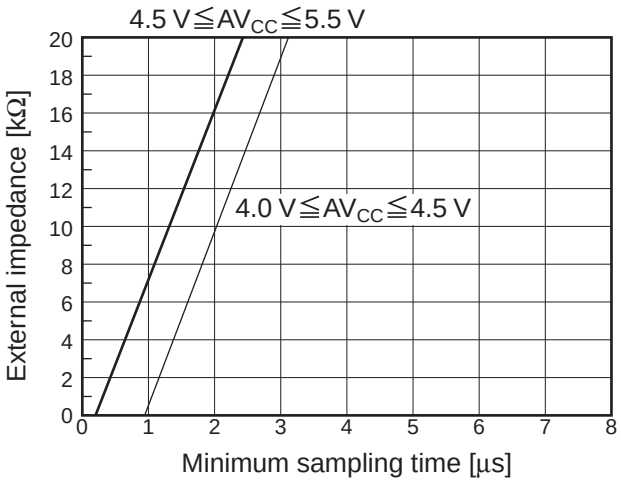
· Relation between External impedance and minimum sampling time

(MB90F352(S), MB90F351A(S), MB90F352A(S), MB90F351TA(S), MB90F352TA(S), MB90F356A(S), MB90F357A(S), MB90F356TA(S), MB90F357TA(S))

[External impedance = 0 kΩ to 100 kΩ]



[External impedance = 0 kΩ to 20 kΩ]

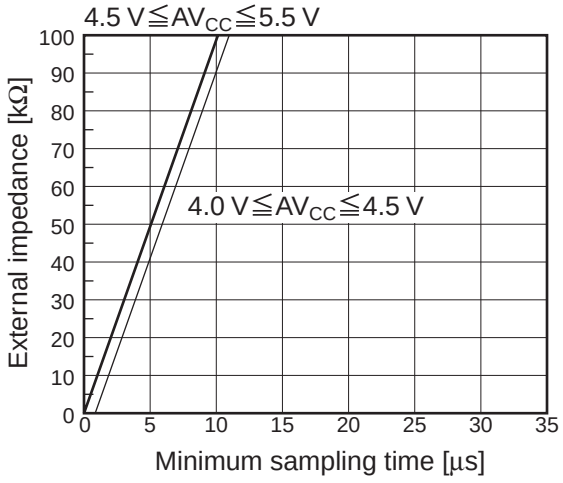


• MASK ROM device

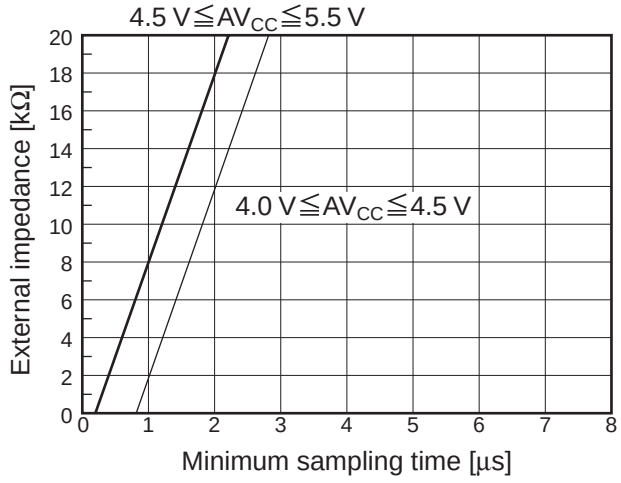
· Relation between External impedance and minimum sampling time

(MB90V340A-101/102/103/104, MB90351A(S), MB90352A(S), MB90351TA(S), MB90352TA(S), MB90356A(S), MB90357A(S), MB90356TA(S), MB90357TA(S))

[External impedance = 0 kΩ to 100 kΩ]



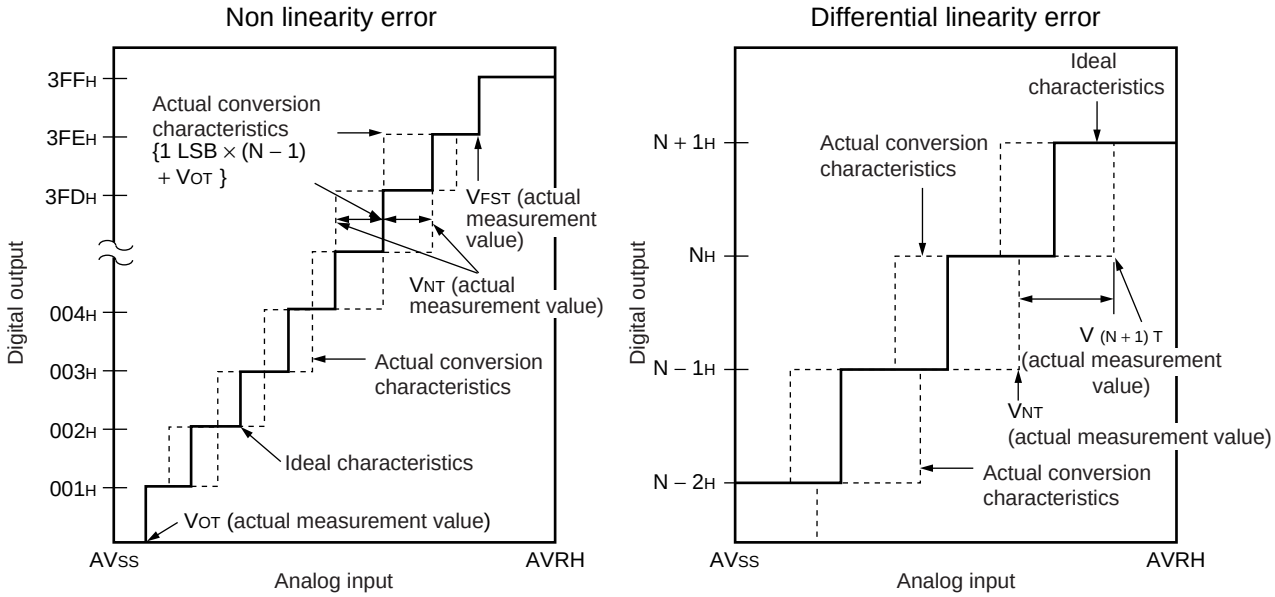
[External impedance = 0 kΩ to 20kΩ]



• **About the error**

Values of relative errors grow larger, as |AVRH – AVSS| becomes smaller.

(Continued)



$$\text{Non linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB [LSB]}$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

N : A/D converter digital output value
V_{OT} : Voltage at which digital output transits from “000_H” to “001_H.”
V_{FST} : Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”