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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 15x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-QFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f352spfm-gse1

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Parameter \ Part Number	MB90F351, MB90F352	MB90F351S, MB90F352S	MB90F351A, MB90F352A	MB90F351TA, MB90F352TA	MB90F351AS, MB90F352AS	MB90F351TAS, MB90F352TAS
16-bit Input Capture	6 channels					
	Retains freerun timer value by (rising edge, falling edge or rising & falling edge), signals an interrupt.					
8/16-bit Programmable Pulse Generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters × 12 8-bit reload registers for L pulse width × 12 8-bit reload registers for H pulse width × 12					
	Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 µs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)					
CAN Interface	1 channel					
	Conforms to CAN Specification Version 2.0 Part A and B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.					
External Interrupt	8 channels					
	Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, extended intelligent I/O services (EI^{2}OS) and DMA.					
D/A converter	—					
I/O Ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)					
Flash Memory	Supports automatic programming, Embedded Algorithm™*2 Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 10 years Boot block configuration Erase can be performed on each block. Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash (MB90F352x only)					
Corresponding EVA name	MB90V340A-102	MB90V340A-101	MB90V340A-102		MB90V340A-101	

*1 : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

*2 : Embedded Algorithm is a trademark of Advanced Micro Devices Inc.

■ PRODUCT LINEUP 2

Parameter \ Part Number	MB90351A, MB90352A	MB90351TA, MB90352TA	MB90351AS, MB90352AS	MB90351TAS, MB90352TAS	MB90V340A-101	MB90V340A-102
CPU	F^2MC-16LX CPU					
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)					
ROM	MASK ROM 64Kbytes : MB90351A(S), MB90351TA(S) 128Kbytes : MB90352A(S), MB90352TA(S)				External	
RAM	4 Kbytes				30 Kbytes	
Emulator-specific power supply*	—				Yes	
Sub clock pin (X0A, X1A) (Max 100 kHz)	Yes		No		No	Yes
Clock monitor function	No					
Low voltage/CPU operation detection reset	No	Yes	No	Yes	No	
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter 4.5 V to 5.5 V : at using external bus				5 V ± 10%	
Operating temperature range	−40 °C to +125 °C				—	
Package	LQFP-64				PGA-299	
UART	2 channels				5 channels	
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device					
I^2C (400 Kbps)	1 channel				2 channels	
A/D Converter	15 channels				24 channels	
	10-bit or 8-bit resolution Conversion time : Min 3 µs includes sample time (per one channel)					
16-bit Reload Timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function.					
16-bit I/O Timer (2 channels)	I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1. I/O Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.				I/O Timer 0 corresponds to ICU 0/1/2/3, OCU 0/1/2/3. I/O Timer 1 corresponds to ICU 4/5/6/7, OCU 4/5/6/7.	
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock frequency)					

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Pin No. LQFP64*	Pin name	Circuit type	Function
24 to 31	P00 to P07	G	General purpose I/O ports. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD00 to AD07		Input/output pins of external address data bus lower 8 bits. This function is enabled when the external bus is enabled.
	INT8 to INT15		External interrupt request input pins for INT8 to INT15
32	P10	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD08		Input/output pin for external bus address data bus bit 8. This function is enabled when external bus is enabled.
	TIN1		Event input pin for reload timer1
33	P11	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD09		Input/output pin for external bus address data bus bit 9. This function is enabled when external bus is enabled.
	TOT1		Output pin for reload timer1
34	P12	N	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD10		Input/output pin for external bus address data bus bit 10. This function is enabled when external bus is enabled.
	SIN3		Serial data input pin for UART3
	INT11R		External interrupt request input pin for INT11
35	P13	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD11		Input/output pin for external bus address data bus bit 11. This function is enabled when external bus is enabled.
	SOT3		Serial data output pin for UART3
36	P14	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD12		Input/output pin for external bus address data bus bit 12. This function is enabled when external bus is enabled.
	SCK3		Clock input/output pin for UART3
37	P15	N	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD13		Input/output pin for external bus address data bus bit 13. This function is enabled when external bus is enabled.
38	P16	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD14		Input/output pin for external bus address data bus bit 14. This function is enabled when external bus is enabled.

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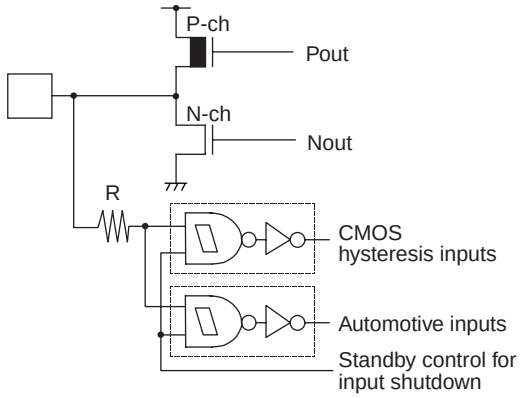
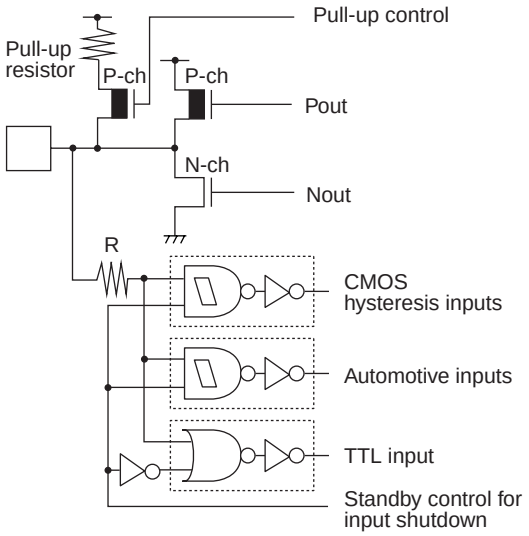
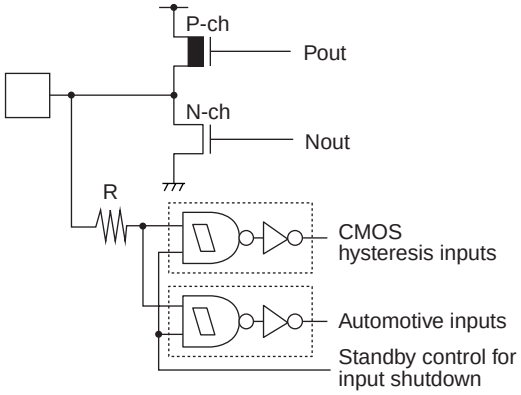
Type	Circuit	Remarks
F		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis inputs (With the stand-by-time input shutdown function) • Automotive input (With the standby-time input shutdown function)
G		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis inputs (With the stand-by-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • TTL input (With the standby-time input shutdown function) • Programmable pull-up resistor: approx. 50 kΩ
H		• CMOS level output (I_{OL} = 3 mA, I_{OH} = –3 mA) • CMOS hysteresis inputs (With the stand-by-time input shutdown function) • Automotive input (With the standby-time input shutdown function)

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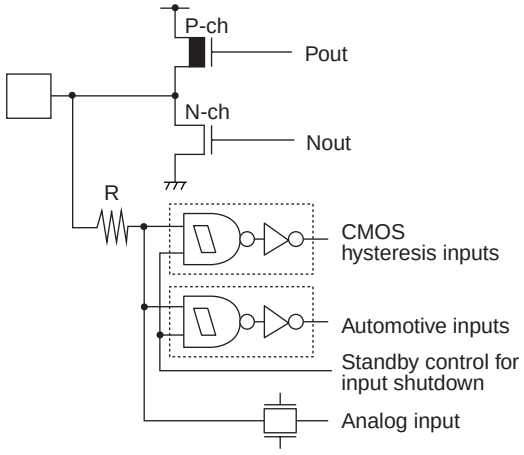
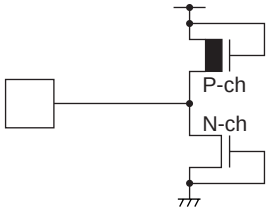
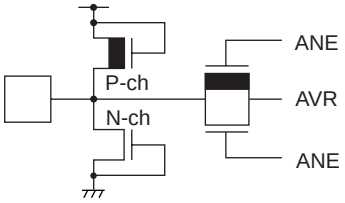
Type	Circuit	Remarks
I		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis inputs (With the stand-by-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • A/D analog input
K		• Power supply input protection circuit
L		• A/D converter reference voltage power supply input pin, with the protection circuit • Flash memory devices do not have a protection circuit against V_{CC} for pin AVRH.

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■ HANDLING DEVICES

Special care is required for the following when handling the device :

- Preventing latch-up
- Treatment of unused pins
- Using external clock
- Precautions for when not using a sub clock signal
- Notes on during operation of PLL clock mode
- Power supply pins (V_{CC}/V_{SS})
- Pull-up/down resistors
- Crystal Oscillator Circuit
- Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs
- Connection of Unused Pins of A/D Converter
- Notes on Energization
- Stabilization of power supply voltage
- Initialization
- Port0 to port3 output during Power-on (External-bus mode)
- Notes on using CAN Function
- Flash security Function
- Correspondence with T_A = + 105 °C or more
- Low voltage/CPU operation detection reset circuit
- Internal CR oscillation circuit

1. Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pin and V_{SS} pin.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

In using the devices, take sufficient care to avoid exceeding maximum ratings.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

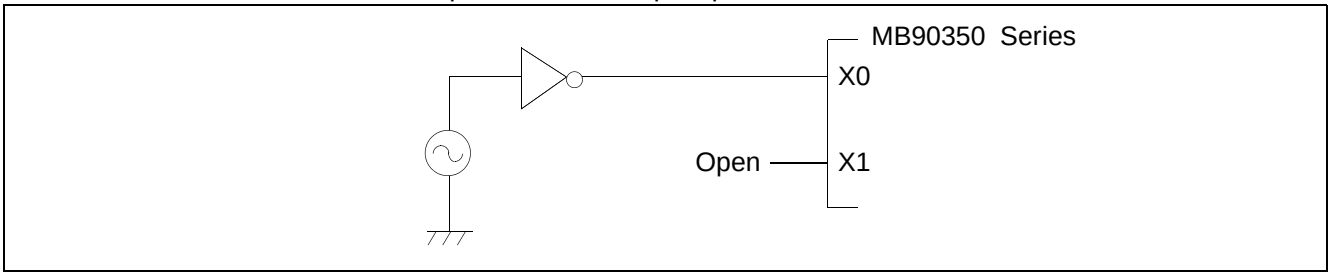
2. Handling unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ .

Unused I/O pins should be set to the output state and can be left open, or the input state with the above described connection.

3. Using external clock

To use external clock, drive the X0 pin and leave X1 pin open.



Address	Register	Abbreviation	Access	Resource name	Initial value
CA$_H$	External Interrupt Enable Register 1	ENIR1	R/W	External Interrupt 1	00000000$_B$
CB$_H$	External Interrupt Source Register 1	EIRR1	R/W		XXXXXXXX$_B$
CC$_H$	External Interrupt Level Register 1	ELVR1	R/W		00000000$_B$
CD$_H$	External Interrupt Level Register 1	ELVR1	R/W		00000000$_B$
CE$_H$	External Interrupt Source Select Register	EISSR	R/W		00000000$_B$
CF$_H$	PLL/Sub clock Control register	PSCCR	W	PLL	XXXX0000$_B$
D0$_H$	DMA Buffer Address Pointer L	BAPL	R/W	DMA	XXXXXXXX$_B$
D1$_H$	DMA Buffer Address Pointer M	BAPM	R/W		XXXXXXXX$_B$
D2$_H$	DMA Buffer Address Pointer H	BAPH	R/W		XXXXXXXX$_B$
D3$_H$	DMA Control Register	DMACS	R/W		XXXXXXXX$_B$
D4$_H$	I/O Register Address Pointer L	IOAL	R/W		XXXXXXXX$_B$
D5$_H$	I/O Register Address Pointer H	IOAH	R/W		XXXXXXXX$_B$
D6$_H$	Data Counter L	DCTL	R/W		XXXXXXXX$_B$
D7$_H$	Data Counter H	DCTH	R/W		XXXXXXXX$_B$
D8$_H$	Serial Mode Register 2	SMR2	W,R/W	UART2	00000000$_B$
D9$_H$	Serial Control Register 2	SCR2	W,R/W		00000000$_B$
DA$_H$	Reception/Transmission Data Register 2	RDR2/ TDR2	R/W		00000000$_B$
DB$_H$	Serial Status Register 2	SSR2	R,R/W		00001000$_B$
DC$_H$	Extended Communication Control Register 2	ECCR2	R,W, R/W		000000XX$_B$
DD$_H$	Extended Status/Control Register 2	ESCR2	R/W		00000100$_B$
DE$_H$	Baud Rate Generator Register 20	BGR20	R/W		00000000$_B$
DF$_H$	Baud Rate Generator Register 21	BGR21	R/W		00000000$_B$
E0$_H$ to EF$_H$	Reserved				
F0$_H$ to FF$_H$	External area				
7900$_H$ to 7907$_H$	Reserved				

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Address	Register	Abbreviation	Access	Resource name	Initial value
7908H	Reload Register L4	PRLL4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXXB
7909H	Reload Register H4	PRLH4	R/W		XXXXXXXXB
790AH	Reload Register L5	PRLL5	R/W		XXXXXXXXB
790BH	Reload Register H5	PRLH5	R/W		XXXXXXXXB
790CH	Reload Register L6	PRLL6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXXB
790DH	Reload Register H6	PRLH6	R/W		XXXXXXXXB
790EH	Reload Register L7	PRLL7	R/W		XXXXXXXXB
790FH	Reload Register H7	PRLH7	R/W		XXXXXXXXB
7910H	Reload Register L8	PRLL8	R/W	16-bit Programmable Pulse Generator 8/9	XXXXXXXXB
7911H	Reload Register H8	PRLH8	R/W		XXXXXXXXB
7912H	Reload Register L9	PRLL9	R/W		XXXXXXXXB
7913H	Reload Register H9	PRLH9	R/W		XXXXXXXXB
7914H	Reload Register LA	PRLLA	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXXB
7915H	Reload Register HA	PRLHA	R/W		XXXXXXXXB
7916H	Reload Register LB	PRLLB	R/W		XXXXXXXXB
7917H	Reload Register HB	PRLHB	R/W		XXXXXXXXB
7918H	Reload Register LC	PRLLC	R/W	16-bit Programmable Pulse Generator C/D	XXXXXXXXB
7919H	Reload Register HC	PRLHC	R/W		XXXXXXXXB
791AH	Reload Register LD	PRLLD	R/W		XXXXXXXXB
791BH	Reload Register HD	PRLHD	R/W		XXXXXXXXB
791CH	Reload Register LE	PRLLE	R/W	16-bit Programmable Pulse Generator E/F	XXXXXXXXB
791DH	Reload Register HE	PRLHE	R/W		XXXXXXXXB
791EH	Reload Register LF	PRLLF	R/W		XXXXXXXXB
791FH	Reload Register HF	PRLHF	R/W		XXXXXXXXB
7920H	Input Capture Register 0	IPCP0	R	Input Capture 0/1	XXXXXXXXB
7921H	Input Capture Register 0	IPCP0	R		XXXXXXXXB
7922H	Input Capture Register 1	IPCP1	R		XXXXXXXXB
7923H	Input Capture Register 1	IPCP1	R		XXXXXXXXB
7924H to 7927H	Reserved				
7928H	Input Capture Register 4	IPCP4	R	Input Capture 4/5	XXXXXXXXB
7929H	Input Capture Register 4	IPCP4	R		XXXXXXXXB
792AH	Input Capture Register 5	IPCP5	R		XXXXXXXXB
792BH	Input Capture Register 5	IPCP5	R		XXXXXXXXB

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Address	Register	Abbreviation	Access	Resource name	Initial value
79C2H	Setting Prohibited				
79C3H to 79DFH	Reserved				
79E0H	Detect Address Setting Register 0	PADR0	R/W	Address Match Detection 0	XXXXXXXXB
79E1H	Detect Address Setting Register 0	PADR0	R/W		XXXXXXXXB
79E2H	Detect Address Setting Register 0	PADR0	R/W		XXXXXXXXB
79E3H	Detect Address Setting Register 1	PADR1	R/W		XXXXXXXXB
79E4H	Detect Address Setting Register 1	PADR1	R/W		XXXXXXXXB
79E5H	Detect Address Setting Register 1	PADR1	R/W		XXXXXXXXB
79E6H	Detect Address Setting Register 2	PADR2	R/W		XXXXXXXXB
79E7H	Detect Address Setting Register 2	PADR2	R/W		XXXXXXXXB
79E8H	Detect Address Setting Register 2	PADR2	R/W		XXXXXXXXB
79E9H to 79EFH	Reserved				
79F0H	Detect Address Setting Register 3	PADR3	R/W	Address Match Detection 1	XXXXXXXXB
79F1H	Detect Address Setting Register 3	PADR3	R/W		XXXXXXXXB
79F2H	Detect Address Setting Register 3	PADR3	R/W		XXXXXXXXB
79F3H	Detect Address Setting Register 4	PADR4	R/W		XXXXXXXXB
79F4H	Detect Address Setting Register 4	PADR4	R/W		XXXXXXXXB
79F5H	Detect Address Setting Register 4	PADR4	R/W		XXXXXXXXB
79F6H	Detect Address Setting Register 5	PADR5	R/W		XXXXXXXXB
79F7H	Detect Address Setting Register 5	PADR5	R/W		XXXXXXXXB
79F8H	Detect Address Setting Register 5	PADR5	R/W		XXXXXXXXB
79F9H to 7BFFH	Reserved				
7C00H to 7CFFH	Reserved for CAN Interface 1. Refer to “■ CAN CONTROLLERS”				
7D00H to 7DFFH	Reserved for CAN Interface 1. Refer to “■ CAN CONTROLLERS”				
7E00H to 7FFFH	Reserved				

Notes :
- Initial value of “X” represents unknown value.
- Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results reading “X”.

(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCLS}	V_{CC}	V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock monitor function, At sub sleep T_A = +25°C	—	60	200	µA	MB90F356A MB90F357A MB90356A MB90357A
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At sub sleep T_A = +25°C	—	60	200	µA	MB90F356AS MB90F357AS MB90356AS MB90357AS
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock monitor function, At sub sleep T_A = +25°C	—	70	150	µA	MB90F351TA MB90F352TA MB90F356TA MB90F357TA MB90351TA MB90352TA MB90356TA MB90357TA
			V_{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock monitor function, At sub sleep T_A = +25°C	—	110	300	µA	MB90F356TA MB90F357TA MB90356TA MB90357TA
			V_{CC} = 5.0 V, Internal CR oscillation/ 4 division, At sub sleep T_A = +25°C	—	110	300	µA	MB90F356TAS MB90F357TAS MB90356TAS MB90357TAS
	I_{CCT}		V_{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock monitor function, At watch mode T_A = +25°C	—	10	35	µA	MB90F351 MB90F352 MB90F351A MB90F352A MB90F356A MB90F357A MB90351A MB90352A MB90356A MB90357A

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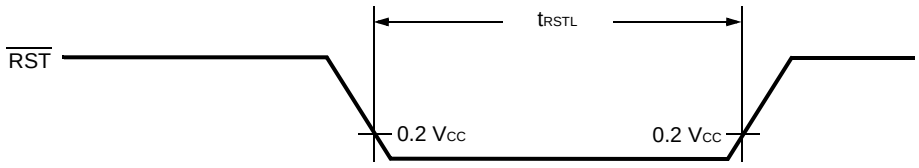
(2) Reset Standby Input

(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

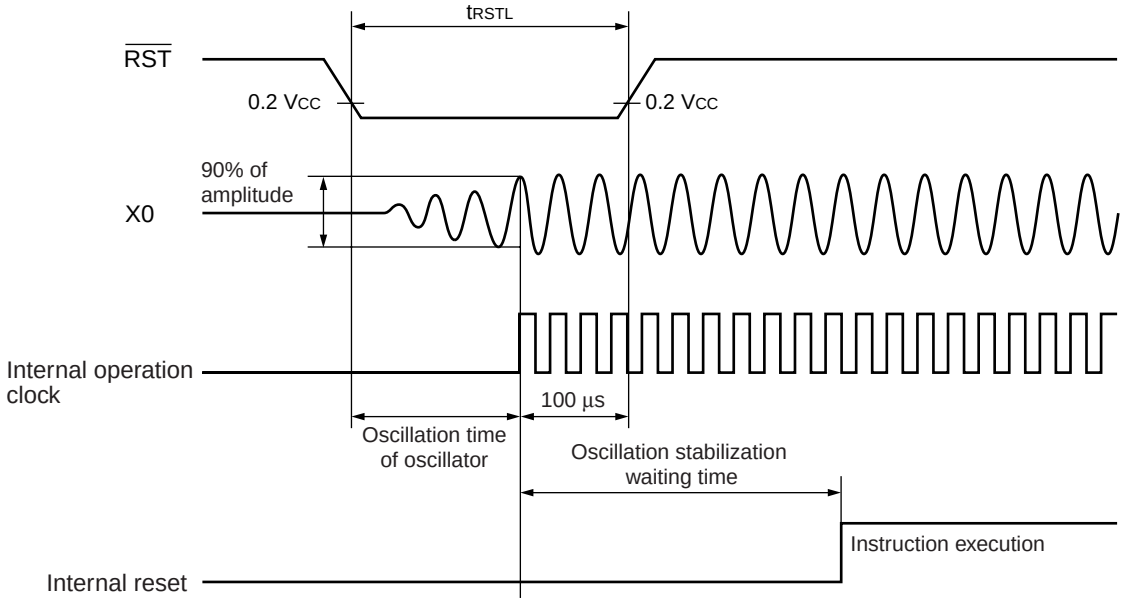
Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	500	—	ns	Under normal operation
			Oscillation time of oscillator* + 100 µs	—	µs	In Stop mode, Sub Clock mode, Sub Sleep mode and Watch mode
			100	—	µs	In Main timer mode and PLL timer mode

* : Oscillation time of oscillator is the time that the amplitude reaches 90%.
In the crystal oscillator, the oscillation time is between several ms to tens of ms. In FAR / ceramic oscillators, the oscillation time is between hundreds of µs to several ms. With an external clock, the oscillation time is 0 ms.

Under normal operation:



In Stop mode, Sub Clock mode, Sub Sleep mode, Watch mode:



(5) Bus Timing (Read)

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 10$	—	ns	
Valid address ⇒ ALE ↓ time	t_{AVLL}	ALE, A21 to A16, AD15 to AD00		$t_{CP}/2 - 20$	—	ns	
ALE ↓ ⇒ Address valid time	t_{LLAX}	ALE, AD15 to AD00		$t_{CP}/2 - 15$	—	ns	
Valid address ⇒ $\overline{RD}$ ↓ time	t_{AVRL}	A21 toA16, AD15 to AD00, $\overline{RD}$		$t_{CP} - 15$	—	ns	
Valid address ⇒ Valid data input	t_{AVDV}	A21 to A16, AD15 to AD00		—	$5\ t_{CP}/2 - 60$	ns	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		$(n^*+3/2)\ t_{CP} - 20$	—	ns	
$\overline{RD}$ ↓ ⇒ Valid data input	t_{RLDV}	$\overline{RD}$, AD15 to AD00		—	$(n^*+3/2)\ t_{CP} - 50$	ns	
$\overline{RD}$ ↑ ⇒ Data hold time	t_{RHDX}	$\overline{RD}$, AD15 to AD00		0	—	ns	
$\overline{RD}$ ↑ ⇒ ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE		$t_{CP}/2 - 15$	—	ns	
$\overline{RD}$ ↑ ⇒ Address valid time	t_{RHAX}	$\overline{RD}$, A21 to A16		$t_{CP}/2 - 10$	—	ns	
Valid address ⇒ CLK ↑ time	t_{AVCH}	A21 to A16, AD15 to AD00, CLK		$t_{CP}/2 - 16$	—	ns	
$\overline{RD}$ ↓ ⇒ CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK		$t_{CP}/2 - 15$	—	ns	
ALE ↓ ⇒ $\overline{RD}$ ↓ time	t_{LLRL}	ALE, $\overline{RD}$		$t_{CP}/2 - 15$	—	ns	

* : n: number of ready cycles

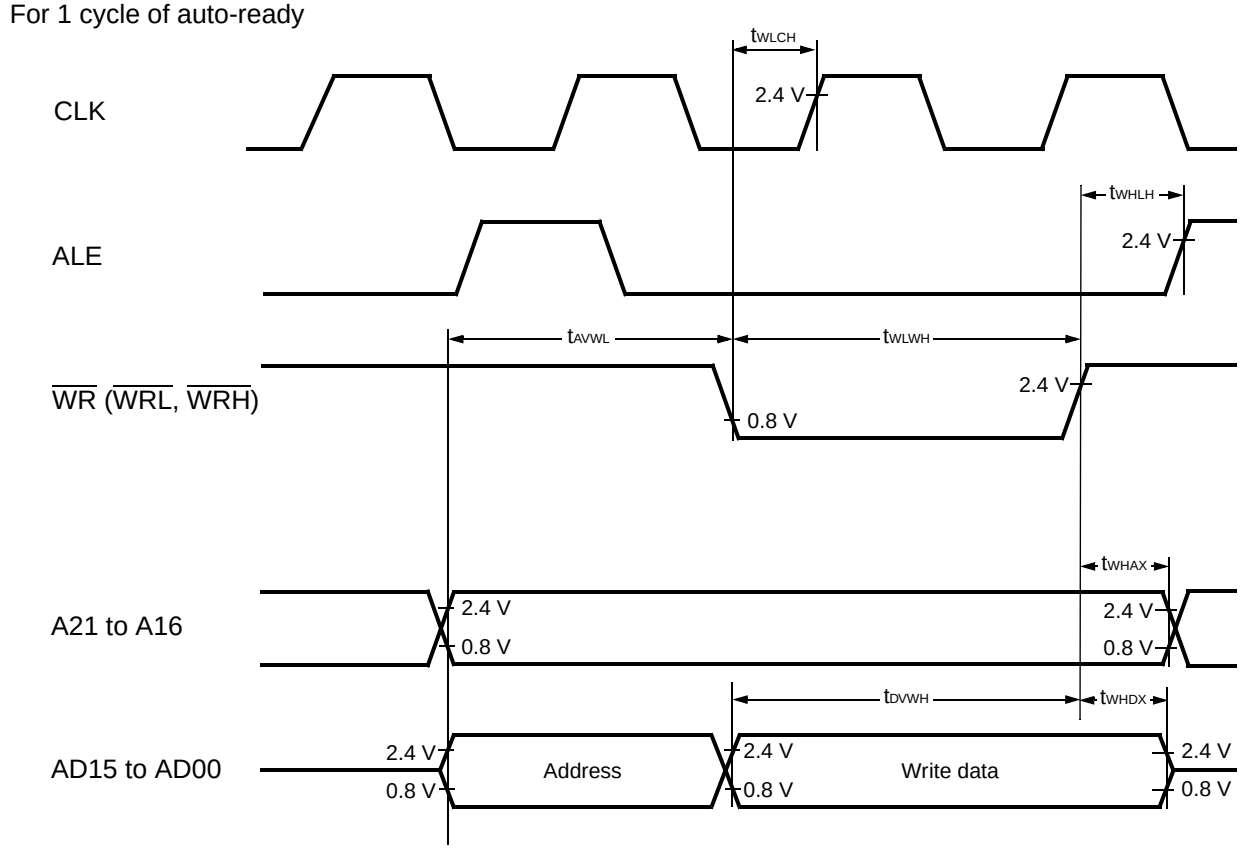
(6) Bus Timing (Write)

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ $\overline{WR}$ ↓ time	t_{AVWL}	A21 to A16, AD15 to AD00, $\overline{WR}$	—	t_{CP}–15	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		(n*+3/2)t_{CP} – 20	—	ns	
Valid data output ⇒ $\overline{WR}$ ↑ time	t_{DVWH}	AD15 to AD00, $\overline{WR}$		(n*+3/2)t_{CP} – 20	—	ns	
$\overline{WR}$ ↑ ⇒ Data hold time	t_{WHDX}	AD15 to AD00, $\overline{WR}$		15	—	ns	
$\overline{WR}$ ↑ ⇒ Address valid time	t_{WHAX}	A21 to A16, $\overline{WR}$		t_{CP}/2 – 10	—	ns	
$\overline{WR}$ ↑ ⇒ ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE		t_{CP}/2 – 15	—	ns	
$\overline{WR}$ ↓ ⇒ CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK		t_{CP}/2 – 15	—	ns	

* : n: Number of ready cycles

For 1 cycle of auto-ready

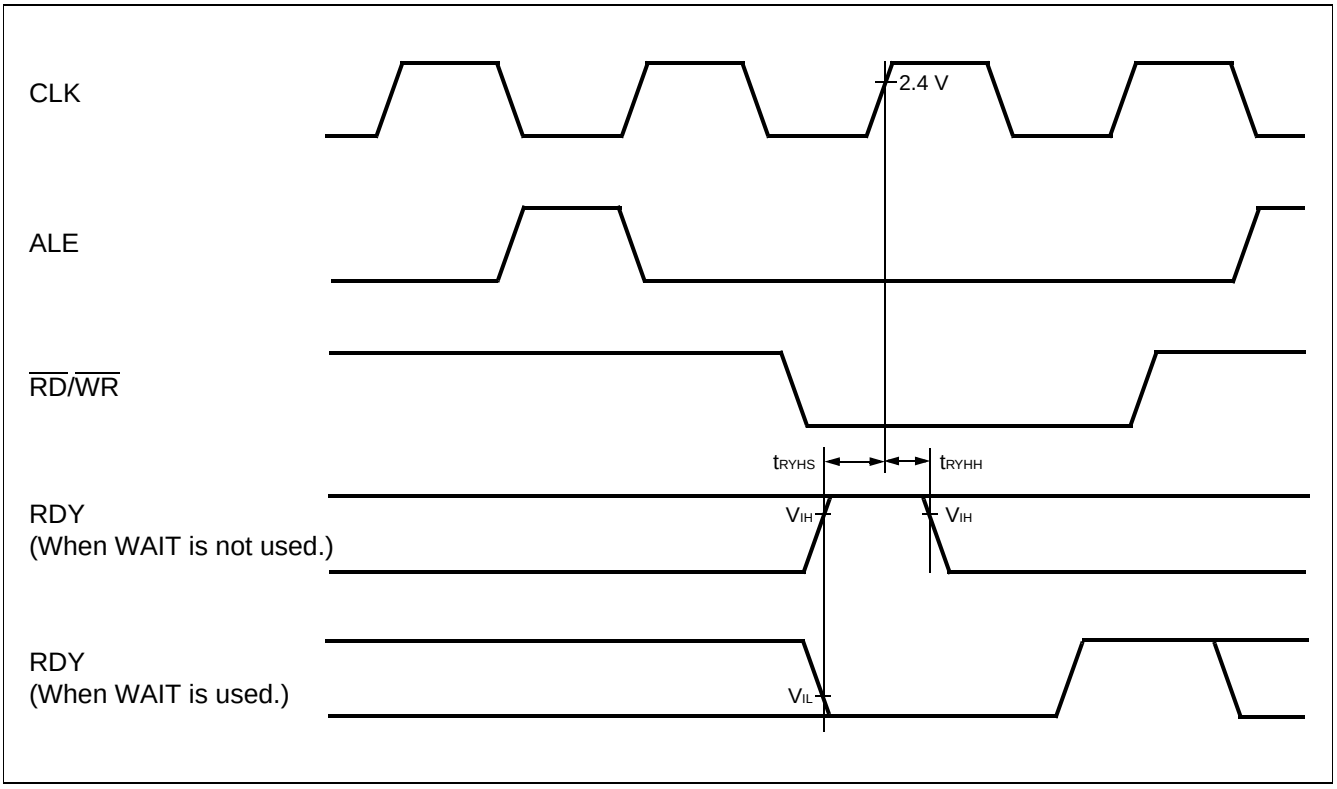


(7) Ready Input Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
RDY set-up time	t_{RYHS}	RDY	—	45	—	ns	f_{CP} = 16 MHz
				32	—	ns	f_{CP} = 24 MHz
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note : If the RDY set-up time is insufficient, use the auto-ready function.



(9) UART 2/3

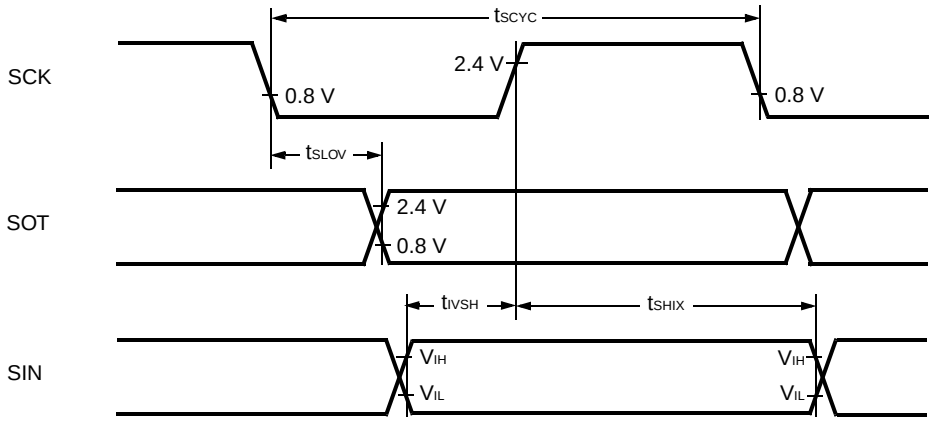
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK2, SCK3	Internal shift clock mode output pins are C_L = 80 pF + 1 TTL	8 t_{CP}*	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK2, SCK3, SOT2, SOT3		–80	+80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK2, SCK3, SIN2, SIN3		100	—	ns	
SCK ↑ → Valid SIN hold time	t_{SHIX}	SCK2, SCK3, SIN2, SIN3		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK2, SCK3	External shift clock mode output pins are C_L = 80 pF + 1 TTL	4 t_{CP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK2, SCK3		4 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK2, SCK3, SOT2, SOT3		—	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK2, SCK3, SIN2, SIN3		60	—	ns	
SCK ↑ → Valid SIN hold time	t_{SHIX}	SCK2, SCK3, SIN2, SIN3		60	—	ns	

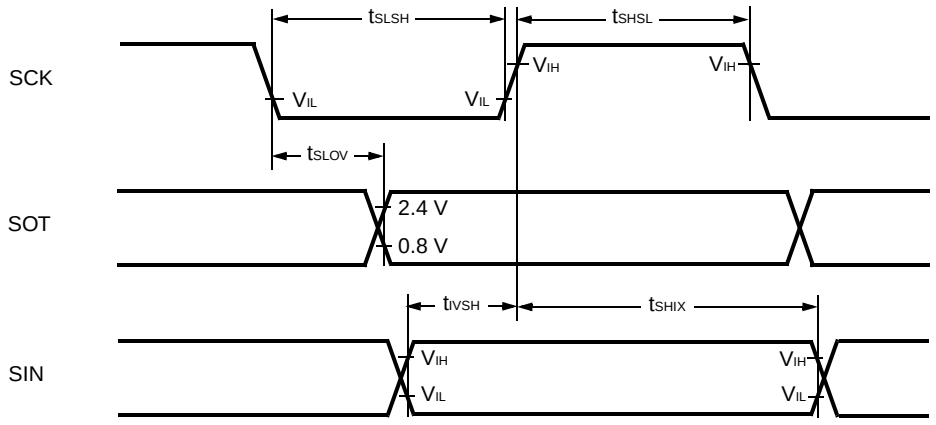
* : Refer to “ (1) Clock timing” rating for t_{CP} (internal operating clock cycle time).

Notes : • AC characteristic in CLK synchronized mode.
• C_L is load capacity value of pins when testing.

• Internal Shift Clock Mode



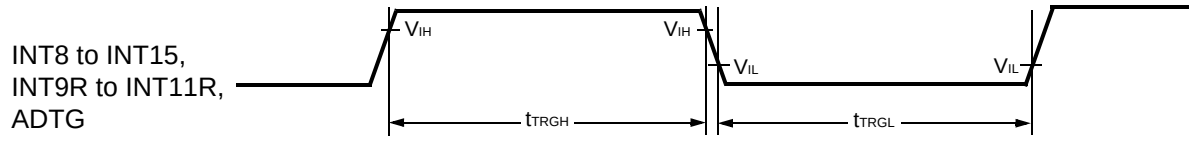
- External Shift Clock Mode



(10) Trigger Input Timing

(MB90F352(S)/MB90F351(S): T_A = –40 °C to +105 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)
(MB90F352(S)/MB90F351(S): T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 16 MHz, V_{SS} = AV_{SS} = 0 V)
(Device other than above: T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INT8 to INT15, INT9R to INT11R, ADTG	—	5 t_{CP}	—	ns	

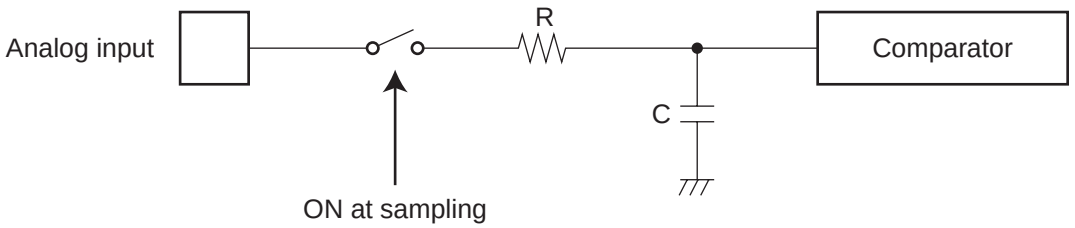


Notes on A/D Converter Section

- **About the external impedance of the analog input and its sampling time**

  A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Also if the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

· Analog input equivalence circuit



MB90F352(S), MB90F351A(S), MB90F352A(S), MB90F351TA(S), MB90F352TA(S), MB90F356A(S), MB90F357A(S), MB90F356TA(S), MB90F357TA(S),

	R	C
$4.5\ V \leqq AV_{CC} \leqq 5.5\ V$	2.0 kΩ (Max)	16.0 pF (Max)
$4.0\ V \leqq AV_{CC} \leqq 4.5\ V$	8.2 kΩ (Max)	16.0 pF (Max)

MB90V340A-101/102/103/104, MB90351A(S), MB90352A(S), MB90351TA(S), MB90352TA(S), MB90356A(S), MB90357A(S), MB90356TA(S), MB90357TA(S),

	R	C
$4.5\ V \leqq AV_{CC} \leqq 5.5\ V$	2.0 kΩ (Max)	14.4 pF (Max)
$4.0\ V \leqq AV_{CC} \leqq 4.5\ V$	8.2 kΩ (Max)	14.4 pF (Max)

Note : The value is reference value.

7. Flash Memory Program/Erase Characteristics

Flash Memory

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = +25 °C V_{CC} = 5.0 V	—	1	15	s	Excludes programming prior to erasure
Chip erase time		—	9	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	16	3,600	µs	Except for the overhead time of the system level
Program/Erase cycle	—	10,000	—	—	cycle	
Flash Memory Data Retention Time	Average T_A = +85 °C	20	—	—	year	*

* : This value comes from the technology qualification.
(Using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C)

Dual Operation Flash Memory

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (4 Kbytes sector)	T_A = +25 °C V_{CC} = 5.0 V	—	0.2	0.5	s	Excludes programming prior to erasure
Sector erase time (16 Kbytes sector)		—	0.5	7.5	s	Excludes programming prior to erasure
Chip erase time		—	4.6	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	64	3,600	µs	Except for the overhead time of the system level
Program/Erase cycle	—	10,000	—	—	cycle	
Flash Memory Data Retention Time	Average T_A = +85 °C	20	—	—	year	*

* : This value comes from the technology qualification.
(Using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C)

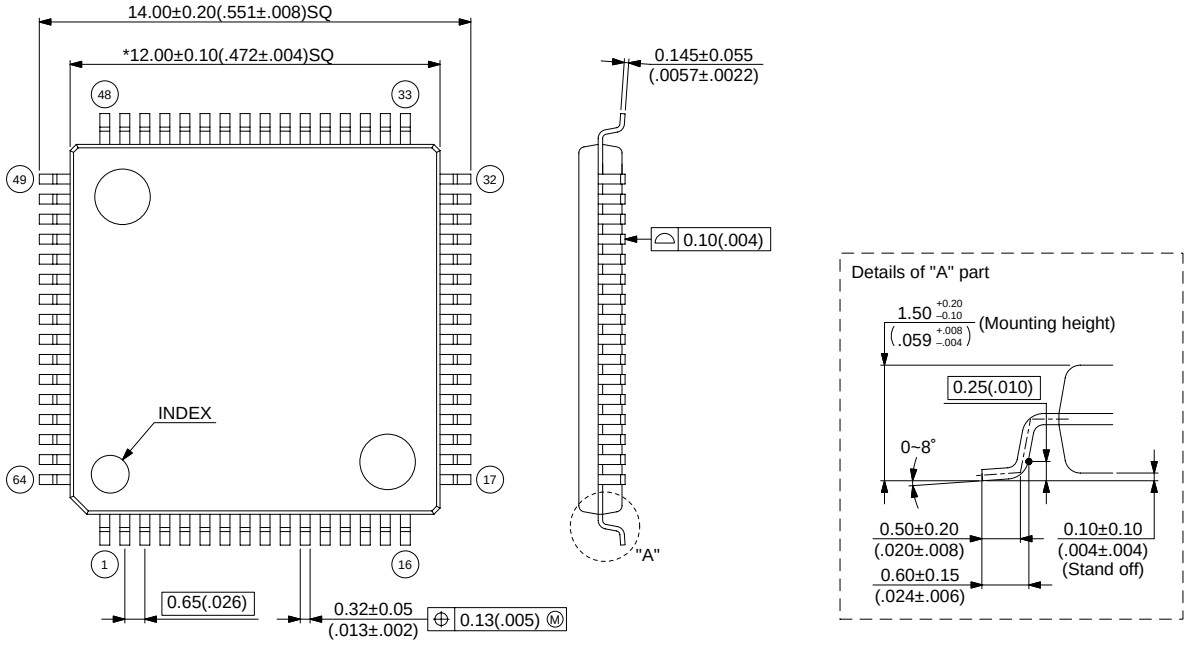
■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F351PFM	64-pin plastic LQFP FPT-64P-M09 12mm □, 0.65mm pitch	Flash memory products (64 Kbytes)
MB90F351SPFM		
MB90F352PFM		Flash memory products (128 Kbytes)
MB90F352SPFM		
MB90F351APMC	64-pin plastic LQFP FPT-64P-M23 12mm □, 0.65mm pitch	Dual operation Flash memory products (64 Kbytes)
MB90F351ASPMC		
MB90F351TAPMC		
MB90F351TASPMC		
MB90F356APMC		
MB90F356ASPMC		
MB90F356TAPMC		
MB90F356TASPMC		
MB90F352APMC	64-pin plastic LQFP FPT-64P-M23 12mm □, 0.65mm pitch	Dual operation Flash memory products (128 Kbytes)
MB90F352ASPMC		
MB90F352TAPMC		
MB90F352TASPMC		
MB90F357APMC		
MB90F357ASPMC		
MB90F357TAPMC		
MB90F357TASPMC		
MB90351APMC	64-pin plastic LQFP FPT-64P-M23 12mm □, 0.65mm pitch	MASK ROM products (64 Kbytes)
MB90351ASPMC		
MB90351TAPMC		
MB90351TASPMC		
MB90356APMC		
MB90356ASPMC		
MB90356TAPMC		
MB90356TASPMC		
MB90352APMC	64-pin plastic LQFP FPT-64P-M23 12mm □, 0.65mm pitch	MASK ROM products (128 Kbytes)
MB90352ASPMC		
MB90352TAPMC		
MB90352TASPMC		
MB90357APMC		
MB90357ASPMC		
MB90357TAPMC		
MB90357TASPMC		

(Continued)

64-pin plastic LQFP
(FPT-64P-M23)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

(Continued)