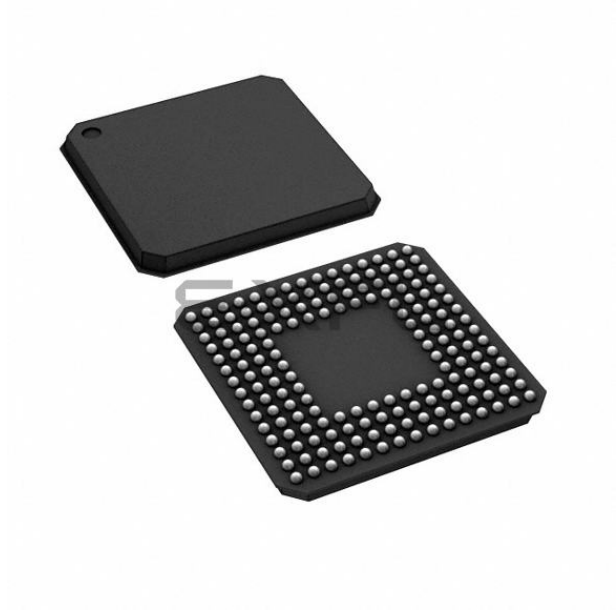

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Application-specific microcontrollers are engineered to

Details	
Product Status	Not For New Designs
Applications	Network Processor
Core Processor	ARM7®
Program Memory Type	External Program Memory
Controller Series	-
RAM Size	External
Interface	EBI/EMI, Ethernet, DMA, SPI, UART
Number of I/O	16
Voltage - Supply	1.4V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	177-LFBGA
Supplier Device Package	177-PFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/digi-international/ns7520b-1-c36

NS7520 Overview

Figure 1 shows the NS7520 modules. Dashed lines indicate shared pins.

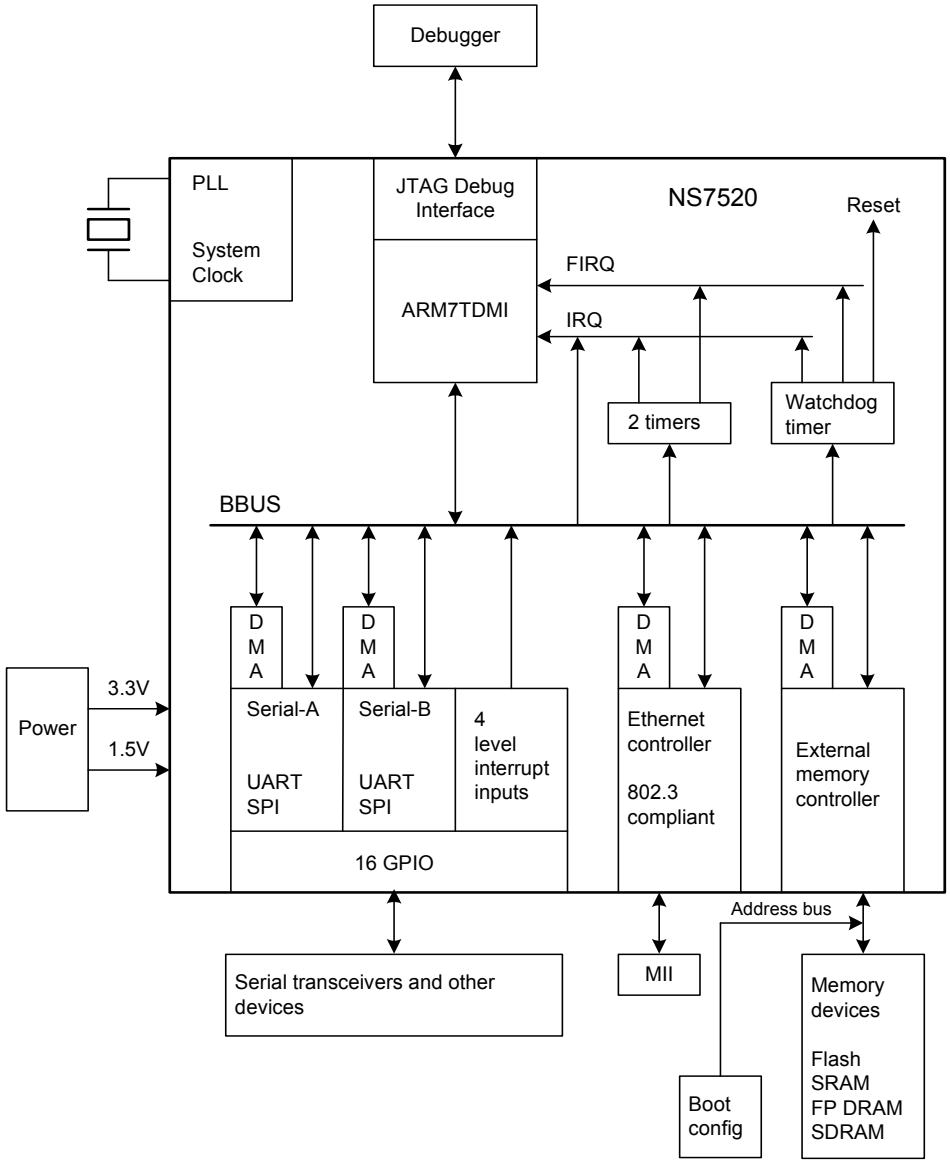


Figure 1: NS7520 module overview

Key Features

This table lists the key features of the NS7520.

CPU core

- ARM7TDMI 32-bit RISC processor
- 32-bit internal bus
- 32-bit ARM and 16-bit Thumb mode
- 15 general purpose 32-bit registers
- 32-bit program counter (PC) and status register
- Five supervisor modes, one user mode

Integrated 10/100 Ethernet MAC

- 10/100 Mbps MII-based PHY interface
- 10 Mbps ENDEC interface
- TP-PMD and fiber-PMD device support
- Full-duplex and half-duplex modes
- Optional 4B/5B coding
- Station, broadcast, and multicast address detection
- 512-byte transmit FIFO, 2 Kbyte receive FIFO
- Intelligent receive-side buffer selection

13-Channel DMA controller

- Two channels dedicated to Ethernet transmit and receive
- Four channels dedicated to two serial modules' transmit and receive
- Four channels for external peripherals. Only two channels — either 3 and 5 or 4 and 6 — can be configured at one time.
- Three channels available for memory-to-memory transfers
- Flexible buffer management

Programmable Timers

- Two independent timers (2µs–20.7 hours)
- Watchdog timer (interrupt or reset on expiration)
- Programmable bus monitor or timer

General purpose I/O pins

- 16 programmable GPIO interface pins
- 4 pins programmable with level-sensitive interrupt

Operating frequency

- 36, 46, or 55 MHz internal clock operation from 18.432 MHz crystal
- f_{MAX} = 36, 46, or 55 (grade–dependent)
- System clock source by external quartz crystal or crystal oscillator, or clock signal
- Programmable PLL, which allows a range of operating frequencies from 10 to f_{MAX}
- Maximum operating frequency from external clock or using PLL multiplication f_{MAX}

177 PFBGA

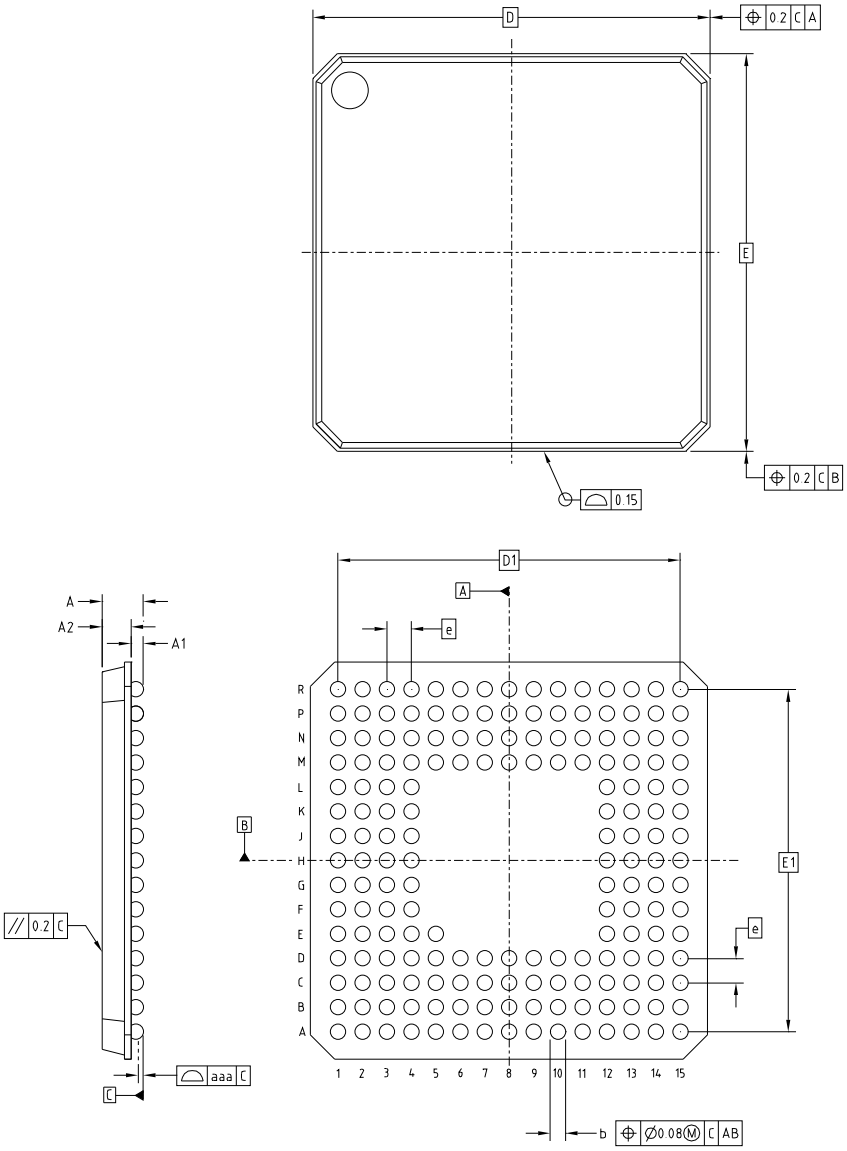


Figure 2: NS7520 pinout and dimensions

Pinout detail tables

Each pinout table applies to a specific interface and contains the following information:

Signal	The pin name for each I/O signal. Some signals have multiple function modes and are identified accordingly. The mode is configured through firmware using one or more configuration registers.
Pin	The pin number assignment for a specific I/O signal. ■ **U** next to the pin number indicates that the pin is a pullup resistor. ■ **D** next to the pin number indicates that the pin is a pulldown resistor. ■ **No value** next to the pin indicates that the pin has neither a pullup nor pulldown resistor. See Figure 5, "Internal pullup characteristics," on page 24 and Figure 6, "Internal pulldown characteristics," on page 25 for an illustration of the characteristics of these pins. Use the figures to select the appropriate value of the complimentary resistor to drive the signal to the opposite logic state. For those pins with no pullup or pulldown resistor, you must select the appropriate value per your design requirements.
_	An underscore (bar) indicates that the pin is *active low*.
I/O	The type of signal — input, output, or input/output.
OD	The output drive strength of an output buffer. The NS7520 uses one of three drivers: ■ 2 mA ■ 4 mA ■ 8 mA

Notes:

- NO CONNECT as a pin description means *do not connect to this pin*.
- The 177th pin (package ball) is for alignment of the package on the PCB.

System Bus interface

Symbol		Pin	I/O	OD	Description	
BCLK		A6	0	8	Synchronous bus clock	
External bus	**Other**				**External bus**	**Other**
ADDR27	CS0OE_	N10 U	I/O	4	Addr bit 27	Logical AND of CS0_ and OE_
ADDR26	CS0WE_	P10 U	I/O	4	Addr bit 26	Logical AND of CS_ and WE_
External bus					**External bus**	
ADDR25		M10 U	I/O	4	Remainder of address bus (through ADDR0)	
ADDR24		R10 U	I/O	4		
ADDR23		N9 U	I/O	4		
ADDR22		R9 U	I/O	4		
ADDR21		M9 U	I/O	4		

GPIO signal	Serial signal	Other signal	Pin	I/O	OD	Serial channel description	Other description
PORTC7	TXDB		G13 U	I/O	2	Channel 2 TXD	GEN interrupt out
PORTC6	DTRB_	DREQ2_	G14 U	I/O	2	Channel 2 DTR_	DMA Channel 4/6 Req
PORTC5	RTSB_	REJECT_	F15 U	I/O	2	Channel 2 RTS_	CAM reject
PORTC4[1]	RXCB/RIB_/ OUT1B_	RESET_	F12 U	I/O	2	Pgm'able Out/ Channel 2 RXCLK/ Channel 2 ring signal/Channel 2 SPI clock (CLK)	RESET output
PORTC3[2]	RXDB	LIRQ3/ DACK2_	F13 U	I/O	2	Channel 2 RXD	Level sensitive IRQ / DMA channel 4/6 ACK
PORTC2[2]	DSRB_	LIRQ2/RPSF_	E15 U	I/O	2	Channel 2 DSR_	Level sensitive IRQ/ CAM request
PORTC1[2]	CTSB_	LIRQ1/ DONE2_(O)	E12 U	I/O	2	Channel 2 CTS_	Level sensitive IRQ / DMA channel 4/6 DONE_Out
PORTC0[2]	TXCB/ OUT2B_/ DCDB_	LIRQ0/ DONE2_(I)	E14 U	I/O	2	Pgm'able Out/ Channel 2 DCD/ Channel 2 SPI enable (SEL_)/ Channel 2 TXCLK	Level sensitive IRQ / DMA channel 4/6 DONE_In

Notes:

1 RESET output indicates the reset state of the NS7520. PORTC4 persists beyond the negation of RESET_ for approximately 512 clock cycles if the PLL is disabled. When the PLL is enabled, PORTC4 persists beyond the negation of RESET_ to allow for PLL lock for 100 microseconds times the ratio of the VCO to XTALA.

This GPIO is left in output mode active following a hardware RESET.

2 PORTC[3:0] pins provide level-sensitive interrupts. The inputs do not need to be synchronous to any clock. The interrupt remains active until cleared by a change in the input signal level.

NS7520 modules

CPU module

The CPU uses an ARM7TDMI core processor. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, which result in high instruction throughput and impressive real-time interrupt response for a small, cost-effective circuit. For more information about ARM7TDMI, see the ARM7TDMI Data Sheet from ARM Ltd. (www.arm.com).

GEN module

The GEN module provides the NS7520 with its main system control functions, as well as these features:

- Two programmable timers with interrupt
- One programmable bus-error timer
- One programmable watchdog timer
- Two 8-bit programmable general-purpose I/O ports

System (SYS) module

The system module provides the system clock (SYS_CLK) and system reset (SYS_RESET) resources.

The system control signals determine the basic operation of the chip:

Signal mnemonic	Signal name	Description
{XTALA1, XTALA2}	Clock source	Operate in one of two ways: ■ The signals are affixed with a 10-20 MHz parallel mode quartz crystal or crystal oscillator and the appropriate components per the component manufacturer. ■ XTALA1 is driven with a clock signal and XTALA2 is left open.
{PLLVDD, PLLVSS}	PLL power	Provide an isolated power supply for the PLL.
RESET_	Chip reset	Active low signal asserted to initiate a hardware reset of the chip.
{TDI, TDO, TNS, TRST_, TCK}	JTAG interface	Provide a JTAG interface for the chip. This interface is used for both boundary scan and ICE control of the internal processor.
{PLLTEST_, BISTEN_, SCANEN_}	Chip mode	Encoded to determine the chip mode.

NS7520 bootstrap initialization

Many internal NS7520 features are configured when the RESET pin is asserted. The address bus configures the appropriate control register bits at powerup. This table shows which bits control which functions:

Address bit	Name	Description
ADDR[27]	Endian configuration	0 Little Endian configuration 1 Big Endian configuration
ADDR[26]	CPU bootstrap	0 CPU disabled; GEN_BUSER=1 1 CPU enabled; GEN_BUSER=0
ADDR[24:23]	CS0/MMCR[19:18] setting	00 8-bit SRAM, 63 wait-states/b00 01 32-bit SRAM, 63 wait-states/b01 10 32-bit SRAM 11 16-bit SRAM, 63 wait-states/b11
ADDR[19:9]	GEN_ID setting	GEN_ID=A[19:09],default='h3ff
ADDR[8:7]	PLL IS setting	IS=A[8:7], default='b10
ADDR[6:5]	PLL FS setting	FS=A[6:5], default='b00
ADDR[4:0]	PLL ND setting	ND=A[4:0], default='b01011

Table 3: NS7520 test modes

JTAG

The NS7520 provides full support for 1149.1 JTAG boundary scan testing. All NS7520 pins can be controlled using the JTAG interface port. The JTAG interface provides access to the ARM7TDMI debug module when the appropriate combination of PLLTST_, BISTEN_, and SCANEN_ is selected (as shown in Table 3: "NS7520 test modes").

ARM Debug

The ARM7TDMI core uses a JTAG TAP controller that shares the pins with the TAP controller used for 1149.1 JTAG boundary scan testing. To enable the ARM7TDMI TAP controller, {PLLTST_,BISTEN_,SCANEN_} must be set as shown in Table 3: "NS7520 test modes".

Sym	Parameter	Conditions	Min	Typ	Max	Unit
I_{IL}	Input current as “0”	No pullup	10		10	µA
I_{OZ}	HighZ leakage current	Any input	-10		10	µA
C_{IO}	Pin capacitance	V_O=0			7	pF

Table 6: Recommended operating temperatures

Absolute maximum ratings

This table defines the maximum values for the voltages that the NS7520 can withstand without being damaged.

Sym	Parameter	Min	Max
V_{DD}	Core supply voltage	-0.3	3.15
V_{CC}	I/O supply voltage	-0.3	3.9
V_{IN}	Input voltage	-0.3	3.9
V_{OUT}	Output voltage	-0.3	3.9

Pad pullup and pulldown characteristics

Figure 5 illustrates characteristics for a pad with internal pullup; Figure 6 illustrates characteristics for a pad with internal pulldown. See "Pinout detail tables," beginning on page 6, for information about which pins use pullup and pulldown resistors.

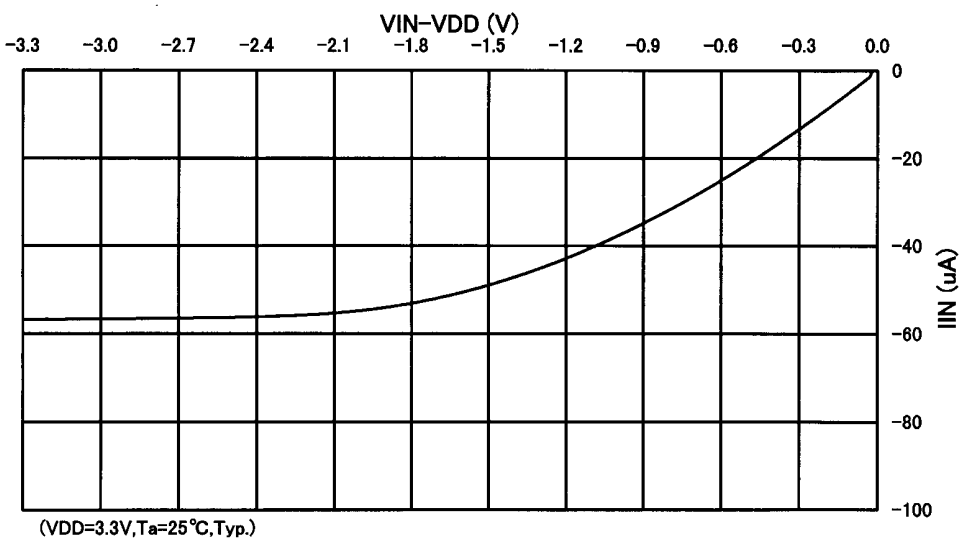
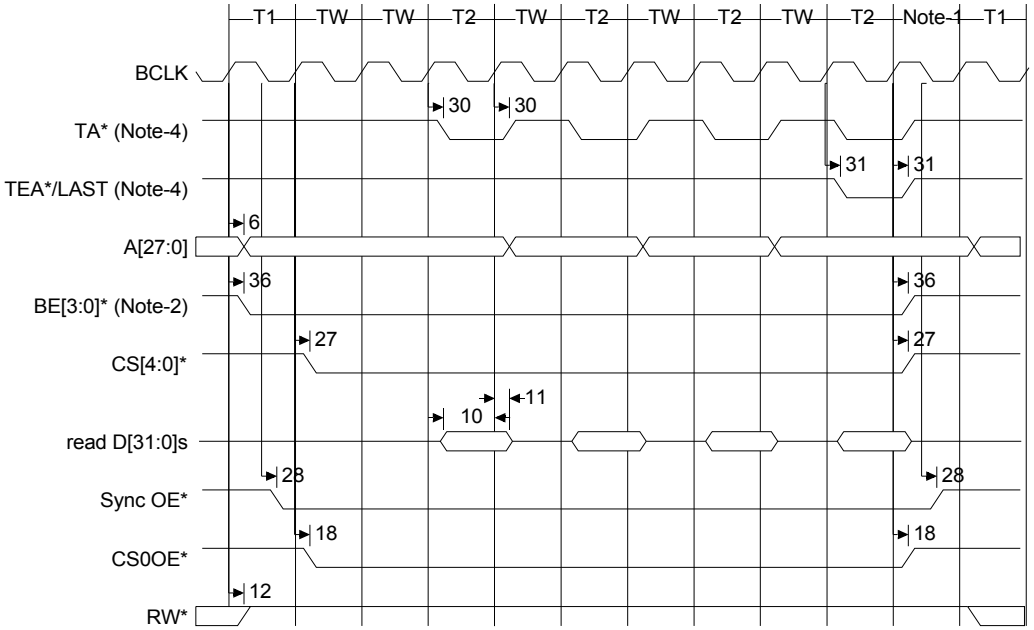


Figure 5: Internal pullup characteristics

SRAM burst read

CS* controlled, four word (4-2-2-2), burst read (wait = 2, BCYC = 01)



Notes:

1 If the next transfer is DMA, null periods between memory transfers can occur. Thirteen clock pulses are required for DMA context switching.

2 Port size determines which byte enable signals are active:

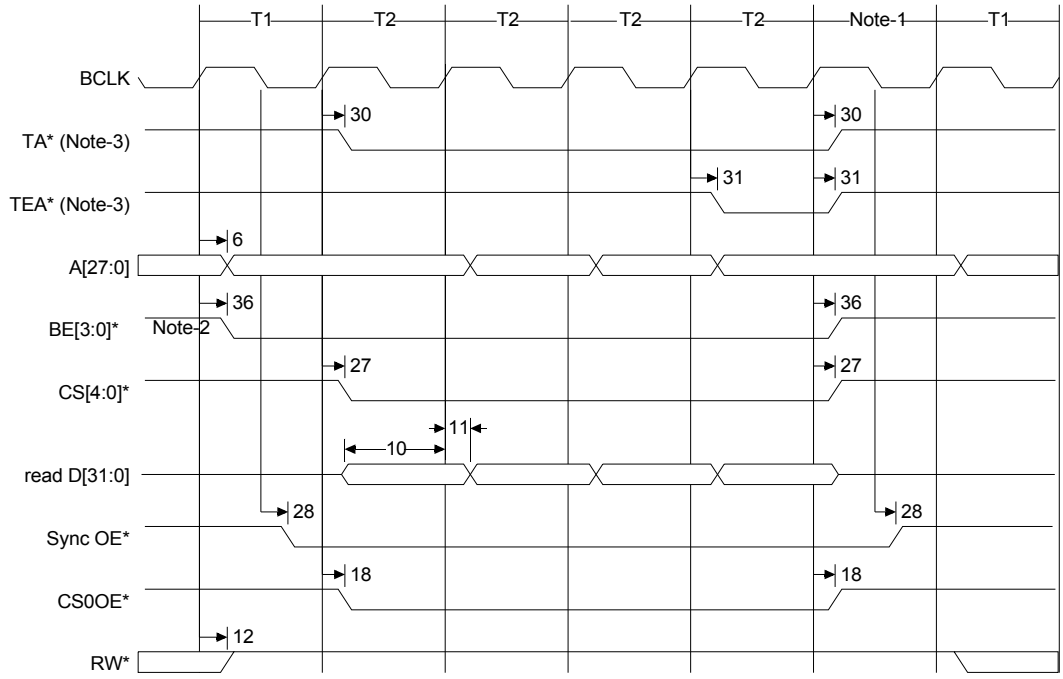
- 8-bit port = BE3*
- 16-bit port = BE[3:0]
- 32-bit port = BE[3:0]

3 The TW cycles are present when the WAIT field is set to 2 or more.

4 The TA* and TEA*/LAST signals are for reference only.

SRAM burst read (2111)

CS* controlled read (wait = 0, BCYC = 00)



Notes:

1 If the next transfer is DMA, null periods between memory transfers can occur. Thirteen clock pulses are required for DMA context switching.

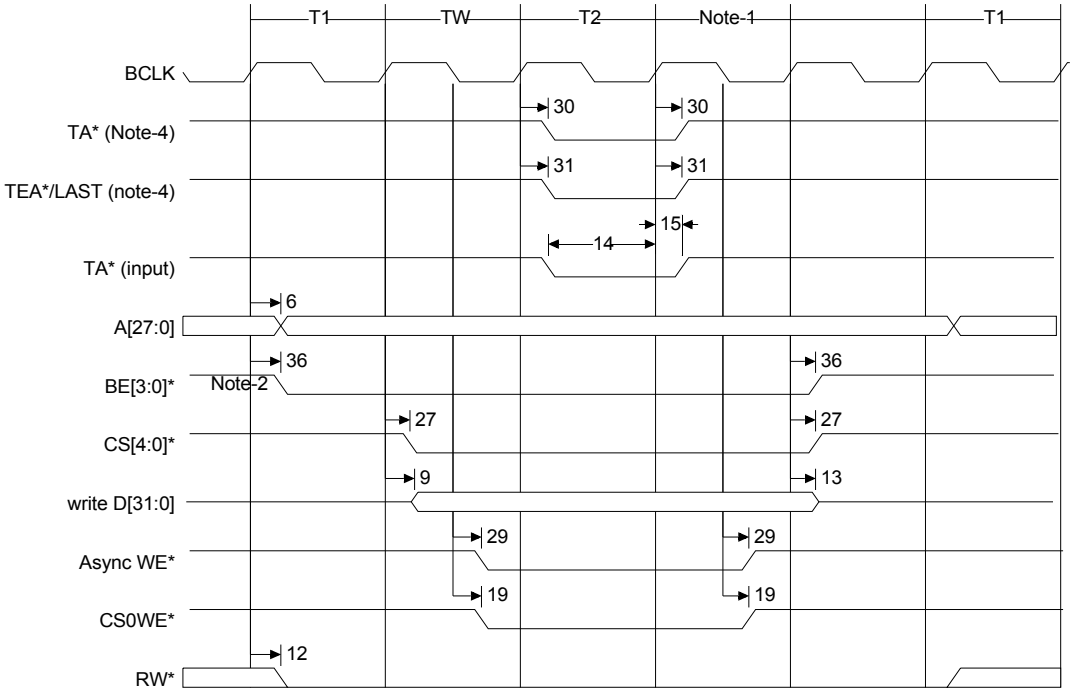
2 Port size determines which byte enable signals are active:

- 8-bit port = BE3*
- 16-bit port = BE[3:0]
- 32-bit port = BE[3:0]

3 The TA* and TEA*/LAST signals are for reference only.

SRAM WE write

WE* controlled write (wait = 2)



Notes:

1 At least one null period occurs between memory transfers. More null periods can occur if the next transfer is DMA. Thirteen clock pulses are required for DMA context switching.

2 Port size determines which byte enable signals are active:

- 8-bit port = BE3*
- 16-bit port = BE[3:0]
- 32-bit port = BE[3:0]

3 The TW cycles are present when the WAIT field is set to 2 or more.

4 The TA* and TEA*/LAST signals are for reference only.

SDRAM timing

BCLK max frequency: 55.296 MHz

Operating conditions:

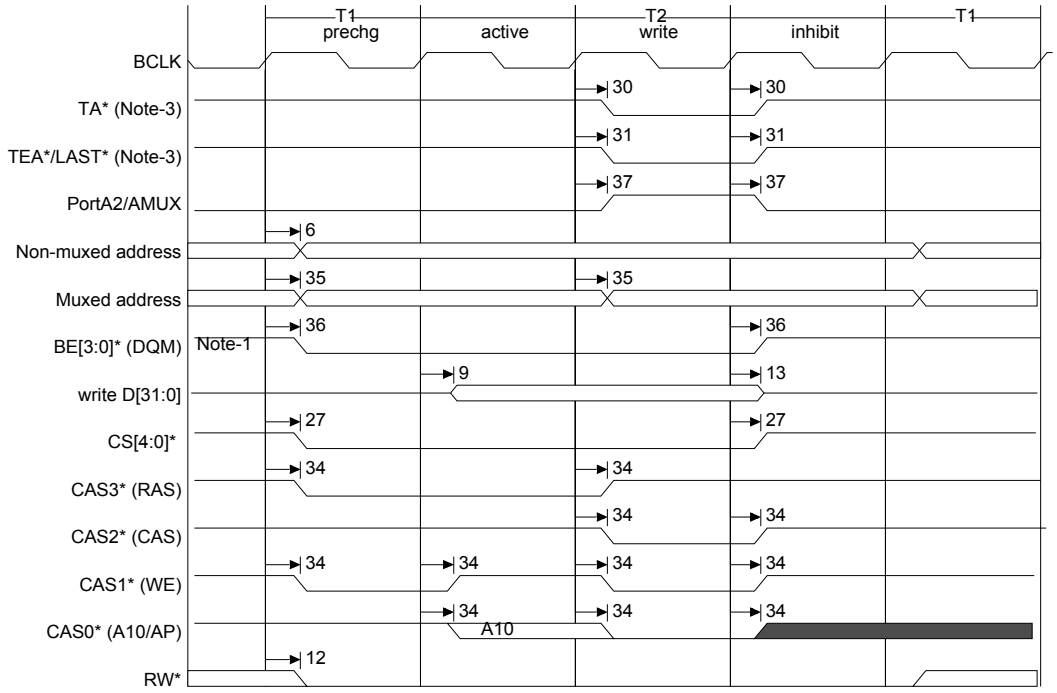
Temperature:	-15.00 (min)	110.00 (max)
Voltage:	1.60 (min)	1.40 (max)
Output load:	25.0pf	
Input drive:	CMOS buffer	

SDRAM timing parameters

Num	Description	Min	Max	Unit
36	BCLK high to BE*/DQM* valid		15.5	ns
6	BCLK high to non-muxed address valid	5	13.5	ns
9	BCLK high to data out valid		14	ns
13	BCLK high to data out high impedance		13	ns
10	Data in valid to BCLK high (setup)	5		ns
11	BCLK high to data in invalid (hold)	3		ns
27	BCLK high to CS* valid		15.5	ns
30	BCLK high to TA* valid		13.5	ns
31	BCLK high to TEA* valid		16	ns
37	BCLK high to PORTA2/AMUX valid		14	ns
35	BCLK high to muxed address valid	6	14.5	ns
34	BCLK high to CAS* valid		12	ns
12	BCLK high to RW* valid		13.5	ns

SDRAM write

SDRAM write



Notes:

1 Port size determines which byte enable signals are active:

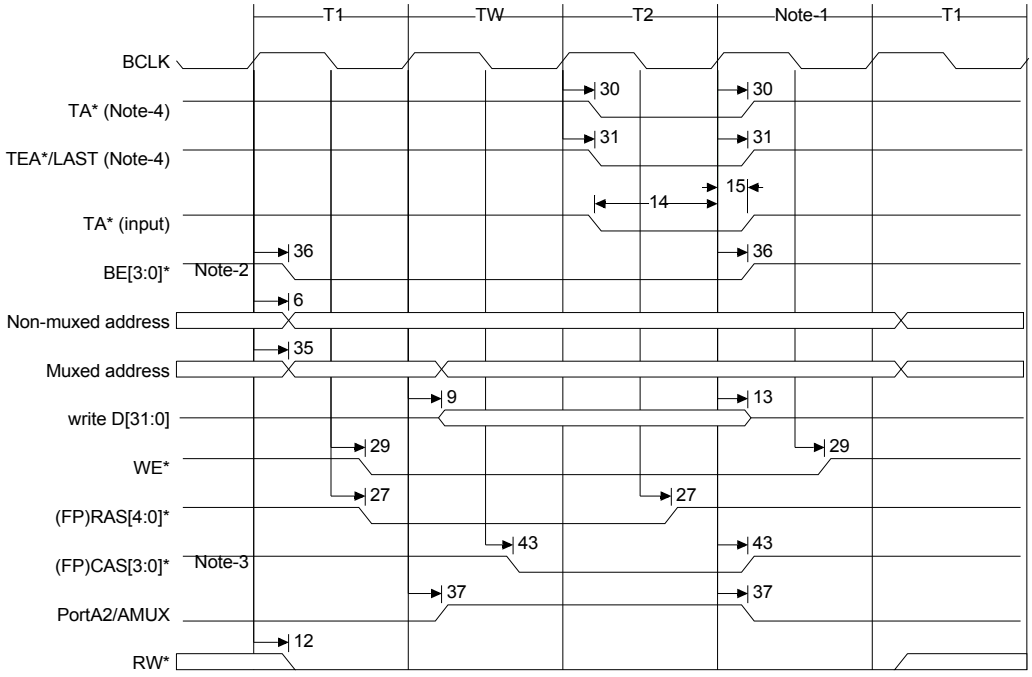
- 8-bit port = BE3*
- 16-bit port = BE[3:2]
- 32-bit port = BE[3:0]

2 The precharge and/or active commands are not always present. These commands depend on the address of the previous SDRAM access.

3 The TA* and TEA*/LAST signals are for reference only.

FP DRAM write

Fast Page write



Notes:

1 If the next transfer is DMA, null periods between memory transfers can occur. Thirteen clock pulses are required for DMA context switching.

2 Port size determines which byte enable signals are active:

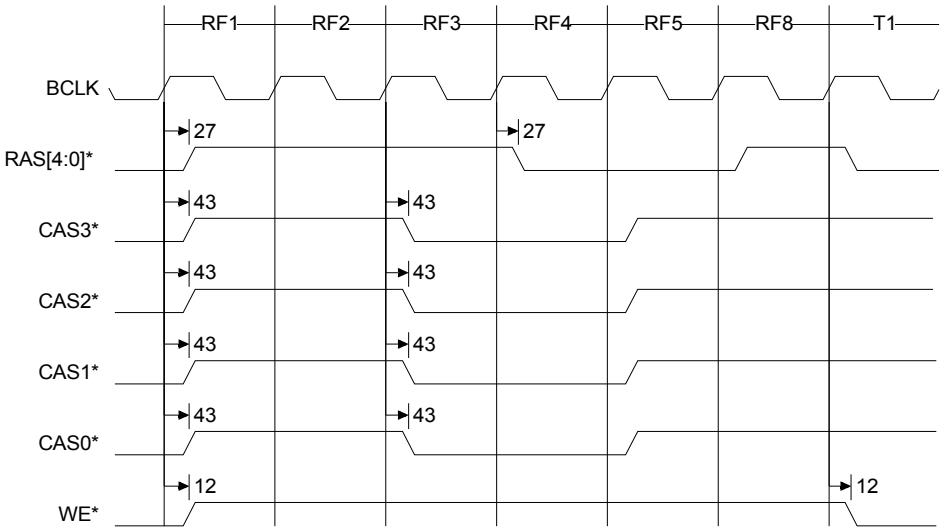
- 8-bit port = BE3*
- 16-bit port = BE[3:2]
- 32-bit port = BE[3:0]

3 Port size determines which CAS signals are active:

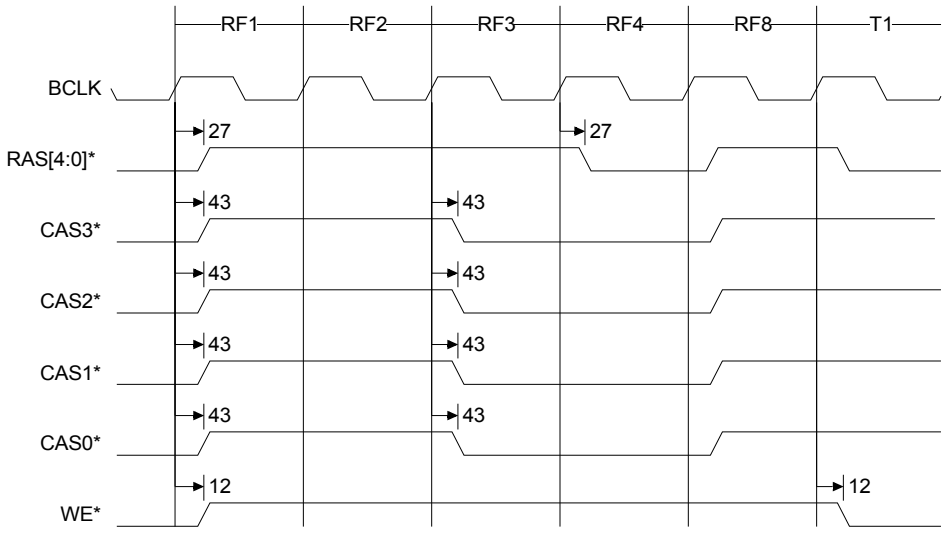
- 8-bit port = CAS3*
- 16-bit port = CAS[3:2]
- 32-bit port = CAS[3:0]

4 The TA* and TEA*/LAST signals are for reference only.

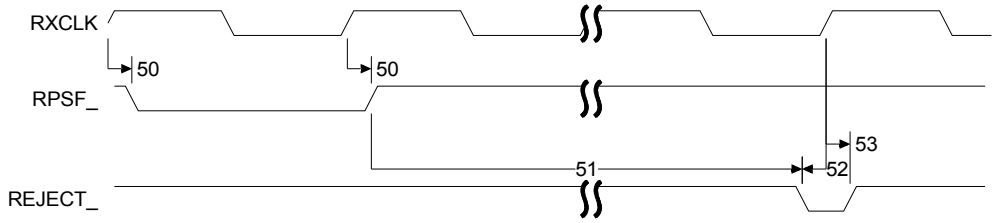
Fast page refresh (RCYC = 10)



Fast page refresh (RCYC = 11)



Ethernet cam timing



JTAG timing

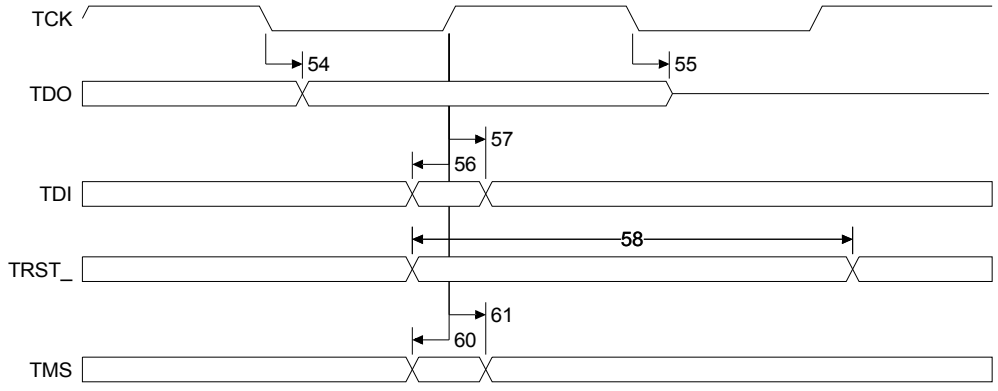
Operating conditions:

Temperature:	-15.00 (min)	110.00 (max)
Voltage:	1.60 (min)	1.40 (max)
Output load:	25.0pf	
Input drive:	CMOS buffer	

jtag arm ice timing parameters

Num	Description	Min	Max	Units
54	TCK to TDO valid		21	ns
55	TCK to TDO HighZ		21	ns
56	TDI setup to TCK rising	1		ns
57	TDI hold from TCK rising	3		ns
58	TRST* width	1		T_{TCK}
60	TMS setup to TCK rising	1		ns
61	TMS hold from TCK rising	3		ns

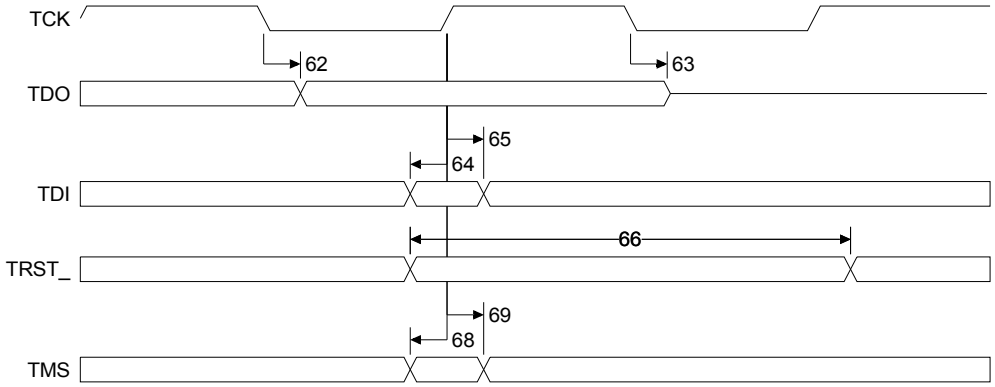
jtag arm ice timing diagram



jtag bscan timing parameters

Num	Description	Min	Max	Units
62	TCK to TDO valid		21	ns
63	TCK to TDO HighZ		21	ns
64	TDI setup to TCK rising	1		ns
65	TDI hold from TCK rising	3		ns
66	TRST* width	1		T_{TCK}
68	TMS setup to TCK rising	1		ns
69	TMS hold to TCK rising	3		ns

jtag bscan timing diagram



External DMA timing

BCLK max frequency: 55.296 MHz

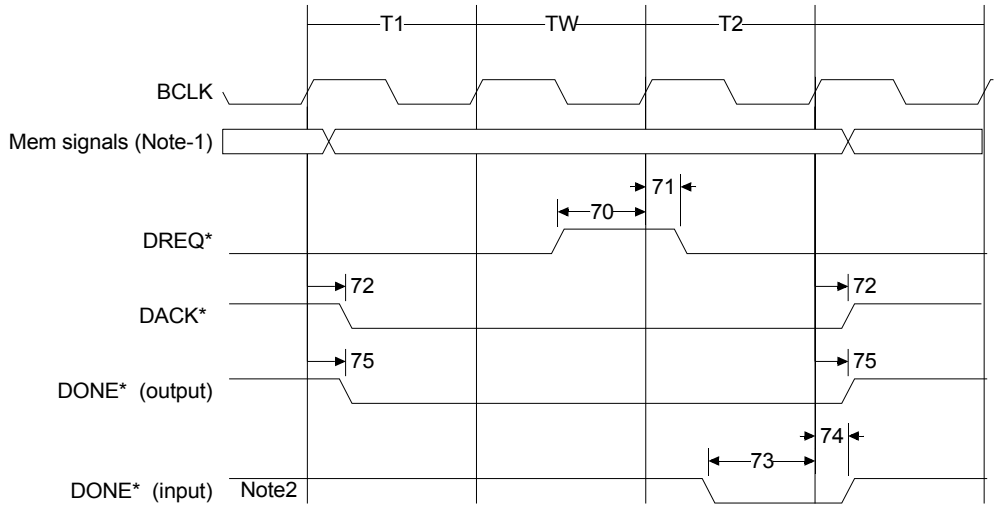
Operating conditions:

Temperature:	-15.00 (min)	110.00 (max)
Voltage:	1.60 (min)	1.40 (max)
Output load:	25.0pf	
Input drive:	CMOS buffer	

External DMA timing parameters

Num	Description	Min	Max	Unit
72	BCLK high to DACK* valid		14	ns
75	BCLK high to DONE* (output) valid		15	ns
70	DREQ* low to BCLK high (setup)	5		ns
71	BCLK high to DREQ* valid (hold)	0		ns
73	DONE* (input) valid BCLK high (setup)	5		ns
74	BLCK high to DONE* (input) valid (hold)	0		ns

Fly-by external DMA

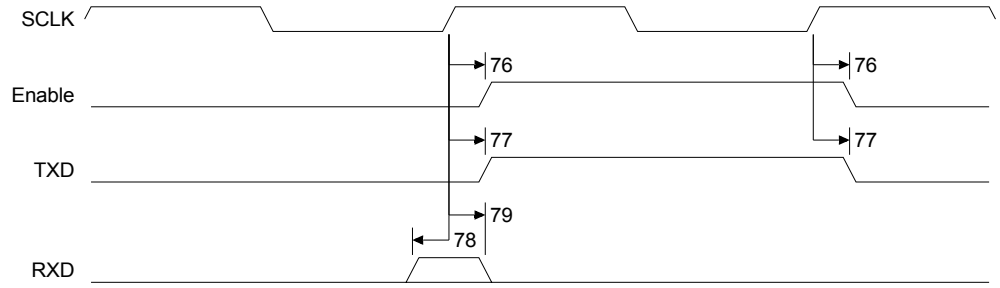


Notes:

1 The memory signals are data[31:0], addr[27:0], BE[3:0], CS/RAS[4:0], CAS[3:0], RW, OE*. WE*, and PORTC3/AMUX. The timing of these signals depends on how the memory is configured (Sync SRAM, Async SRAM, FP DRAM, or SDRAM).

2 The DONE* signal works as an input only when the DMA channel is configured as fly-by write.

synchronous serial internal clock



synchronous serial external clock