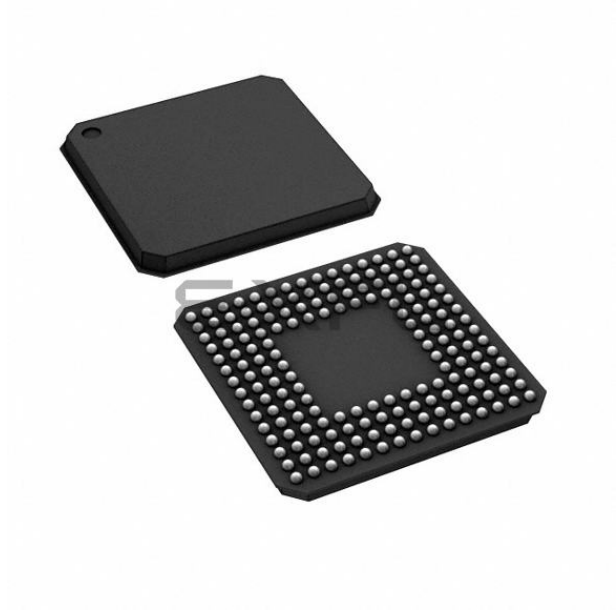

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Application-specific microcontrollers are engineered to

Details	
Product Status	Not For New Designs
Applications	Network Processor
Core Processor	ARM7®
Program Memory Type	External Program Memory
Controller Series	-
RAM Size	External
Interface	EBI/EMI, Ethernet, DMA, SPI, UART
Number of I/O	16
Voltage - Supply	1.4V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	177-LFBGA
Supplier Device Package	177-PFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/digi-international/ns7520b-1-c55

NS7520 Overview

Figure 1 shows the NS7520 modules. Dashed lines indicate shared pins.

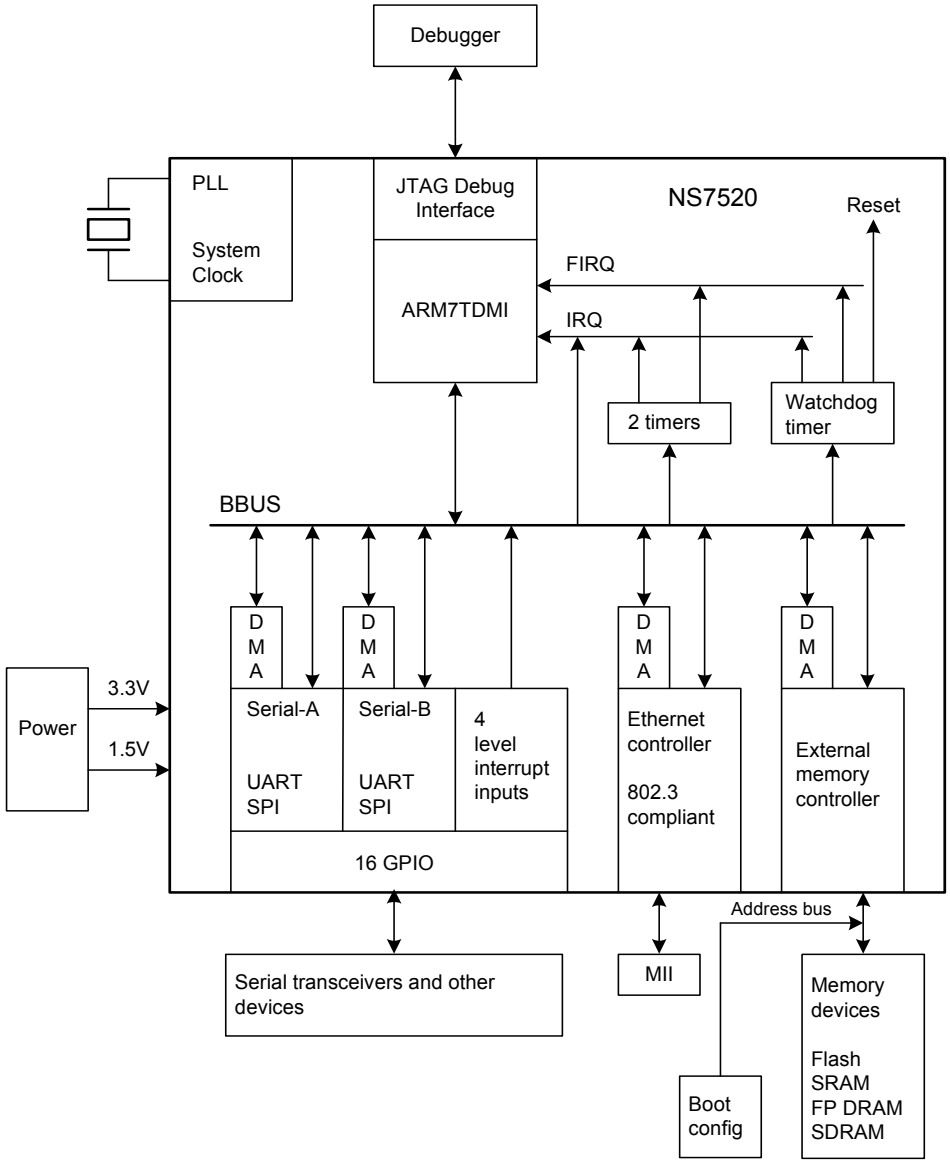


Figure 1: NS7520 module overview

Key Features

This table lists the key features of the NS7520.

CPU core

- ARM7TDMI 32-bit RISC processor
- 32-bit internal bus
- 32-bit ARM and 16-bit Thumb mode
- 15 general purpose 32-bit registers
- 32-bit program counter (PC) and status register
- Five supervisor modes, one user mode

Integrated 10/100 Ethernet MAC

- 10/100 Mbps MII-based PHY interface
- 10 Mbps ENDEC interface
- TP-PMD and fiber-PMD device support
- Full-duplex and half-duplex modes
- Optional 4B/5B coding
- Station, broadcast, and multicast address detection
- 512-byte transmit FIFO, 2 Kbyte receive FIFO
- Intelligent receive-side buffer selection

13-Channel DMA controller

- Two channels dedicated to Ethernet transmit and receive
- Four channels dedicated to two serial modules' transmit and receive
- Four channels for external peripherals. Only two channels — either 3 and 5 or 4 and 6 — can be configured at one time.
- Three channels available for memory-to-memory transfers
- Flexible buffer management

Programmable Timers

- Two independent timers (2µs–20.7 hours)
- Watchdog timer (interrupt or reset on expiration)
- Programmable bus monitor or timer

General purpose I/O pins

- 16 programmable GPIO interface pins
- 4 pins programmable with level-sensitive interrupt

Operating frequency

- 36, 46, or 55 MHz internal clock operation from 18.432 MHz crystal
- f_{MAX} = 36, 46, or 55 (grade–dependent)
- System clock source by external quartz crystal or crystal oscillator, or clock signal
- Programmable PLL, which allows a range of operating frequencies from 10 to f_{MAX}
- Maximum operating frequency from external clock or using PLL multiplication f_{MAX}

Serial ports

- Two fully independent serial ports (UART, SPI)
- Digital phase lock loop (DPLL) for receive clock extractions
- 32-byte transmit/receive FIFOs
- Internal programmable bit-rate generators
- Bit rates 75–230400 in 16X mode
- Bit rates 1200 bps–4 Mbps in 1X mode
- Flexible baud rate generator, external clock for synchronous operation
- Receive-side character and buffer gap timers
- Four receive-side data match detectors

Power and Operating Voltages

- 500 mW maximum at 55 MHz (all outputs switching)
- 418 mW maximum at 46 MHz (all outputs switching)
- 291 mW maximum at 36 MHz (all outputs switching)
- 3.3 V — I/O
- 1.5 V — Core

Bus interface

- Five independent programmable chip selects with 256 Mb addressing per chip select
- Chip select support for SRAM, FP/EDO DRAM, SDRAM, Flash, and EEPROM without external glue
- 8-, 16-, and 32-bit peripheral support
- External address decoding and cycle termination
- Dynamic bus sizing
- Internal DRAM/SDRAM controller with address multiplexer and programmable refresh frequency
- Internal refresh controller (CAS before RAS)
- Burst-mode support
- 0–63 wait states per chip select
- Address pins that configurem chip operating modes (see "NS7520 bootstrap initialization" on page 22)

Operating frequency

The NS7520 is available in grades operating at three maximum operating frequencies: 36 MHz, 46 MHz, and 55 MHz. The operating frequency is set during bootstrap initialization, using pins A[8:0]. These address pins load the PLL Settings register on powerup reset. A[8:7] determines IS (charge pump current); A[6:5] determines FS (output divider), and A[4:0] defines ND (PLL multiplier). Each bit in A[8:0] can be set individually. See the discussion of the PLL Settings register in the *NS7520 Hardware Reference* for more information.

Pinout detail tables

Each pinout table applies to a specific interface and contains the following information:

Signal	The pin name for each I/O signal. Some signals have multiple function modes and are identified accordingly. The mode is configured through firmware using one or more configuration registers.
Pin	The pin number assignment for a specific I/O signal. ■ **U** next to the pin number indicates that the pin is a pullup resistor. ■ **D** next to the pin number indicates that the pin is a pulldown resistor. ■ **No value** next to the pin indicates that the pin has neither a pullup nor pulldown resistor. See Figure 5, "Internal pullup characteristics," on page 24 and Figure 6, "Internal pulldown characteristics," on page 25 for an illustration of the characteristics of these pins. Use the figures to select the appropriate value of the complimentary resistor to drive the signal to the opposite logic state. For those pins with no pullup or pulldown resistor, you must select the appropriate value per your design requirements.
_	An underscore (bar) indicates that the pin is *active low*.
I/O	The type of signal — input, output, or input/output.
OD	The output drive strength of an output buffer. The NS7520 uses one of three drivers: ■ 2 mA ■ 4 mA ■ 8 mA

Notes:

- NO CONNECT as a pin description means *do not connect to this pin*.
- The 177th pin (package ball) is for alignment of the package on the PCB.

System Bus interface

Symbol		Pin	I/O	OD	Description	
BCLK		A6	0	8	Synchronous bus clock	
External bus	**Other**				**External bus**	**Other**
ADDR27	CS0OE_	N10 U	I/O	4	Addr bit 27	Logical AND of CS0_ and OE_
ADDR26	CS0WE_	P10 U	I/O	4	Addr bit 26	Logical AND of CS_ and WE_
External bus					**External bus**	
ADDR25		M10 U	I/O	4	Remainder of address bus (through ADDR0)	
ADDR24		R10 U	I/O	4		
ADDR23		N9 U	I/O	4		
ADDR22		R9 U	I/O	4		
ADDR21		M9 U	I/O	4		

Symbol	Pin	I/O	OD	Description
ADDR20	N8 U	I/O	4	
ADDR19	P8 U	I/O	4	
ADDR18	M7 U	I/O	4	
ADDR17	R7 U	I/O	4	
ADDR16	N7 U	I/O	4	
ADDR15	R6 U	I/O	4	
ADDR14	M6 U	I/O	4	
ADDR13	P6 U	I/O	4	
ADDR12	N6 U	I/O	4	
ADDR11	M5 U	I/O	4	
ADDR10	P5 U	I/O	4	
ADDR9	N5 U	I/O	4	
ADDR8	R4 U	I/O	4	
ADDR7	R3 U	I/O	4	
ADDR6	R2 U	I/O	4	
ADDR5	M4 U	I/O	4	
ADDR4	N4 U	I/O	4	
ADDR3	R1 U	I/O	4	
ADDR2	M3 U	I/O	4	
ADDR1	N2 U	I/O	4	
ADDR0	P1 U	I/O	4	
DATA31	N1	I/O	4	Data bus
DATA30	M1	I/O	4	
DATA29	L3	I/O	4	
DATA28	L2	I/O	4	
DATA27	L4	I/O	4	
DATA26	L1	I/O	4	
DATA25	K3	I/O	4	
DATA24	K2	I/O	4	
DATA23	K1	I/O	4	
DATA22	J2	I/O	4	
DATA21	J3	I/O	4	
DATA20	J1	I/O	4	

Symbol	Pin	I/O	OD	Description
RW_	D6	I/O	2	Transfer direction
BR_	D7	NO CONNECT		
BG_	C7	NO CONNECT		
BUSY_	B7	NO CONNECT		

System bus interface signal descriptions

Mnemonic	Signal	Description
BCLK	Bus clock	Provides the bus clock. All system bus interface signals are referenced to the BCLK signal.
ADDR[27:0]	Address bus	Identifies the address of the peripheral being addressed by the current bus master. The address bus is bi-directional.
DATA[31:0]	Data bus	Provides the data transfer path between the NS7520 and external peripheral devices. The data bus is bi-directional. **Recommendation:** Less than x32 (S)DRAM/SRAM memory configurations. Unconnected data bus pins will float during memory read cycles. Floating inputs can be a source of wasted power. For other than x32 DRAM/SRAM configurations, the unused data bus signals should be pulled up.
TS_	Transfer start	NO CONNECT
BE_	Byte enable	Identifies which 8-bit bytes of the 32-bit data bus are active during any given system bus memory cycle. The BE_ signals are active low and bi-directional.
TA_	Transfer acknowledge	Indicates the end of the current system bus memory cycle. This signal is driven to 1 prior to tri-stating its driver. TA_ is bi-directional.
TEA_	Transfer error acknowledge	Indicates an error termination or burst cycle termination: ■ In conjunction with TA_ to signal the end of a burst cycle. ■ Independently of TA_ to signal that an error occurred during the current bus cycle. TEA_ terminates the current burst cycle. This signal is driven to 1 prior to tri-stating its driver. TEA_ is bi-directional. The NS7520 or the external peripheral can drive this signal.
RW_	Read/write indicator	Indicates the direction of the system bus memory cycle. RW_ high indicates a read operation; RW_ low indicates a write operation. The RW_ signal is bi-directional.
BR_	Bus request	NO CONNECT
BG_	Bus grant	NO CONNECT
BUSY_	Bus busy	NO CONNECT

Chip select controller

The NS7520 supports five unique chip select configurations.

Symbol	Pin	I/O	OD	Description
CS4_	B4	O	4	Chip select/DRAM RAS_
CS3_	A4	O	4	Chip select/DRAM RAS_
CS2_	C5	O	4	Chip select/DRAM RAS_
CS1_	B5	O	4	Chip select/DRAM RAS_
CS0_	D5	O	4	Chip select (boot select)
CAS3_	A1	O	4	FP/EDO DRAM column strobe D31:D24/SDRAM RAS_
CAS2_	C4	O	4	FP/EDO DRAM column strobe D23:D16/SDRAM CAS_
CAS1_	B3	O	4	FP/EDO DRAM column strobe D15:D08/SDRAM WE_
CAS0_	A2	O	4	FP/EDO DRAM column strobe D07:D00/SDRAM A10(AP)
WE_	C6	O	4	Write enable for NCC Ctrl'd cycles
OE_	B6	O	4	Output enable for NCC Ctrl'd cycles

Chip select controller signal descriptions

Mnemonic	Signal	Description
CS0_ CS1_ CS2_ CS3_ CS4_	Chip select 0 Chip select 1 Chip select 2 Chip select 3 Chip select 4	Unique chip select outputs supported by the NS7520. Each chip select can be configured to decode a portion of the available address space and can address a maximum of 256 Mbytes of address space. The chip selects are configured using registers in the memory module. A chip select signal is driven low to indicate the end of the current memory cycle. For FP/EDO DRAM, these signals provide the RAS signal.
CAS0_ CAS1_ CAS2_ CAS3_	Column address strobe signals	Activated when an address is decoded by a chip select module configured for DRAM mode. The CAS_ signals are active low and provide the column address strobe function for DRAM devices. The CAS_ signals also identify which 8-bit bytes of the 32-bit data bus are active during any given system bus memory cycle. For SDRAM, CAS[3:1]_ provides the SDRAM command field. CAS0_ provides the auto-precharge signal. For non-DRAM settings, these signals are 1.
WE_	Write enable	Active low signal that indicates that a memory write cycle is in progress. This signal is activated only during write cycles to peripherals controlled by one of the chip selects in the memory module.
OE_	Output enable	Active low signal that indicates that a memory read cycle is in progress. This signal is activated only during read cycles from peripherals controlled by one of the chip selects in the memory module.

"No connect" pins

Pin	Description
R13	Add a 15K ohm pulldown to GND (15K ohm is the recommended value; 10–20K ohms is acceptable)
P12	Add a 15K ohm pulldown to GND (15K ohm is the recommended value; 10–20K ohms is acceptable)
N12	Tie to GND
R15	XTALB2: NO CONNECT
M11	NO CONNECT
P11	NO CONNECT
N11	NO CONNECT
R12	NO CONNECT
R14	NO CONNECT
P13	NO CONNECT

Note: If your design implements 10-2-K ohm *pullups* instead of *pulldowns* on R13 and P12, and a pullup on N12 instead of *GND*, no action is required.

General Purpose I/O

GPIO signal	Serial signal	Other signal	Pin	I/O	OD	Serial channel description	Other description
PORTA7	TXDA		J14 U	I/O	2	Channel 1 TXD	
PORTA6	DTRA_	DREQ1_	J13 U	I/O	2	Channel 1 DTR_	DMA channel 3/5 Req
PORTA5	RTSA_		J15 U	I/O	2	Channel 1 RTS_	
PORTA4	RXCA/RIA_/ OUT1A_		J12 U	I/O	2	Pgm'able Out/ Channel 1 RXCLK/ Channel 1 ring signal/Channel 1 SPI clock (CLK)	
PORTA3	RXDA	DACK1_	H15 U	I/O	2	Channel 1 RXD	DMA channel 3/5 ACK
PORTA2	DSRA_	AMUX	H12 U	I/O	2	Channel 1 DSR_	DRAM addr mux
PORTA1	CTSA_	DONE1_ (O)	H13 U	I/O	2	Channel 1 CTS_	DMA channel 3/5 DONE_Out
PORTA0	TXCA/ OUT2A_/ DCDA_	DONE1_ (I)	G12 U	I/O	2	Pgm'able Out/ Channel 1 DCD/ Channel 1 SPI enable (SEL_)/ Channel 1 TXCLK	DMA channel 3/5 DONE_In

Mnemonic	Signal	Description
TCK	Test mode clock	TCK operates the JTAG standard. Consult the JTAG specifications for use in boundary-scan testing. These signals meet the requirements of the Raven and Jeeni debuggers.

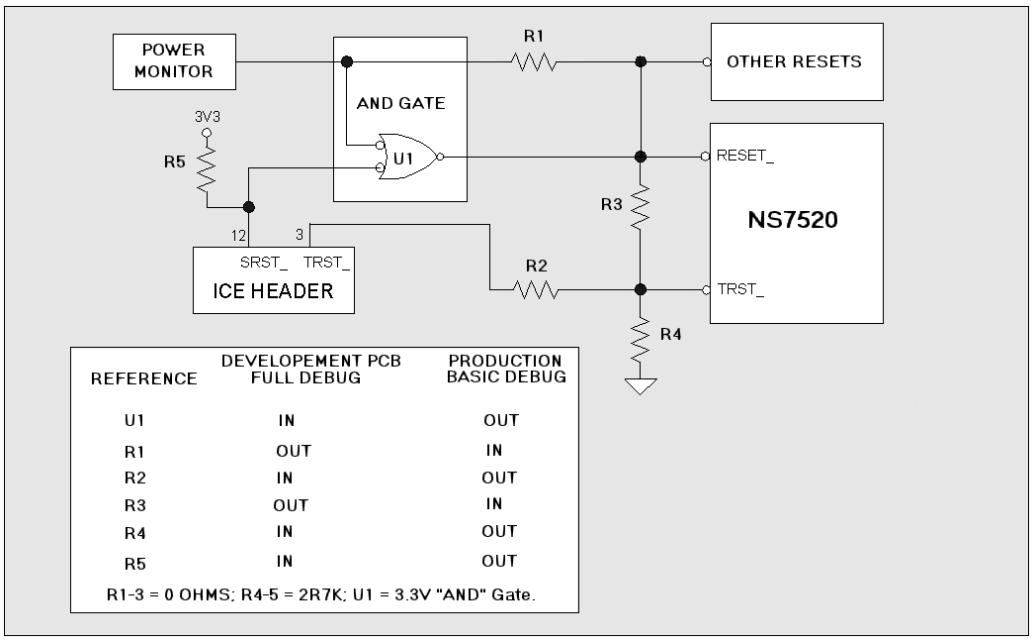


Figure 3: TRST_ termination

Power supply

Signal	Pin	Description
Oscillator VCC (3.3V)	N13, C3	Oscillator power supply
Core VCC (1.5V)	R8, L14, C14, C13	Core power supply
I/O VCC (3.3V)	E4, K4, M2, N3, P3, R5, H14, F14, B8, A3	I/O power supply
GND	D2, F1, J4, P4, P7, M8, P9, R11, K15, G15, E13, D13, B14, C11, A7, A5, B2, P2, P14, K13	Ground

NS7520 bootstrap initialization

Many internal NS7520 features are configured when the RESET pin is asserted. The address bus configures the appropriate control register bits at powerup. This table shows which bits control which functions:

Address bit	Name	Description
ADDR[27]	Endian configuration	0 Little Endian configuration 1 Big Endian configuration
ADDR[26]	CPU bootstrap	0 CPU disabled; GEN_BUSER=1 1 CPU enabled; GEN_BUSER=0
ADDR[24:23]	CS0/MMCR[19:18] setting	00 8-bit SRAM, 63 wait-states/b00 01 32-bit SRAM, 63 wait-states/b01 10 32-bit SRAM 11 16-bit SRAM, 63 wait-states/b11
ADDR[19:9]	GEN_ID setting	GEN_ID=A[19:09],default='h3ff
ADDR[8:7]	PLL IS setting	IS=A[8:7], default='b10
ADDR[6:5]	PLL FS setting	FS=A[6:5], default='b00
ADDR[4:0]	PLL ND setting	ND=A[4:0], default='b01011

Table 3: NS7520 test modes

JTAG

The NS7520 provides full support for 1149.1 JTAG boundary scan testing. All NS7520 pins can be controlled using the JTAG interface port. The JTAG interface provides access to the ARM7TDMI debug module when the appropriate combination of PLLTST_, BISTEN_, and SCANEN_ is selected (as shown in Table 3: "NS7520 test modes").

ARM Debug

The ARM7TDMI core uses a JTAG TAP controller that shares the pins with the TAP controller used for 1149.1 JTAG boundary scan testing. To enable the ARM7TDMI TAP controller, {PLLTST_,BISTEN_,SCANEN_} must be set as shown in Table 3: "NS7520 test modes".

DC characteristics and other operating specifications

The NS7520 operates using an internal core V_{DD} supply voltage of 1.5V. A 3.3VC supply is required for the I/O cells, which drive/accept 3.3V levels.

Table 4 provides the DC characteristics for inputs; Table 5 provides the DC characteristics for outputs.

Sym	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high voltage		2.0		3.6	V
V_{IL}	Input low voltage		V_{SS} – 0.3		0.8	V

Table 4: DC characteristics — Inputs

Sym	Parameter	Conditions		Min	Max		Unit
P	Power consumption	F_{SYSCLK} = 55 MHz			508		mW
			Core			192	mW
			I/O			316	mW
		F_{SYSCLK} = 46 MHz			425		mW
			Core			161	mW
			I/O			264	mW
		F_{SYSCLK} = 36 MHz			333		mW
			Core			126	mW
			I/O			207	mW
V_{OL}	Output low voltage	Outputs & bi-directional		0	0.4		V
V_{OH}	Output high voltage	Outputs & bi-directional		2.4	V_{DD}		V

Table 5: DC characteristics — Outputs

Table 6 defines the DC operating (thermal) conditions for the NS7520. Operating the NS7520 outside these conditions results in unpredictable behavior.

Sym	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Core supply voltage		1.4	1.5	1.6	V
V_{CC}	I/O supply voltage		3.0	3.3	3.6	V
T_{OP}	Ambient temperature		-40		85	^{o}C
T_J	Junction temperature			110		^{o}C
T_{STG}	Storage temperature		-40		125	^{o}C
θ_J	Pkg thermal resistance			50		^{o}C/W
I_{IH}	Input threshold	No pullup	-10		10	µA

Table 6: Recommended operating temperatures

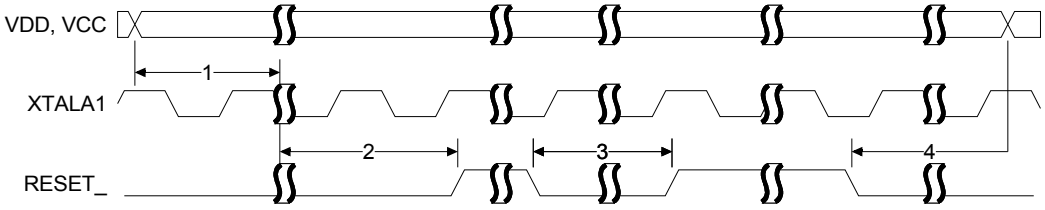
Reset_timing

From a cold start, RESET_ must be asserted until all power supplies are above their specified thresholds. An additional 8 microseconds is required for oscillator settling time (allow 40ms for crystal startup).

Due to an internal three flip-flop delay on the external RESET_ signal, after the oscillator is settled, RESET_ must be asserted for three periods of the XTALA1 clock in these situations:

- Before release of reset after application of power
- While valid power is maintained to initiate *hot reset* (reset while power is at or above specified thresholds)
- Before loss of valid power during power outage/power down

The PORTC4 output indicates the reset state of the chip. PORTC4 persists beyond the negation of RESET_ for approximately 512 system clock cycles if the PLL is disabled. When the PLL is enabled, PORTC4 persists beyond the negation of RESET_ to allow for PLL lock for 100 microseconds times the ratio of the VCO to XTALA.

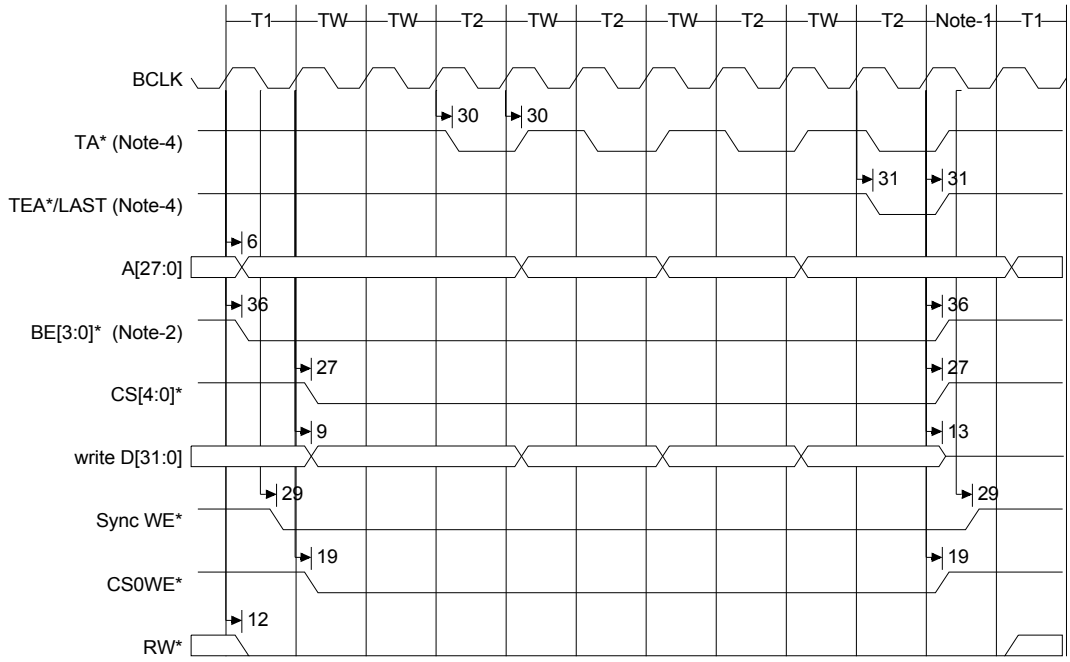


Reset timing parameters

Num	Description	Min	Typ	Max	Units
1	Power valid before reset negated	40			ms **Note:** RESET_ should remain low for at least 40ms after power reaches 3.0V.
2	Reset asserted after power valid	3			T_{XTALA1}
3	Reset asserted while power valid	3			T_{XTALA1}
4	Reset asserted before power invalid	3			T_{XTALA1}

SRAM burst write

CS controlled, four word (4-2-2-2), burst write (wait = 2, BCYC = 01)



Notes:

1 If the next transfer is DMA, null periods between memory transfers can occur. Thirteen clock pulses are required for DMA context switching.

2 Port size determines which byte enable signals are active:

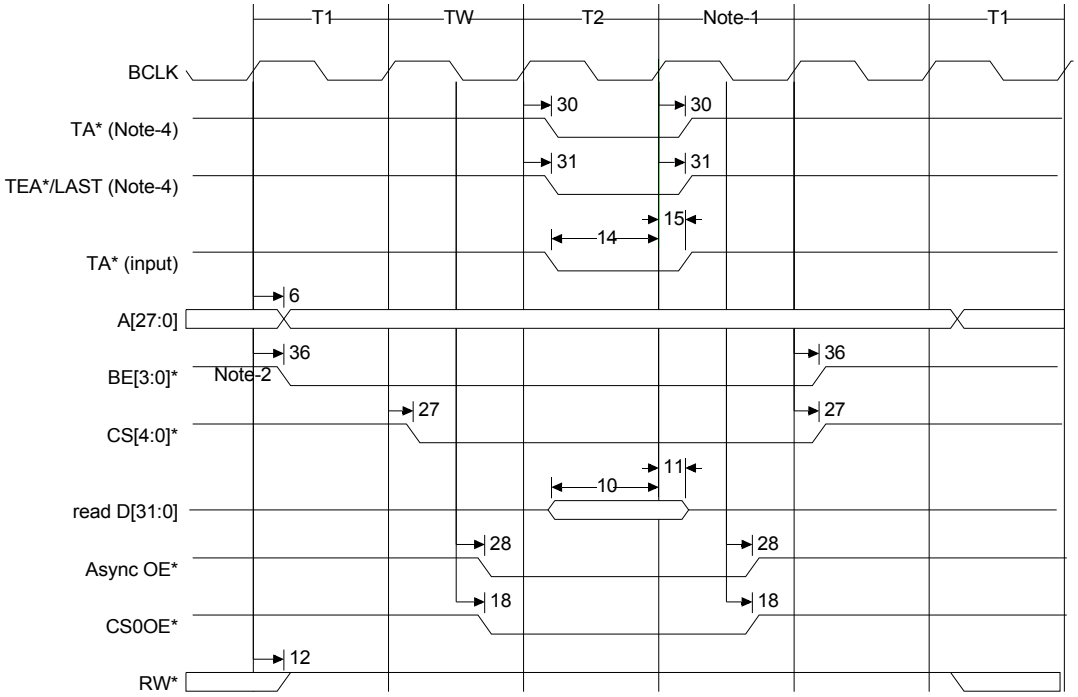
- 8-bit port = BE3*
- 16-bit port = BE[3:0]
- 32-bit port = BE[3:0]

3 The TW cycles are present when the WAIT field is set to 2 or more.

4 The TA* and TEA*/LAST signals are for reference only.

SRAM OE read

OE* controlled read (wait = 2)



Notes:

1 At least one null period occurs between memory transfers. More null periods can occur if the next transfer is DMA. Thirteen clock pulses are required for DMA context switching.

2 Port size determines which byte enable signals are active:

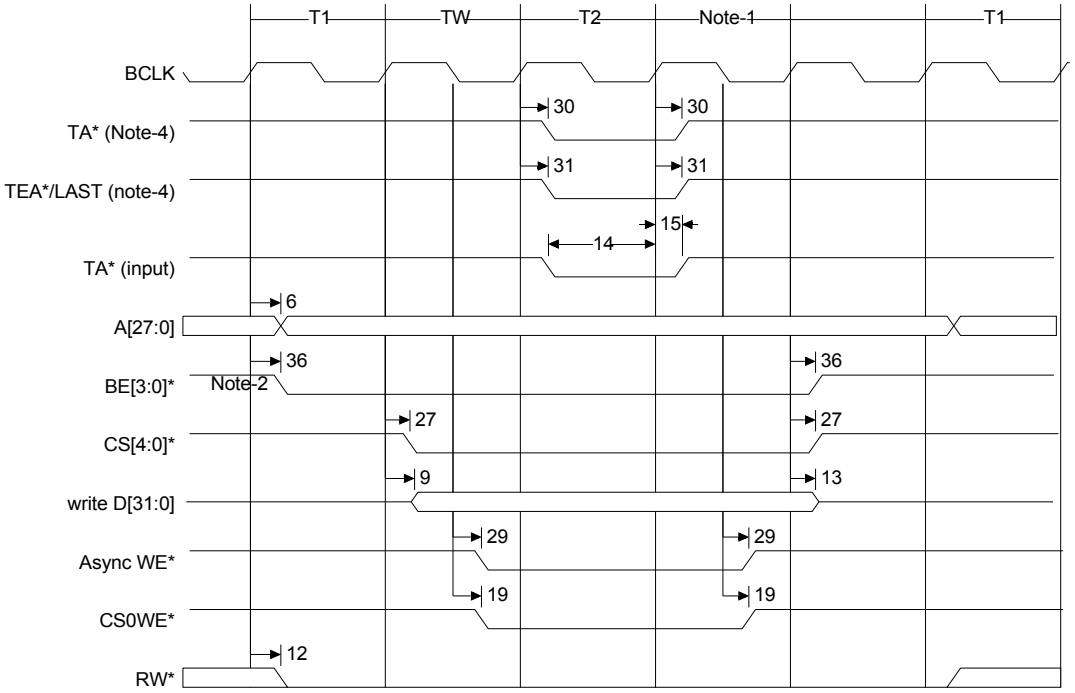
- 8-bit port = BE3*
- 16-bit port = BE[3:0]
- 32-bit port = BE[3:0]

3 The TW cycles are present when the WAIT field is set to 2 or more.

4 The TA* and TEA*/LAST signals are for reference only.

SRAM WE write

WE* controlled write (wait = 2)



Notes:

1 At least one null period occurs between memory transfers. More null periods can occur if the next transfer is DMA. Thirteen clock pulses are required for DMA context switching.

2 Port size determines which byte enable signals are active:

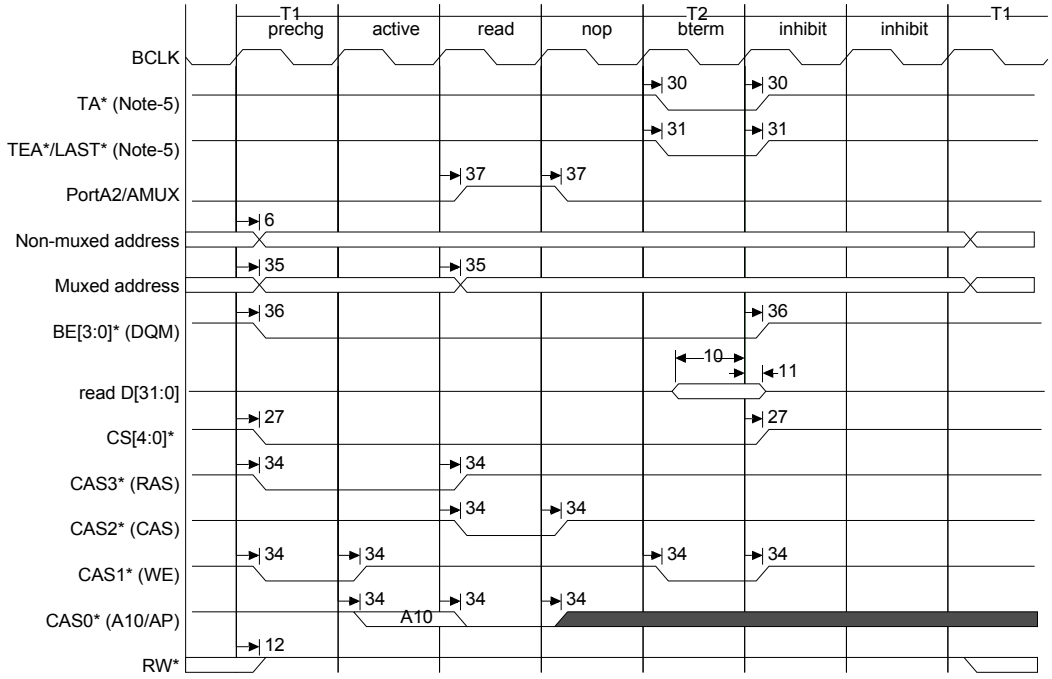
- 8-bit port = BE3*
- 16-bit port = BE[3:0]
- 32-bit port = BE[3:0]

3 The TW cycles are present when the WAIT field is set to 2 or more.

4 The TA* and TEA*/LAST signals are for reference only.

SDRAM read

SDRAM read, CAS latency = 2



Notes:

1 Port size determines which byte enable signals are active:

- 8-bit port = BE3*
- 16-bit port = BE[3:2]
- 32-bit port = BE[3:0]

2 The precharge and/or active commands are not always present. These commands depend on the address of the previous SDRAM access.

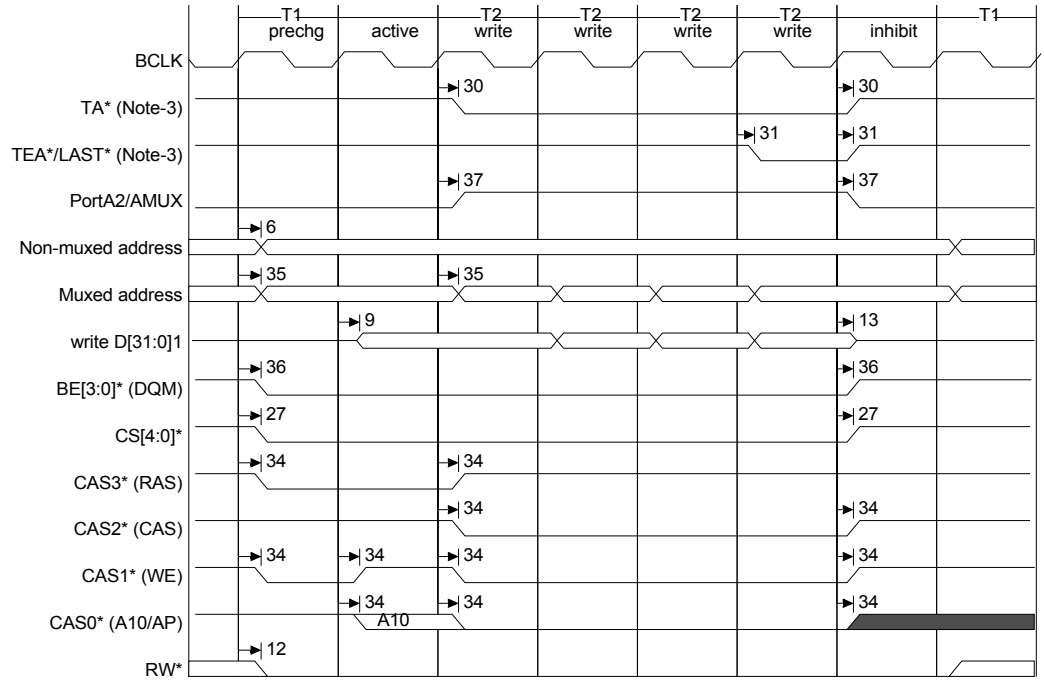
3 If CAS latency = 3, 2 NOPs occur between the read and burst terminate commands.

4 If CAS latency = 3, 3 inhibits occur after burst terminate.

5 The TA* and TEA*/LAST signals are for reference only.

SDRAM burst write

SDRAM burst write



Notes:

1 Port size determines which byte enable signals are active:

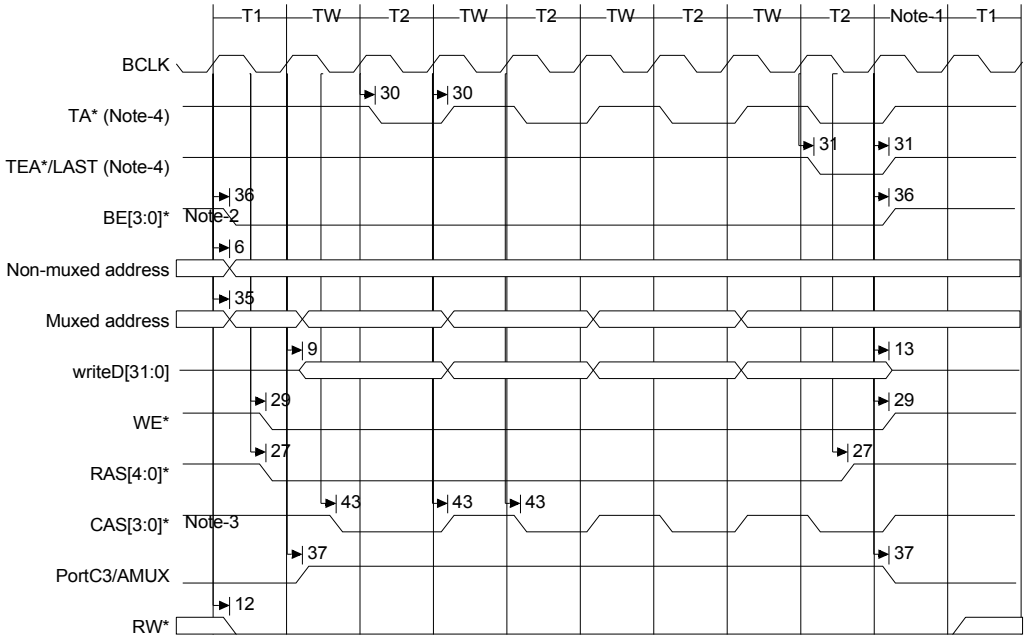
- 8-bit port = BE3*
- 16-bit port = BE[3:2]
- 32-bit port = BE[3:0]

2 The precharge and/or active commands are not always present. These commands depend on the address of the previous SDRAM access. When the active command is not present, parameter #35 is valid during the write (T2) cycle.

3 The TA* and TEA*/LAST signals are for reference only.

FP DRAM burst write

Fast Page burst write



Notes:

1 If the next transfer is DMA, null periods between memory transfers can occur. Thirteen clock pulses are required for DMA context switching.

2 Port size determines which byte enable signals are active:

- 8-bit port = BE3*
- 16-bit port = BE[3:2]
- 32-bit port = BE[3:0]

3 Port size determines which CAS signals are active:

- 8-bit port = CAS3*
- 16-bit port = CAS[3:2]
- 32-bit port = CAS[3:0]

4 The TA* and TEA*/LAST signals are for reference only.

5 The BCYC field should never be set to 00.

Ethernet timing

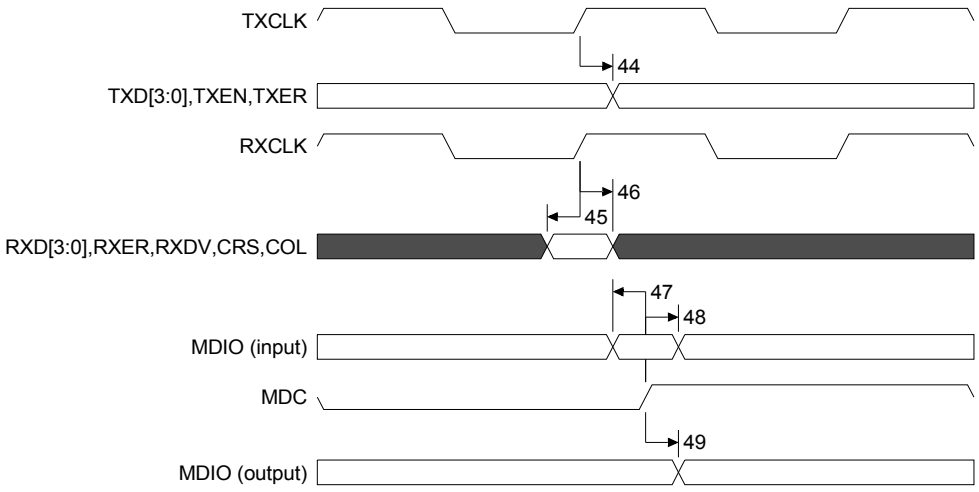
Operating conditions:

Temperature:	-15.00 (min)	110.00 (max)
Voltage:	1.60 (min)	1.40 (max)
Output load:	25.0pf	
Input drive:	CMOS buffer	

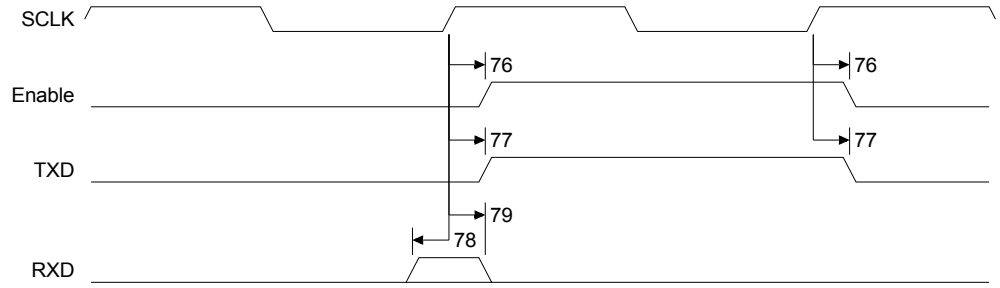
Ethernet timing parameters

Num	Description	Min	Max	Unit
44	TXCLK high to TXD*, TXEN, TXER valid		11.5	ns
45	RXD*, RXER, RXDV, TXCOL, RXCRS valid to RXCLK high (setup)	3		ns
46	RXCLK high to RXD*, RXER, RXDV, TXCOL, RXCRS hold time	2		ns
49	MDC high to MDIO valid		50	ns
47	MDIO valid to MDC high (setup)	3		ns
48	MDC high to MDIO hold time	3		ns
50	RXCLK high to RSPF* valid		15.5	ns
52	REJECT* valid to RXCLK high (setup)	3		ns
53	REJECT* valid from RXCLK high (hold)	1.5		ns

Ethernet PHY timing



synchronous serial internal clock



synchronous serial external clock