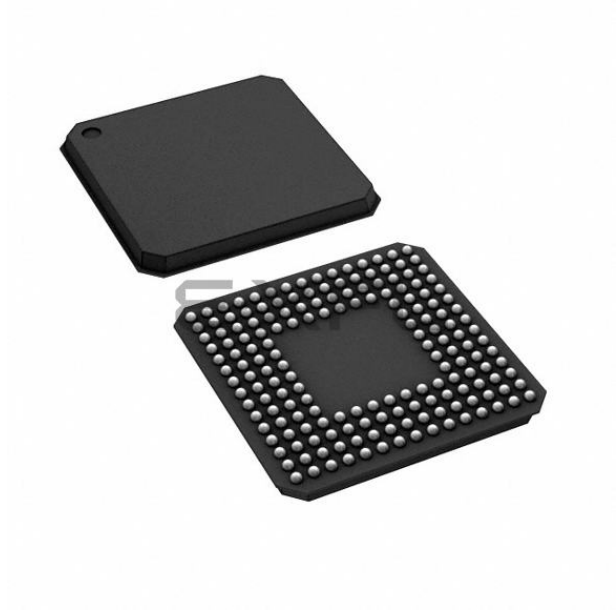

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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Not For New Designs
Applications	Network Processor
Core Processor	ARM7®
Program Memory Type	External Program Memory
Controller Series	-
RAM Size	External
Interface	EBI/EMI, Ethernet, DMA, SPI, UART
Number of I/O	16
Voltage - Supply	1.4V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	177-LFBGA
Supplier Device Package	177-PFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/digi-international/ns7520b-1-i55

Symbol	Pin	I/O	OD	Description
DATA19	H3	I/O	4	
DATA18	H4	I/O	4	
DATA17	H1	I/O	4	
DATA16	H2	I/O	4	
DATA15	G4	I/O	4	
DATA14	G1	I/O	4	
DATA13	G3	I/O	4	
DATA12	G2	I/O	4	
DATA11	F4	I/O	4	
DATA10	F2	I/O	4	
DATA9	F3	I/O	4	
DATA8	E1	I/O	4	
DATA7	E2	I/O	4	
DATA6	E3	I/O	4	
DATA5	D1	I/O	4	
DATA4	C1	I/O	4	
DATA3	B1	I/O	4	
DATA2	D4	I/O	4	
DATA1	D3	I/O	4	
DATA0	C2	I/O	4	
BE3_	D9	I/O	2	Byte enable D31:D24
BE2_	A9	I/O	2	Byte enable D23:D16
BE1_	C9	I/O	2	Byte enable D15:D08
BE0_	B9	I/O	2	Byte enable D07:D00
TS_	A8	I/O	4	DO NOT USE Add an external 820 ohm pullup to 3.3 V.
TA_	D8 U	I/O	4	Data transfer acknowledge Add an external 820 ohm pullup to 3.3 V. TA_ is bidirectional. It is used in input mode to terminate a memory cycle externally. It is used in output mode for reference purposes only.
TEA_	C8 U	I/O	4	Data transfer error acknowledge Add an external 820 ohm pullup to 3.3 V. TEA_ is bidirectional. It is used in input mode to terminate a memory cycle externally. It is used in output mode for reference purposes only.

Symbol	Pin	I/O	OD	Description
RW_	D6	I/O	2	Transfer direction
BR_	D7	NO CONNECT		
BG_	C7	NO CONNECT		
BUSY_	B7	NO CONNECT		

System bus interface signal descriptions

Mnemonic	Signal	Description
BCLK	Bus clock	Provides the bus clock. All system bus interface signals are referenced to the BCLK signal.
ADDR[27:0]	Address bus	Identifies the address of the peripheral being addressed by the current bus master. The address bus is bi-directional.
DATA[31:0]	Data bus	Provides the data transfer path between the NS7520 and external peripheral devices. The data bus is bi-directional. **Recommendation:** Less than x32 (S)DRAM/SRAM memory configurations. Unconnected data bus pins will float during memory read cycles. Floating inputs can be a source of wasted power. For other than x32 DRAM/SRAM configurations, the unused data bus signals should be pulled up.
TS_	Transfer start	NO CONNECT
BE_	Byte enable	Identifies which 8-bit bytes of the 32-bit data bus are active during any given system bus memory cycle. The BE_ signals are active low and bi-directional.
TA_	Transfer acknowledge	Indicates the end of the current system bus memory cycle. This signal is driven to 1 prior to tri-stating its driver. TA_ is bi-directional.
TEA_	Transfer error acknowledge	Indicates an error termination or burst cycle termination: ■ In conjunction with TA_ to signal the end of a burst cycle. ■ Independently of TA_ to signal that an error occurred during the current bus cycle. TEA_ terminates the current burst cycle. This signal is driven to 1 prior to tri-stating its driver. TEA_ is bi-directional. The NS7520 or the external peripheral can drive this signal.
RW_	Read/write indicator	Indicates the direction of the system bus memory cycle. RW_ high indicates a read operation; RW_ low indicates a write operation. The RW_ signal is bi-directional.
BR_	Bus request	NO CONNECT
BG_	Bus grant	NO CONNECT
BUSY_	Bus busy	NO CONNECT

Chip select controller

The NS7520 supports five unique chip select configurations.

Symbol	Pin	I/O	OD	Description
CS4_	B4	O	4	Chip select/DRAM RAS_
CS3_	A4	O	4	Chip select/DRAM RAS_
CS2_	C5	O	4	Chip select/DRAM RAS_
CS1_	B5	O	4	Chip select/DRAM RAS_
CS0_	D5	O	4	Chip select (boot select)
CAS3_	A1	O	4	FP/EDO DRAM column strobe D31:D24/SDRAM RAS_
CAS2_	C4	O	4	FP/EDO DRAM column strobe D23:D16/SDRAM CAS_
CAS1_	B3	O	4	FP/EDO DRAM column strobe D15:D08/SDRAM WE_
CAS0_	A2	O	4	FP/EDO DRAM column strobe D07:D00/SDRAM A10(AP)
WE_	C6	O	4	Write enable for NCC Ctrl'd cycles
OE_	B6	O	4	Output enable for NCC Ctrl'd cycles

Chip select controller signal descriptions

Mnemonic	Signal	Description
CS0_ CS1_ CS2_ CS3_ CS4_	Chip select 0 Chip select 1 Chip select 2 Chip select 3 Chip select 4	Unique chip select outputs supported by the NS7520. Each chip select can be configured to decode a portion of the available address space and can address a maximum of 256 Mbytes of address space. The chip selects are configured using registers in the memory module. A chip select signal is driven low to indicate the end of the current memory cycle. For FP/EDO DRAM, these signals provide the RAS signal.
CAS0_ CAS1_ CAS2_ CAS3_	Column address strobe signals	Activated when an address is decoded by a chip select module configured for DRAM mode. The CAS_ signals are active low and provide the column address strobe function for DRAM devices. The CAS_ signals also identify which 8-bit bytes of the 32-bit data bus are active during any given system bus memory cycle. For SDRAM, CAS[3:1]_ provides the SDRAM command field. CAS0_ provides the auto-precharge signal. For non-DRAM settings, these signals are 1.
WE_	Write enable	Active low signal that indicates that a memory write cycle is in progress. This signal is activated only during write cycles to peripherals controlled by one of the chip selects in the memory module.
OE_	Output enable	Active low signal that indicates that a memory read cycle is in progress. This signal is activated only during read cycles from peripherals controlled by one of the chip selects in the memory module.

Ethernet interface MAC

Note: ENDEC values for general-purpose output and TXD refer to bits in the Ethernet General Control register. ENDEC values for general-purpose input and RXD refer to bits in the Ethernet General Status register.

In this table, *GP* designates *general-purpose*.

Symbol		Pin	I/O	OD	Description	
MII	**ENDEC**				**MII**	**ENDEC**
MDC	GP output	D10	O	2	MII management clock	State of (LPBK bit XOR (Mode=SEEQ))
MDIO	GP output	B10 U	I/O	2	MII data	State of UTP_STP bit
TXCLK		C10	I		TX clock	
TXD3	GP output	A12	O	2	TX data 3	State of AUI_TP[0] bit
TXD2	GP output	B11	O	2	TX data 2	State of AUI_TP[1] bit
TXD1	GP output	D11	O	2	TX data 1	Inverted state of PDN bit, open collector
TXD0	TXD	A11	O	2	TX data 0	Transmit data
TXER	GP output	A13	O	2	TX code error	State of LNK_DIS_ bit
TXEN		B12	O	2	TX enable	
TXCOL		A14	I		Collision	
RXCRS		D12	I		Carrier sense	
RXCLK		C12	I		RX clock	
RXD3	GP input	D14	I		RX data 3	Read state in bit 12
RXD2	GP input	B15	I		RX data 2	Read state in bit 15
RXD1	GP input	A15	I		RX data 1	Read state in bit 13
RXD0	RXD	B13	I		RX data 0	Receive data
RXER	GP input	C15	I		RX error	Read state in bit 11
RXDV	GP input	D15	I		RX data valid	Read state in bit 10

Ethernet interface MAC signal descriptions

The Ethernet MII (media independent interface) provides the connection between the Ethernet PHY and the MAC (media access controller).

Mnemonic	Signal	Description
MDC	MII management clock	Provides the clock for the MDIO serial data channel. The MDC signal is an NS7520 output. The frequency is derived from the system operating frequency per the CLKS field setting (see the CLKS field in Table 69: "MII Management Configuration register bit definition" on page 191).

"No connect" pins

Pin	Description
R13	Add a 15K ohm pulldown to GND (15K ohm is the recommended value; 10–20K ohms is acceptable)
P12	Add a 15K ohm pulldown to GND (15K ohm is the recommended value; 10–20K ohms is acceptable)
N12	Tie to GND
R15	XTALB2: NO CONNECT
M11	NO CONNECT
P11	NO CONNECT
N11	NO CONNECT
R12	NO CONNECT
R14	NO CONNECT
P13	NO CONNECT

Note: If your design implements 10-2-K ohm *pullups* instead of *pulldowns* on R13 and P12, and a pullup on N12 instead of *GND*, no action is required.

General Purpose I/O

GPIO signal	Serial signal	Other signal	Pin	I/O	OD	Serial channel description	Other description
PORTA7	TXDA		J14 U	I/O	2	Channel 1 TXD	
PORTA6	DTRA_	DREQ1_	J13 U	I/O	2	Channel 1 DTR_	DMA channel 3/5 Req
PORTA5	RTSA_		J15 U	I/O	2	Channel 1 RTS_	
PORTA4	RXCA/RIA_/ OUT1A_		J12 U	I/O	2	Pgm'able Out/ Channel 1 RXCLK/ Channel 1 ring signal/Channel 1 SPI clock (CLK)	
PORTA3	RXDA	DACK1_	H15 U	I/O	2	Channel 1 RXD	DMA channel 3/5 ACK
PORTA2	DSRA_	AMUX	H12 U	I/O	2	Channel 1 DSR_	DRAM addr mux
PORTA1	CTSA_	DONE1_ (O)	H13 U	I/O	2	Channel 1 CTS_	DMA channel 3/5 DONE_Out
PORTA0	TXCA/ OUT2A_/ DCDA_	DONE1_ (I)	G12 U	I/O	2	Pgm'able Out/ Channel 1 DCD/ Channel 1 SPI enable (SEL_)/ Channel 1 TXCLK	DMA channel 3/5 DONE_In

System mode (test support)

PLLTST_, BISTEN_, and SCANEN_ primary inputs control different test modes for both functional and manufacturing test operations (see Table 3: "NS7520 test modes" on page 22).

Symbol	Pin	I/O	OD	Description
PLLTST_	N15	I		Encoded with BISTEN_ and SCANEN_ Add an external pullup to 3.3V or pulldown to GND.
BISTEN_	M15	I		Encoded with PLLTST_ and SCANEN_ Add an external pullup to 3.3V or pulldown to GND.
SCANEN_	L13	I		Encoded with BISTEN_ and PLLTST_ Add an external pullup to 3.3V or pulldown to GND.

JTAG test

JTAG boundary scan allows a tester to check the soldering of all signal pins and tri-state all outputs.

Symbol	Pin	I/O	OD	Description
TDI	N14 U	I		Test data in.
TDO	M13	O	2	Test data out.
TMS	M12 U	I		Test mode select.
TRST_	M14	I		Test mode reset. Requires external termination when not being used (see Figure 3, "TRST_ termination," on page 17 for an illustration of the termination circuit on the development PCB).
TCK	P15	I		Test mode clock. Add an external pullup to 3.3V.

ARM debugger signal descriptions

Mnemonic	Signal	Description
TDI	Test data in	TDI operates the JTAG standard. Consult the JTAG specifications for use in boundary-scan testing. These signals meet the requirements of the Raven and Jeeni debuggers.
TDO	Test data out	TDO operates the JTAG standard. Consult the JTAG specifications for use in boundary-scan testing. These signals meet the requirements of the Raven and Jeeni debuggers.
TMS	Test mode select	TMS operates the JTAG standard. Consult the JTAG specifications for use in boundary-scan testing. These signals meet the requirements of the Raven and Jeeni debuggers.
TRST_	Test mode reset	TRST_ operates the JTAG standard. Consult the JTAG specifications for use in boundary-scan testing. These signals meet the requirements of the Raven and Jeeni debuggers.

NS7520 modules

CPU module

The CPU uses an ARM7TDMI core processor. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, which result in high instruction throughput and impressive real-time interrupt response for a small, cost-effective circuit. For more information about ARM7TDMI, see the ARM7TDMI Data Sheet from ARM Ltd. (www.arm.com).

GEN module

The GEN module provides the NS7520 with its main system control functions, as well as these features:

- Two programmable timers with interrupt
- One programmable bus-error timer
- One programmable watchdog timer
- Two 8-bit programmable general-purpose I/O ports

System (SYS) module

The system module provides the system clock (SYS_CLK) and system reset (SYS_RESET) resources.

The system control signals determine the basic operation of the chip:

Signal mnemonic	Signal name	Description
{XTALA1, XTALA2}	Clock source	Operate in one of two ways: ■ The signals are affixed with a 10-20 MHz parallel mode quartz crystal or crystal oscillator and the appropriate components per the component manufacturer. ■ XTALA1 is driven with a clock signal and XTALA2 is left open.
{PLLVDD, PLLVSS}	PLL power	Provide an isolated power supply for the PLL.
RESET_	Chip reset	Active low signal asserted to initiate a hardware reset of the chip.
{TDI, TDO, TNS, TRST_, TCK}	JTAG interface	Provide a JTAG interface for the chip. This interface is used for both boundary scan and ICE control of the internal processor.
{PLLTEST_, BISTEN_, SCANEN_}	Chip mode	Encoded to determine the chip mode.

The NS7520 clock module creates the BCLK and FXTAL signals. Both signals are used internally, but BCLK can also be accessed at ball A6 by setting the BCLKD field in the System Control register to 0.

- BCLK functions as the system clock and provides the majority of the NS7520's timing.
- FXTAL provides the timing for the DRAM refresh counter, can be selected instead of BCLK to provide timing for the watchdog timer, the two internal timers, and the Serial module.

BBus module

The BBus module provides the data path among NS7520 internal modules. This module provides the address and data multiplexing logic that supports the data flow through the NS7520. The BBus module is the central arbiter for all the NS7520 bus masters and, once mastership is granted, handles the decoding of each address to one (or none) of the NS7520 modules.

Memory module (MEM)

The MEM module provides a glueless interface to external memory devices such as Flash, DRAM, and EEPROM. The memory controller contains an integrated DRAM controller and supports five unique chip select configurations.

The MEM module monitors the BBus interface for access to the bus module; that is, any access not addressing internal resources. If the address to be used corresponds to a Base Address register in the MEM module, the MEM module provides the memory access signals and responds to the BBus with the necessary completion signal.

The MEM module can be configured to interface with FP, EDO, or SDRAM (synchronous DRAM), although the NS7520 cannot interface with more than one device type at a time.

DMA controller

The NS7520 contains one DMA controller, with 13 DMA channels. Each DMA channel moves blocks of data between memory and a memory peripheral.

The DMA controller supports both fly-by operations and memory-to-memory operations:

- When configured for fly-by operation, the DMA controller transfers data between one of the NS7520 peripherals and a memory location.
- When configured for memory-to-memory operations, the DMA controller uses a temporary holding register between read and write operations. Two memory cycles are executed.

Ethernet controller

The Ethernet controller provides the NS7520 with one IEEE 802.3u compatible Ethernet interface. The Ethernet interface includes the Ethernet front-end (EFE) and media access controller (MAC).

The Ethernet module supports both media independent interface (MII) and ENDEC modes.

Sym	Parameter	Conditions	Min	Typ	Max	Unit
I_{IL}	Input current as “0”	No pullup	10		10	µA
I_{OZ}	HighZ leakage current	Any input	-10		10	µA
C_{IO}	Pin capacitance	V_O=0			7	pF

Table 6: Recommended operating temperatures

Absolute maximum ratings

This table defines the maximum values for the voltages that the NS7520 can withstand without being damaged.

Sym	Parameter	Min	Max
V_{DD}	Core supply voltage	-0.3	3.15
V_{CC}	I/O supply voltage	-0.3	3.9
V_{IN}	Input voltage	-0.3	3.9
V_{OUT}	Output voltage	-0.3	3.9

Pad pullup and pulldown characteristics

Figure 5 illustrates characteristics for a pad with internal pullup; Figure 6 illustrates characteristics for a pad with internal pulldown. See "Pinout detail tables," beginning on page 6, for information about which pins use pullup and pulldown resistors.

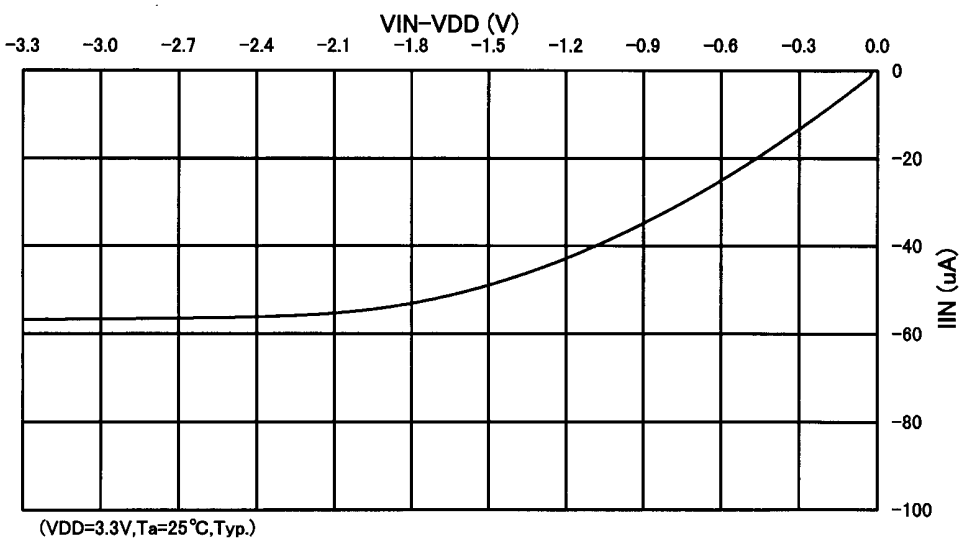


Figure 5: Internal pullup characteristics

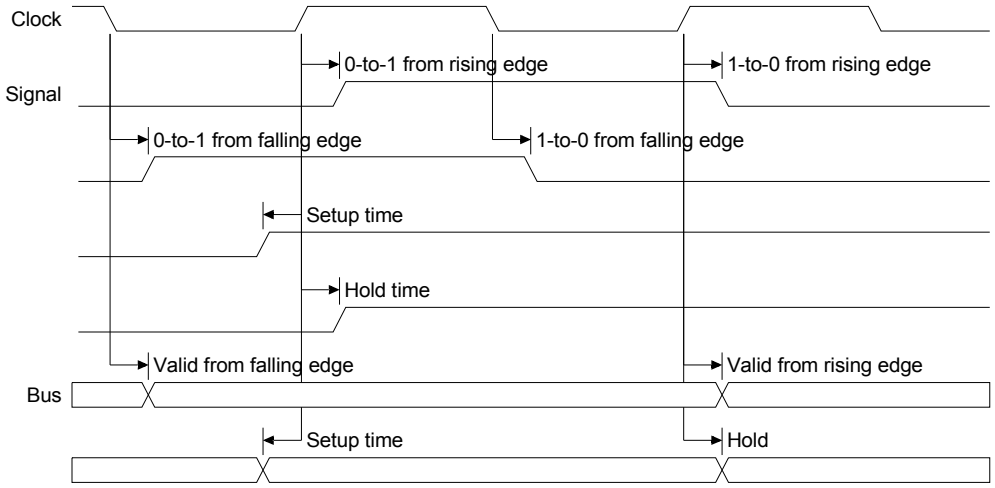
Timing Diagrams

Timing_Specifications

All timing specifications consist of the relationship between a reference clock and a signal:

- There are bussed and non-bussed signals. Non-bussed signals separately illustrate 0-to-1 and 1-to-0 transitions.
- Inputs have setup/hold times versus clock rising.
- Outputs have switching time relative to either clock rising or clock falling.

Note: Timing relationships in this diagram are drawn without proportion to actual delay.



SRAM timing

BCLK max frequency: 55.296 MHz

Operating conditions:

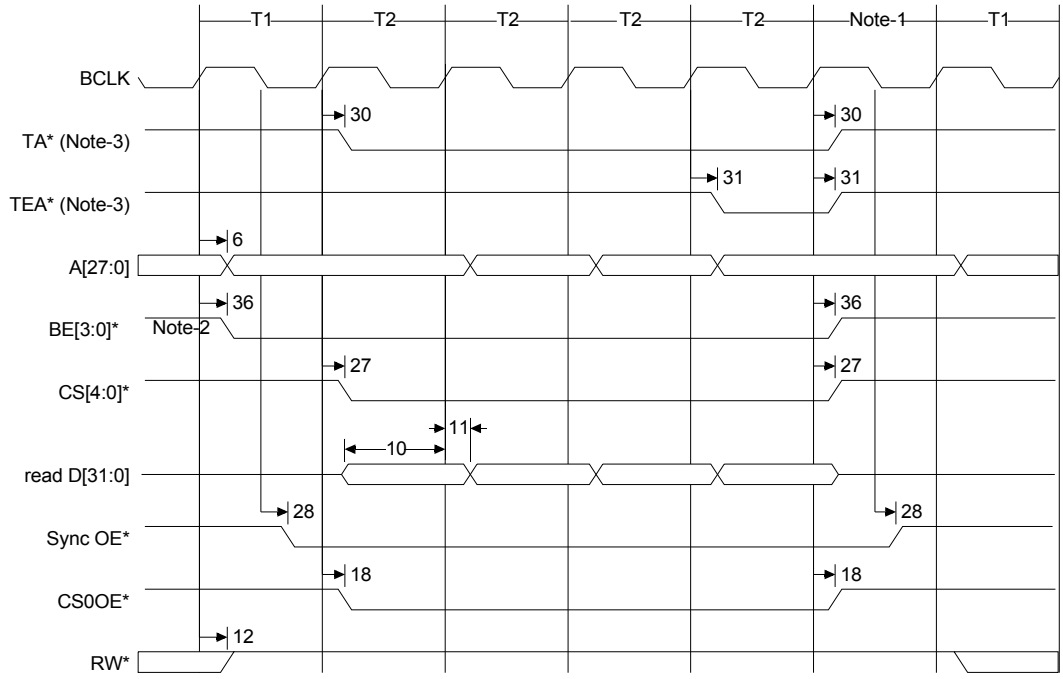
Temperature:	-15.00 (min)	110.00 (max)
Voltage:	1.60 (min)	1.40 (max)
Output load:	25.0pf	
Input drive:	CMOS buffer	

SRAM timing parameters

Num	Description	Min	Max	Unit
36	BCLK high to BE* valid		15.5	ns
6	BCLK high to address valid	5	13.5	ns
9	BCLK high to data out valid		14	ns
13	BCLK high to data out high impedance		13	ns
10	Data in valid to BCLK high (setup)	5		ns
11	BCLK high to data in invalid (hold)	3		ns
14	TA* valid to BCLK high (setup)	5		ns
15	BCLK high to TA* invalid (hold)	3		ns
27	BCLK high to CS* valid		12.5	ns
28	BCLK low to OE* valid		12.5	ns
29	BCLK low to WE* valid		13	ns
30	BCLK high to TA* valid		13.5	ns
31	BCLK high to TEA* valid		16	ns
18	BCLK low to A27 (CS0OE*) valid		13.5	ns
19	BCLK low A26 (CS0WE*) valid		13.5	ns
12	BCLK high to RW* valid		13.5	ns

SRAM burst read (2111)

CS* controlled read (wait = 0, BCYC = 00)



Notes:

1 If the next transfer is DMA, null periods between memory transfers can occur. Thirteen clock pulses are required for DMA context switching.

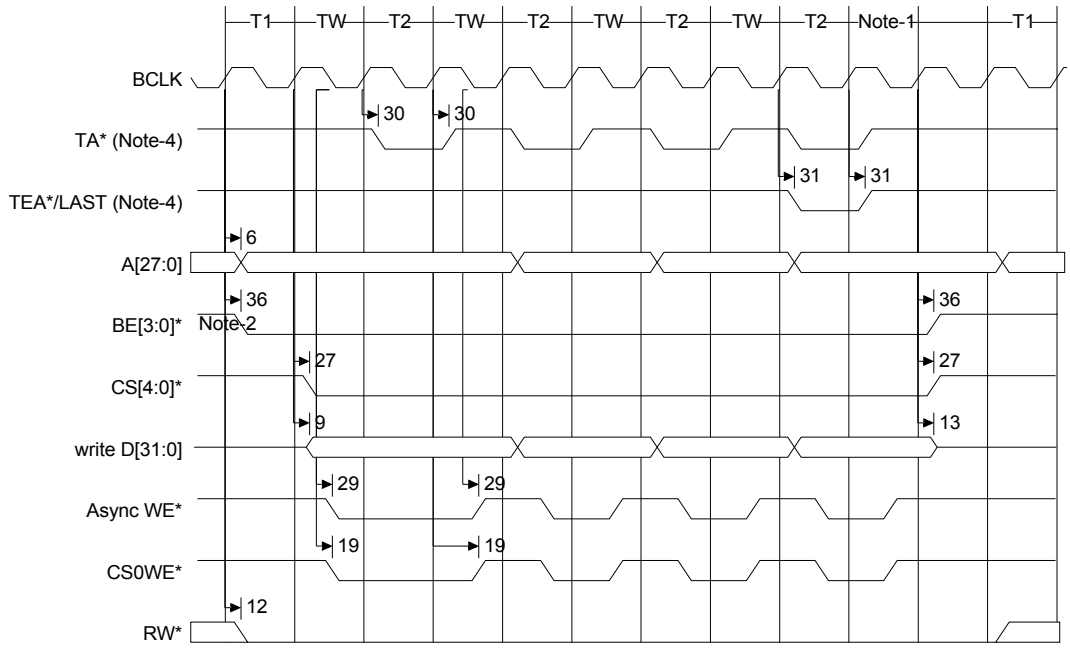
2 Port size determines which byte enable signals are active:

- 8-bit port = BE3*
- 16-bit port = BE[3:0]
- 32-bit port = BE[3:0]

3 The TA* and TEA*/LAST signals are for reference only.

SRAM WE burst write

WE* controlled, four word (3-2-2-2), burst write (wait = 2, BCYC = 01)



Notes:

1 At least one null period occurs between memory transfers. More null periods can occur if the next transfer is DMA. Thirteen clock pulses are required for DMA context switching.

2 Port size determines which byte enable signals are active:

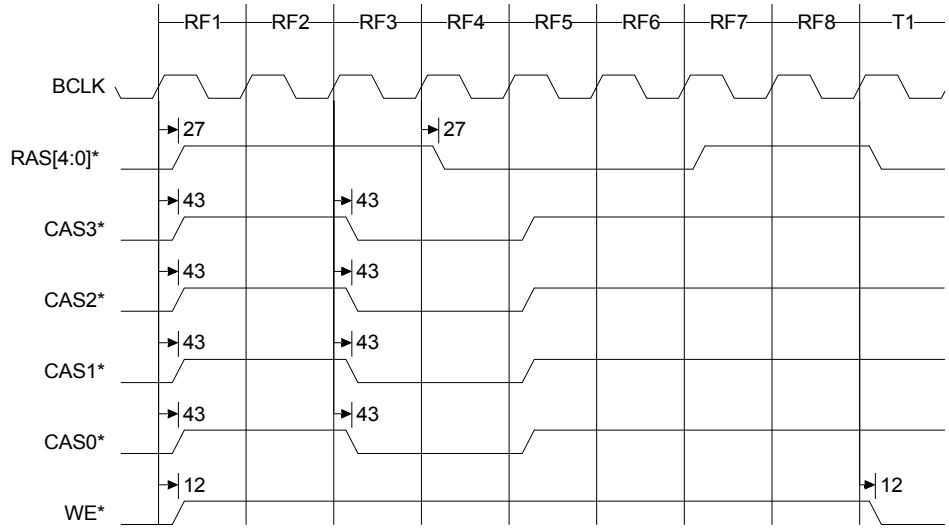
- 8-bit port = BE3*
- 16-bit port = BE[3:0]
- 32-bit port = BE[3:0]

3 The TW cycles are present when the WAIT field is set to 2 or more.

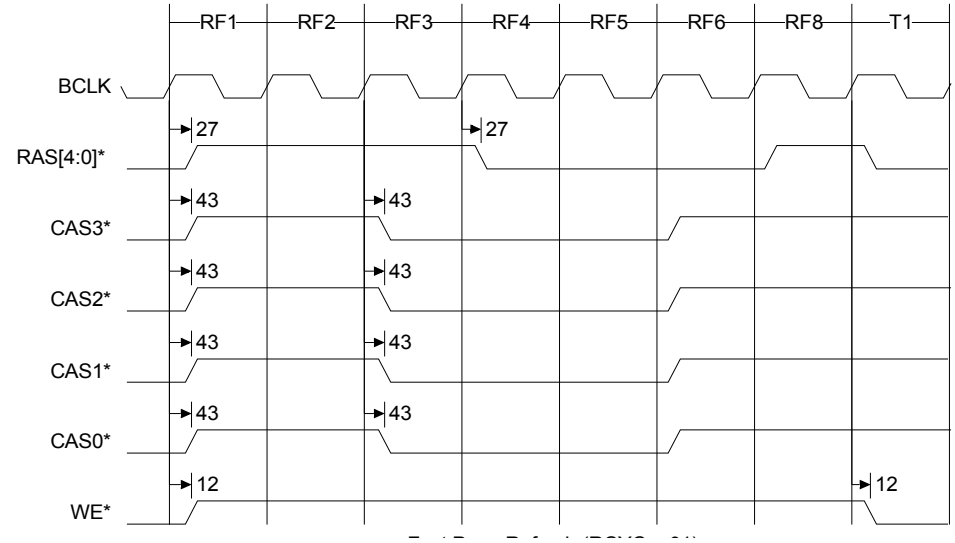
4 The TA* and TEA*/LAST signals are for reference only.

fp_refresh_cycles

Fast page refresh (RCYC = 00)



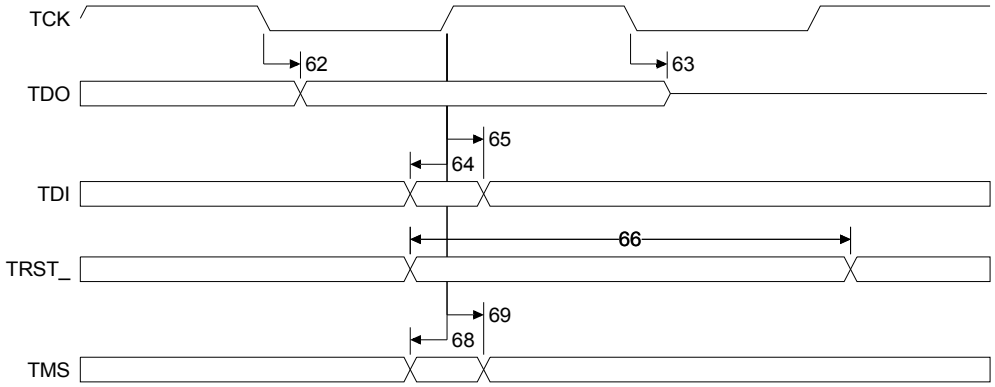
Fast page refresh (RCYC = 01)



jtag bscan timing parameters

Num	Description	Min	Max	Units
62	TCK to TDO valid		21	ns
63	TCK to TDO HighZ		21	ns
64	TDI setup to TCK rising	1		ns
65	TDI hold from TCK rising	3		ns
66	TRST* width	1		T_{TCK}
68	TMS setup to TCK rising	1		ns
69	TMS hold to TCK rising	3		ns

jtag bscan timing diagram



GPIO timing

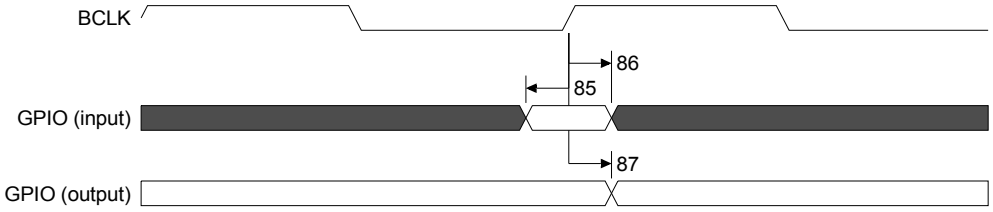
Operating conditions:

Temperature:	-15.00 (min)	110.00 (max)
Voltage:	1.60 (min)	1.40 (max)
Output load:	25.0pf	
Input drive:	CMOS buffer	

GPIO timing parameters

Num	Description	Min	Max	Unit
85	GPIO (setup) to BCLK rising	3		ns
86	GPIO (hold) from BCLK rising	0		ns
87	BCLK to GPIO (output)		17	ns

GPIO timing diagram



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