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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 19x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LFBGA
Supplier Device Package	64-MAPBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk10dn32vmp5

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Terminology and guidelines

Field	Description	Values
FFF	Program flash memory size	 32 = 32 KB 64 = 64 KB 128 = 128 KB 256 = 256 KB 512 = 512 KB 1M0 = 1 MB
R	Silicon revision	 Z = Initial (Blank) = Main A = Revision after main
Т	Temperature range (°C)	 V = -40 to 105 C = -40 to 85
PP	Package identifier	 FM = 32 QFN (5 mm x 5 mm) FT = 48 QFN (7 mm x 7 mm) LF = 48 LQFP (7 mm x 7 mm) LH = 64 LQFP (10 mm x 10 mm) MP = 64 MAPBGA (5 mm x 5 mm) LK = 80 LQFP (12 mm x 12 mm) MB = 81 MAPBGA (8 mm x 8 mm) LL = 100 LQFP (14 mm x 14 mm) ML = 104 MAPBGA (8 mm x 8 mm) LQ = 121 MAPBGA (8 mm x 8 mm) LQ = 144 LQFP (20 mm x 20 mm) MD = 144 MAPBGA (13 mm x 13 mm) MJ = 256 MAPBGA (17 mm x 17 mm)
СС	Maximum CPU frequency (MHz)	 5 = 50 MHz 7 = 72 MHz 10 = 100 MHz 12 = 120 MHz 15 = 150 MHz
Ν	Packaging type	 R = Tape and reel (Blank) = Trays

2.4 Example

This is an example part number:

MK10DN128VLH5

3 Terminology and guidelines

Terminology and guidelines



3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	• @ –40 to 25°C	—	0.176	0.859	μA	
	• @ 70°C	—	2.2	13.1	μA	
	• @ 105°C	—	13	23.9	μA	
I _{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V					
	• @ –40 to 25°C		0.19	0.22	μA	
	• @ 70°C	_	0.49	0.64	uA	
	• @ 105°C	_	2.2	3.2	μA	
I _{DD_VBAT}	Average current when CPU is not accessing RTC registers					9
	• @ 1.8V					
	 @ -40 to 25°C 	_	0.57	0.67	uА	
	• @ 70°C	_	0.90	1.2	μA	
	• @ 105°C	_	2.4	3.5	μA	
	• @ 3.0V				Port	
	 @ -40 to 25°C 		0.67	0.94	uА	
	• @ 70°C		1.0	1.4	uA	
	• @ 105°C	_	2.7	3.9	μA	

Table 6. Power consumption operating behaviors (continued)

- 1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
- 2. 50MHz core and system clock, 25MHz bus clock, and 25MHz flash clock . MCG configured for FEI mode. All peripheral clocks disabled.
- 3. 50MHz core and system clock, 25MHz bus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, and peripherals are in active operation.
- 4. Max values are measured with CPU executing DSP instructions
- 5. 25MHz core and system clock, 25MHz bus clock, and 12.5MHz flash clock. MCG configured for FEI mode.
- 6. 4 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
- 7. 4 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
- 8. 4 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
- 9. Includes 32kHz oscillator current and RTC operation.

5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL

Symbol	Description	Min.	Max.	Unit	Notes
f _{LPTMR_pin}	LPTMR clock	_	25	MHz	
f _{LPTMR_ERCLK}	LPTMR external reference clock	_	16	MHz	
f _{I2S_MCLK}	I2S master clock	_	12.5	MHz	
f _{I2S_BCLK}	I2S bit clock	_	4	MHz	

Table 9. Device clock specifications (continued)

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

5.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CMT, and I²C signals.

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	_	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path		_	ns	3
	External reset pulse width (digital glitch filter disabled)	100	_	ns	3
	Mode select (EZP_CS) hold time after reset deassertion	2	_	Bus clock cycles	
	Port rise and fall time (high drive strength)				4
	Slew disabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	13	ns	
	• $2.7 \le V_{DD} \le 3.6V$	_		ns	
	Slew enabled		7		
	• $1.71 \le V_{DD} \le 2.7V$	—		ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	36 24	ns	

Table 10. General switching specifications

Table continues on the next page...

Symbol	Description	Min.	Max.	Unit	Notes
	Port rise and fall time (low drive strength)				5
	Slew disabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	12	ns	
	• $2.7 \le V_{DD} \le 3.6V$	_	6	ns	
	Slew enabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	36	ns	
	• $2.7 \le V_{DD} \le 3.6V$	_	24	ns	
		1			

Table 10. General switching specifications (continued)

- 1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
- 2. The greater synchronous and asynchronous timing must be met.
- 3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
- 4. 75pF load
- 5. 15pF load

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
TJ	Die junction temperature	-40	125	°C
T _A	Ambient temperature	-40	105	°C

5.4.2 Thermal attributes

Board type	Symbol	Description	64 MAPBGA	64 LQFP	Unit	Notes
Single-layer (1s)	R _{θJA}	Thermal resistance, junction to ambient (natural convection)	107	65	°C/W	1, 2
Four-layer (2s2p)	R _{0JA}	Thermal resistance, junction to ambient (natural convection)	56	46	°C/W	1, 3

Table continues on the next page ...

Board type	Symbol	Description	64 MAPBGA	64 LQFP	Unit	Notes
Single-layer (1s)	R _{0JMA}	Thermal resistance, junction to ambient (200 ft./ min. air speed)	90	53	°C/W	1,3
Four-layer (2s2p)	R _{ejma}	Thermal resistance, junction to ambient (200 ft./ min. air speed)	51	40	°C/W	3
	R _{0JB}	Thermal resistance, junction to board	31	28	°C/W	5
_	R _{θJC}	Thermal resistance, junction to case	31	15	°C/W	6
_	Ψ _{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	6	3	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2. Determined according to JEDEC Standard JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air) with the single layer board horizontal. For the LQFP, the board meets the JESD51-3 specification. For the MAPBGA, the board meets the JESD51-9 specification.

3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions – Forced Convection (Moving Air)* with the board horizontal.

5. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.

- 6. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
- 7. Determined according to JEDEC Standard JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air).

6 Peripheral operating requirements and behaviors

6.1 Core modules

Symbol	Description	Min.	Тур.	Max.	Unit	Notes	
f _{fll_ref}	FLL reference free	quency range	31.25	—	39.0625	kHz	
f _{dco}	DCO output frequency range	Low range (DRS=00) 640 × f _{fll_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f _{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f _{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f _{fll_ref}	80	83.89	100	MHz	
f _{dco_t_DMX3}	DCO output frequency	Low range (DRS=00) 732 × f _{fll_ref}	_	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f _{fll_ref}	_	47.97	_	MHz	
		Mid-high range (DRS=10) 2197 × f _{fll_ref}	_	71.99	_	MHz	
		High range (DRS=11) 2929 × f _{fll_ref}	_	95.98	_	MHz	
J _{cyc_fll}	FLL period jitter		_	180	_	ps	
	 f_{VCO} = 48 M f_{VCO} = 98 M 	Hz Hz	_	150	_		
t _{fll_acquire}	FLL target frequer	ncy acquisition time	—		1	ms	6
	-	Р	LL				
f _{vco}	VCO operating fre	quency	48.0	—	100	MHz	
I _{pll}	PLL operating cur PLL @ 96 M 2 MHz, VDI	rent 1Hz (f _{osc_hi_1} = 8 MHz, f _{pll_ref} = V multiplier = 48)	_	1060	_	μΑ	7
I _{pll}	PLL operating current • PLL @ 48 MHz (f _{osc_hi_1} = 8 MHz, f _{pll_ref} = 2 MHz, VDIV multiplier = 24)			600	_	μA	7
f _{pll_ref}	PLL reference frequency range		2.0	—	4.0	MHz	
J _{cyc_pll}	PLL period jitter (F	RMS)					8
	• f _{vco} = 48 MH	lz	-	120	—	ps	
	• f _{vco} = 100 M	Hz	-	50	-	ps	

Table 13. MCG specifications (continued)

Table continues on the next page ...

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	_	μA	
	• 4 MHz	—	400	_	μA	
	• 8 MHz (RANGE=01)	—	500	_	μA	
	• 16 MHz	—	2.5	_	mA	
	• 24 MHz	—	3	_	mA	
	• 32 MHz	—	4	_	mA	
C _x	EXTAL load capacitance	—	—			2, 3
Cy	XTAL load capacitance	—	—	—		2, 3
R _F	Feedback resistor — low-frequency, low-power mode (HGO=0)	_	—	_	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	_	10	_	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—		MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	_	1	_	MΩ	
R _S	Series resistor — low-frequency, low-power mode (HGO=0)	_	_	_	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	_	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	_	_	_	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)					
			0		kΩ	
V _{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)		0.6	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	_	V _{DD}	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	_	0.6	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	_	V _{DD}	_	V	

Table 14. Oscillator DC electrical specifications (continued)

1. V_{DD} =3.3 V, Temperature =25 °C

2. See crystal or resonator manufacturer's recommendation

3. C_x, C_y can be provided by using either the integrated capacitors or by using external components.

4. When low power mode is selected, R_F is integrated and must not be attached externally.

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
t _{nvmretd1k}	Data retention after up to 1 K cycles	20	100	_	years	
n _{nvmcycd}	Cycling endurance	10 K	50 K	_	cycles	2
	FlexRAM as	s EEPROM				
t _{nvmretee100}	Data retention up to 100% of write endurance	5	50		years	
t _{nvmretee10}	Data retention up to 10% of write endurance	20	100		years	
	Write endurance					3
n _{nvmwree16}	EEPROM backup to FlexRAM ratio = 16	35 K	175 K	—	writes	
n _{nvmwree128}	• EEPROM backup to FlexRAM ratio = 128	315 K	1.6 M	—	writes	
n _{nvmwree512}	• EEPROM backup to FlexRAM ratio = 512	1.27 M	6.4 M	—	writes	
n _{nvmwree4k}	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	—	writes	
n _{nvmwree8k}	• EEPROM backup to FlexRAM ratio = 8192	20 M	100 M	—	writes	

Table 21. NVM reliability specifications (continued)

 Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.

2. Cycling endurance represents number of program/erase cycles at -40°C \leq T_j \leq 125°C.

3. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup. Minimum and typical values assume all byte-writes to FlexRAM.

6.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the flash memory module to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

Writes_FlexRAM =
$$\frac{\text{EEPROM} - 2 \times \text{EEESIZE}}{\text{EEESIZE}} \times \text{Write}_\text{efficiency} \times n_{\text{nvmcycd}}$$

where

• Writes_FlexRAM — minimum number of writes to each FlexRAM location

- EEPROM allocated FlexNVM based on DEPART; entered with the Program Partition command
- EEESIZE allocated FlexRAM based on DEPART; entered with the Program Partition command
- Write_efficiency
 - 0.25 for 8-bit writes to FlexRAM
 - 0.50 for 16-bit or 32-bit writes to FlexRAM
- n_{nvmcycd} data flash cycling endurance (the following graph assumes 10,000 cycles)



Figure 8. EEPROM backup writes to FlexRAM

6.4.2 EzPort Switching Specifications

Table 22. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V

Table continues on the next page ...

Num	Description	Min.	Max.	Unit
EP1	EZP_CK frequency of operation (all commands except READ)	—	f _{SYS} /2	MHz
EP1a	EZP_CK frequency of operation (READ command)		f _{SYS} /8	MHz
EP2	EZP_CS negation to next EZP_CS assertion	2 x t _{EZP_CK}	_	ns
EP3	EZP_CS input valid to EZP_CK high (setup)	5	_	ns
EP4	EZP_CK high to $\overline{\text{EZP}_{CS}}$ input invalid (hold)	5		ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	_	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	_	ns
EP7	EZP_CK low to EZP_Q output valid		17	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	_	ns
EP9	EZP_CS negation to EZP_Q tri-state	_	12	ns







6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

6.6 Analog

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
C _{rate}	ADC conversion rate	16 bit modes No ADC hardware averaging	37.037	_	461.467	Ksps	5
		Continuous conversions enabled, subsequent conversion time					

Table 23. 16-bit ADC operating conditions (continued)

- Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- 2. DC potential difference.
- 3. This resistance is external to MCU. The analog source resistance should be kept as low as possible in order to achieve the best results. The results in this datasheet were derived from a system which has <8 Ω analog source resistance. The R_{AS}/ C_{AS} time constant should be kept to <1ns.
- 4. To use the maximum ADC conversion clock frequency, the ADHSC bit should be set and the ADLPC bit should be clear.
- 5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool: http://cache.freescale.com/ files/soft_dev_tools/software/app_software/converters/ADC_CALCULATOR_CNV.zip?fpsp=1



Figure 10. ADC input impedance equivalency diagram

6.6.1.2 16-bit ADC electrical characteristics Table 24. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I _{DDA_ADC}	Supply current		0.215		1.7	mA	3

Table continues on the next page ...

6.8.1 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	_	25	MHz	
DS1	DSPI_SCK output cycle time	2 x t _{BUS}	_	ns	
DS2	DSPI_SCK output high/low time	(t _{SCK} /2) – 2	(t _{SCK} /2) + 2	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	(t _{BUS} x 2) – 2	_	ns	1
DS4	DSPI_SCK to DSPI_PCSn invalid delay	(t _{BUS} x 2) – 2	_	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	_	8	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	0	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	14		ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	_	ns	

 Table 30.
 Master mode DSPI timing (limited voltage range)

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].

2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].



Figure 15. DSPI classic SPI timing — master mode

Table 31. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz

Table continues on the next page ...

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	_	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	_	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	_	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	29	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	_	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	_	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	_	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	21	ns

Table 35. I2S/SAI slave mode timing

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear



Figure 20. I2S/SAI timing — slave modes

6.8.5.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 36.I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes
(full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	_	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	_	ns
S7	I2S_TX_BCLK to I2S_TXD valid	_	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	45	_	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	_	ns



Figure 21. I2S/SAI timing — master modes

Table 37. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	_	ns

Table continues on the next page...

Table 37. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	_	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	3	_	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	63	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	_	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	_	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear





6.9 Human-machine interfaces (HMI)

6.9.1 TSI electrical specifications

Table 38. TSI electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{DDTSI}	Operating voltage	1.71	—	3.6	V	
C _{ELE}	Target electrode capacitance range	1	20	500	pF	1

Table continues on the next page ...

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to http://www.freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
64-pin LQFP	98ASS23234W
64-pin MAPBGA	98ASA00420D

8 Pinout

8.1 K10 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

64 MAP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
BGA												
A1	1	PTE0	DISABLED		PTE0		UART1_TX				RTC_CLKOUT	
B1	2	PTE1/ LLWU_P0	DISABLED		PTE1/ LLWU_P0		UART1_RX					
C5	3	VDD	VDD	VDD								
C4	4	VSS	VSS	VSS								
E1	5	PTE16	ADC0_SE4a	ADC0_SE4a	PTE16	SPI0_PCS0	UART2_TX	FTM_CLKIN0		FTM0_FLT3		
D1	6	PTE17	ADC0_SE5a	ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	FTM_CLKIN1		LPTMR0_ ALT3		
E2	7	PTE18	ADC0_SE6a	ADC0_SE6a	PTE18	SPI0_SOUT	UART2_CTS_ b	I2C0_SDA				
D2	8	PTE19	ADC0_SE7a	ADC0_SE7a	PTE19	SPI0_SIN	UART2_RTS_ b	I2C0_SCL				
G1	9	ADC0_DP0	ADC0_DP0	ADC0_DP0								
F1	10	ADC0_DM0	ADC0_DM0	ADC0_DM0								_
G2	11	ADC0_DP3	ADC0_DP3	ADC0_DP3								

Pinout

64 Map Bga	64 LQFP	Pin Name	Default	ALTO	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
F2	12	ADC0_DM3	ADC0_DM3	ADC0_DM3								
F4	13	VDDA	VDDA	VDDA								
G4	14	VREFH	VREFH	VREFH								
G3	15	VREFL	VREFL	VREFL								
F3	16	VSSA	VSSA	VSSA								
H1	17	VREF_OUT/ CMP1_IN5/ CMP0_IN5	VREF_OUT/ CMP1_IN5/ CMP0_IN5	VREF_OUT/ CMP1_IN5/ CMP0_IN5								
H2	18	CMP1_IN3/ ADC0_SE23	CMP1_IN3/ ADC0_SE23	CMP1_IN3/ ADC0_SE23								
H3	19	XTAL32	XTAL32	XTAL32								
H4	20	EXTAL32	EXTAL32	EXTAL32								
H5	21	VBAT	VBAT	VBAT								
D3	22	PTAO	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSI0_CH1	PTAO	UART0_CTS_ b/ UART0_COL_ b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
D4	23	PTA1	JTAG_TDI/ EZP_DI	TSI0_CH2	PTA1	UARTO_RX	FTM0_CH6				JTAG_TDI	EZP_DI
E5	24	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO	TSI0_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
D5	25	PTA3	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	UARTO_RTS_ b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
G5	26	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSI0_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
F5	27	PTA5	DISABLED		PTA5		FTM0_CH2			I2S0_TX_ BCLK	JTAG_TRST_ b	
H6	28	PTA12	DISABLED		PTA12		FTM1_CH0			I2S0_TXD0	FTM1_QD_ PHA	
G6	29	PTA13/ LLWU_P4	DISABLED		PTA13/ LLWU_P4		FTM1_CH1			I2S0_TX_FS	FTM1_QD_ PHB	
G7	30	VDD	VDD	VDD								
H7	31	VSS	VSS	VSS								
H8	32	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
G8	33	PTA19	XTALO	XTALO	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ ALT1		
F8	34	RESET_b	RESET_b	RESET_b								
F7	35	PTB0/ LLWU_P5	ADC0_SE8/ TSI0_CH0	ADC0_SE8/ TSI0_CH0	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_ PHA		
F6	36	PTB1	ADC0_SE9/ TSI0_CH6	ADC0_SE9/ TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_ PHB		
E7	37	PTB2	ADC0_SE12/ TSI0_CH7	ADC0_SE12/ TSI0_CH7	PTB2	I2C0_SCL	UARTO_RTS_ b			FTM0_FLT3		
E8	38	PTB3	ADC0_SE13/ TSI0_CH8	ADC0_SE13/ TSI0_CH8	PTB3	I2C0_SDA	UARTO_CTS_ b/			FTM0_FLT0		



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