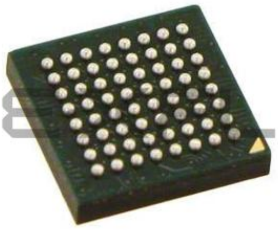
NXP USA Inc. - MK10DN64VMP5 Datasheet



What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 19x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LFBGA
Supplier Device Package	64-MAPBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk10dn64vmp5

Table of Contents

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	130	µA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

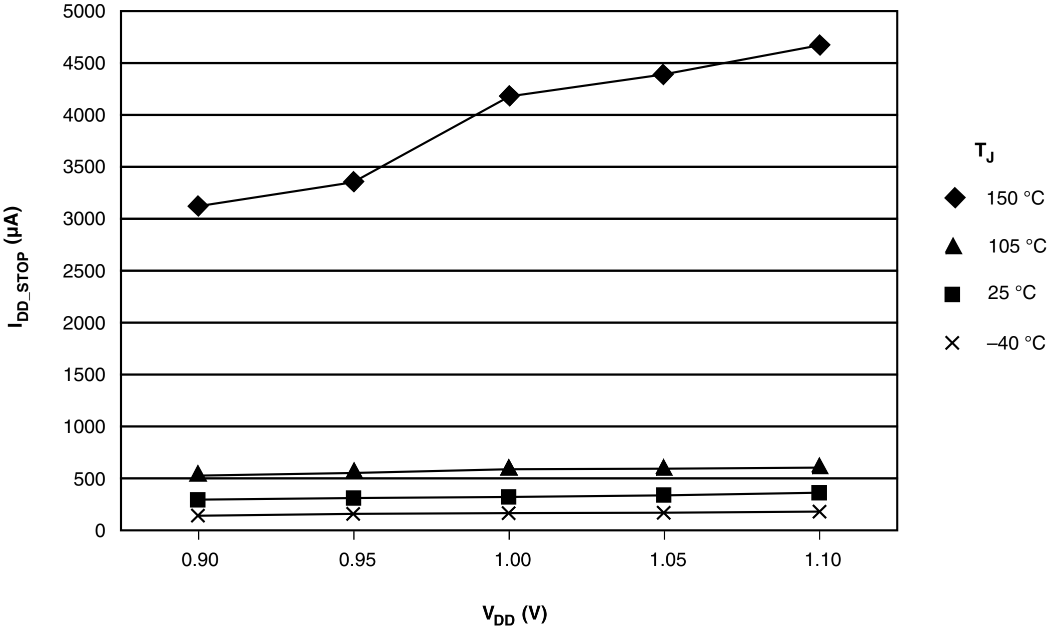
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

Table 2. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising thresholds are falling threshold + hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

Table 10. General switching specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	Port rise and fall time (low drive strength)				5
	• Slew disabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	12	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	6	ns	
	• Slew enabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	36	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	24	ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75pF load
5. 15pF load

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature	–40	105	°C

5.4.2 Thermal attributes

Board type	Symbol	Description	64 MAPBGA	64 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	107	65	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	56	46	°C/W	1, 3

Table continues on the next page...

6.1.1 JTAG electricals

Table 12. JTAG voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	5.5	V
J1	TCLK frequency of operation • JTAG • CJTAG	 — —	 10 5	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width • JTAG • CJTAG	 100 200	 — —	 ns ns ns
J4	TCLK rise and fall times	—	1	ns
J5	TMS input data setup time to TCLK rise • JTAG • CJTAG	53 112	— —	ns
J6	TDI input data setup time to TCLK rise	8	—	ns
J7	TMS input data hold time after TCLK rise • JTAG • CJTAG	3.4 3.4	— —	ns
J8	TDI input data hold time after TCLK rise	3.4	—	ns
J9	TCLK low to TMS data valid • JTAG • CJTAG	— —	48 85	ns
J10	TCLK low to TDO data valid	—	48	ns
J11	Output data hold/invalid time after clock edge[1]	—	3	ns

[1] They are common for JTAG and CJTAG. Input transition = 1 ns and Output load = 50pf

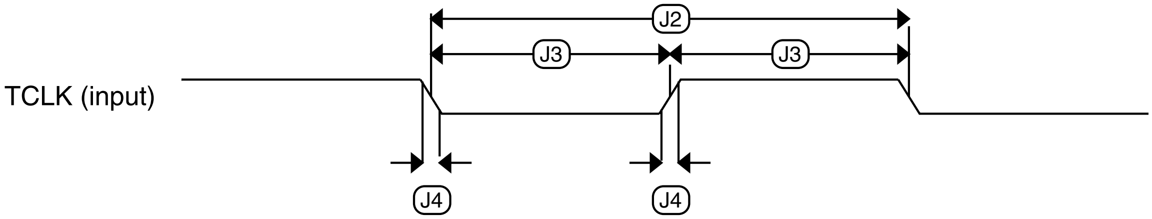


Figure 4. Test clock input timing

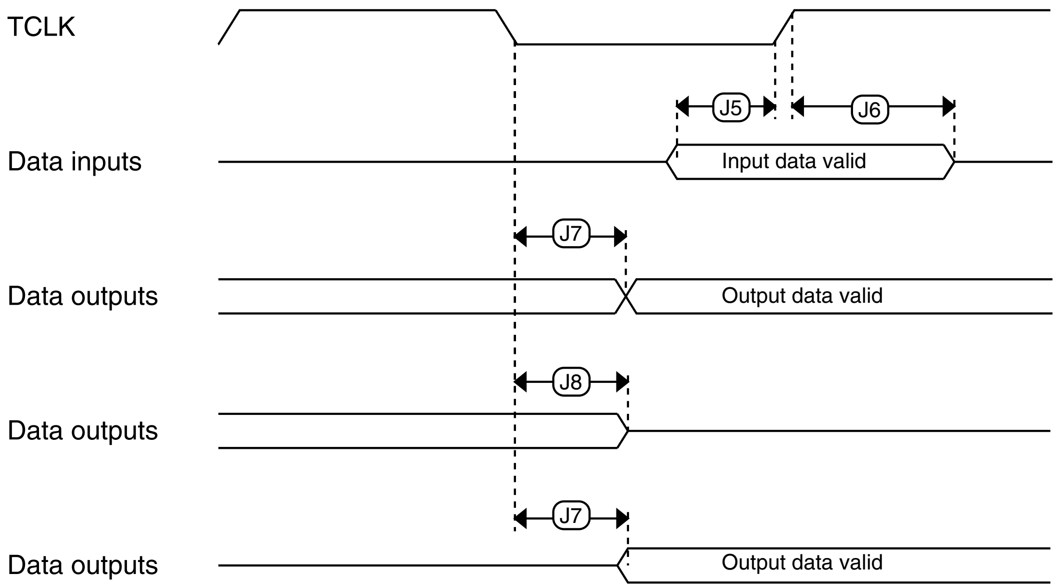


Figure 5. Boundary scan (JTAG) timing

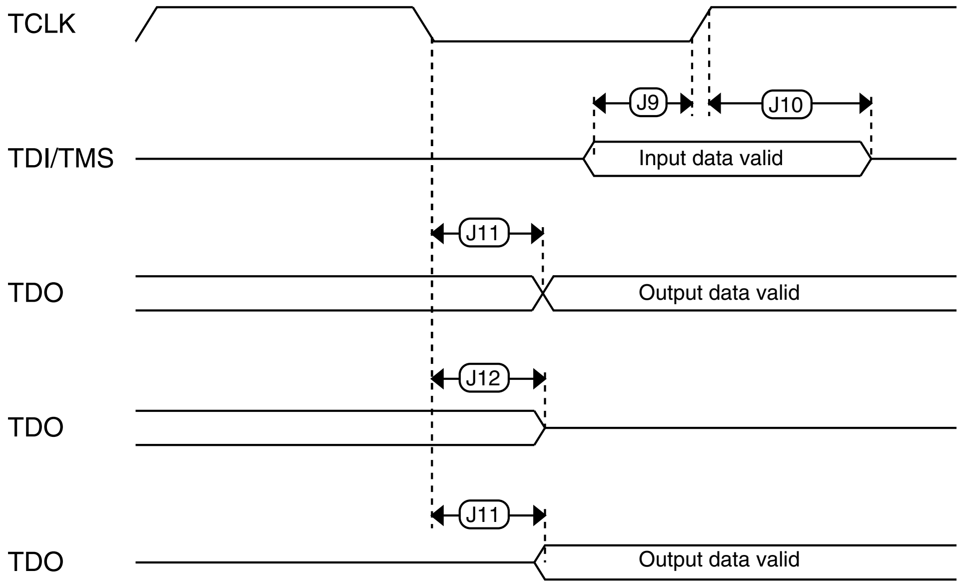


Figure 6. Test Access Port timing

Table 13. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) 732 × f_{fll_ref}	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f_{fll_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f_{fll_ref}	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{VCO} = 48 MHz • f_{VCO} = 98 MHz		— —	180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	6
	PLL						
f_{vco}	VCO operating frequency		48.0	—	100	MHz	
I_{pll}	PLL operating current • PLL @ 96 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 48)		—	1060	—	µA	7
I_{pll}	PLL operating current • PLL @ 48 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 24)		—	600	—	µA	7
f_{pll_ref}	PLL reference frequency range		2.0	—	4.0	MHz	
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 48 MHz • f_{vco} = 100 MHz		— —	120 50	— —	ps ps	8

Table continues on the next page...

Table 19. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
Word-write to FlexRAM for EEPROM operation						
$t_{eewr16bers}$	Word-write to erased FlexRAM location execution time	—	175	260	μs	
	Word-write to FlexRAM execution time:					
$t_{eewr16b8k}$	• 8 KB EEPROM backup	—	340	1700	μs	
$t_{eewr16b16k}$	• 16 KB EEPROM backup	—	385	1800	μs	
$t_{eewr16b32k}$	• 32 KB EEPROM backup	—	475	2000	μs	
Longword-write to FlexRAM for EEPROM operation						
$t_{eewr32bers}$	Longword-write to erased FlexRAM location execution time	—	360	540	μs	
	Longword-write to FlexRAM execution time:					
$t_{eewr32b8k}$	• 8 KB EEPROM backup	—	545	1950	μs	
$t_{eewr32b16k}$	• 16 KB EEPROM backup	—	630	2050	μs	
$t_{eewr32b32k}$	• 32 KB EEPROM backup	—	810	2250	μs	

1. Assumes 25MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

6.4.1.3 Flash high voltage current behaviors

Table 20. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

6.4.1.4 Reliability specifications

Table 21. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2
Data Flash						
$t_{nvmretd10k}$	Data retention after up to 10 K cycles	5	50	—	years	

Table continues on the next page...

- EEPROM — allocated FlexNVM based on DEPART; entered with the Program Partition command
- EEESIZE — allocated FlexRAM based on DEPART; entered with the Program Partition command
- Write_efficiency —
  - 0.25 for 8-bit writes to FlexRAM
  - 0.50 for 16-bit or 32-bit writes to FlexRAM
- $n_{nvmcycd}$ — data flash cycling endurance (the following graph assumes 10,000 cycles)

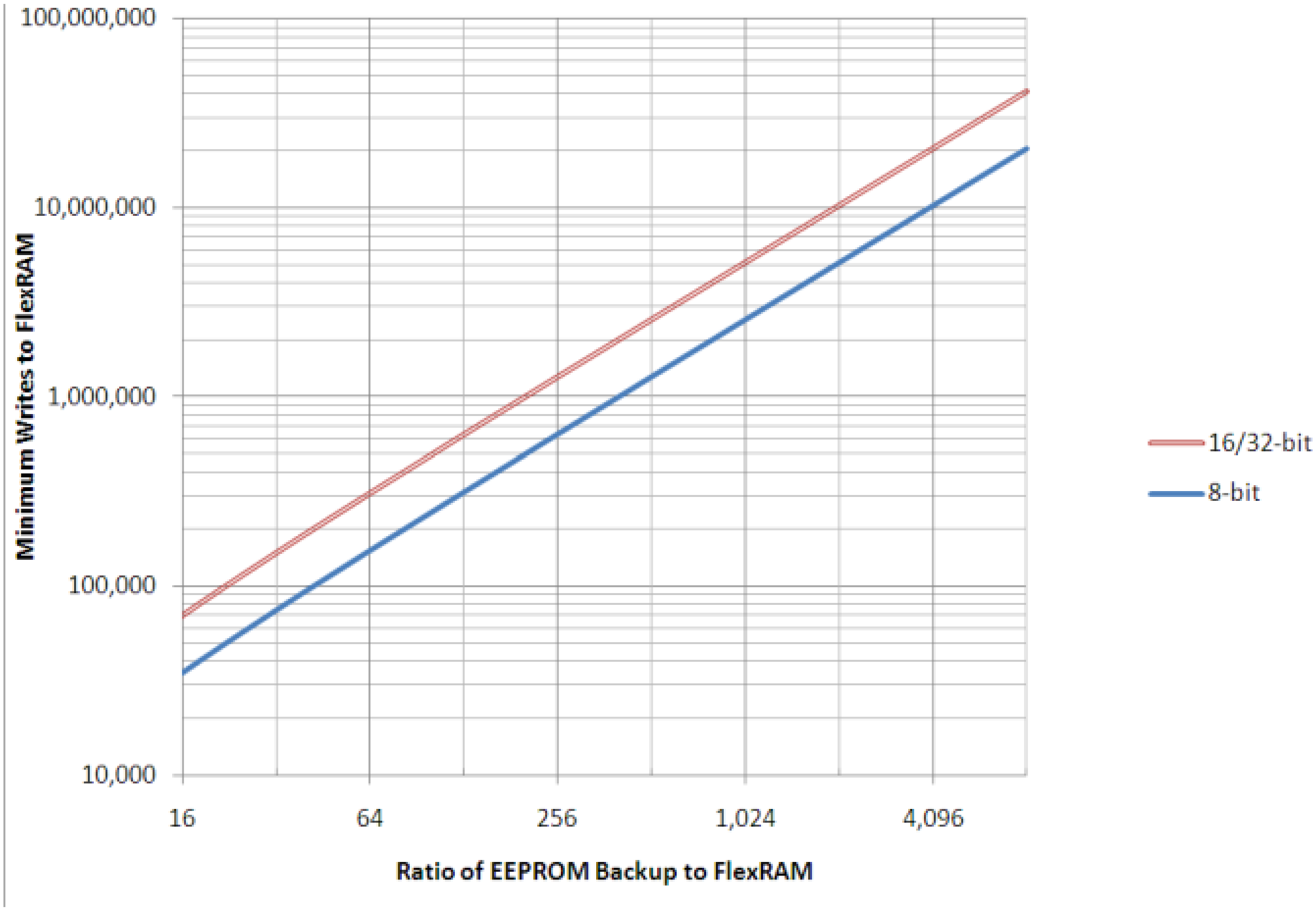


Figure 8. EEPROM backup writes to FlexRAM

6.4.2 EzPort Switching Specifications

Table 22. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V

Table continues on the next page...

Table 24. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
f_{ADACK}	ADC asynchronous clock source	• ADLPC=1, ADHSC=0 • ADLPC=1, ADHSC=1 • ADLPC=0, ADHSC=0 • ADLPC=0, ADHSC=1	1.2 3.0 2.4 4.4	2.4 4.0 5.2 6.2	3.9 7.3 6.1 9.5	MHz MHz MHz MHz	t_{ADACK} = 1/ f_{ADACK}
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12 bit modes • <12 bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12 bit modes • <12 bit modes	— —	±0.7 ±0.2	-1.1 to +1.9 -0.3 to 0.5	LSB[4]	5
INL	Integral non-linearity	• 12 bit modes • <12 bit modes	— —	±1.0 ±0.5	-2.7 to +1.9 -0.7 to +0.5	LSB[4]	5
E_{FS}	Full-scale error	• 12 bit modes • <12 bit modes	— —	-4 -1.4	-5.4 -1.8	LSB[4]	V_{ADIN} = V_{DDA} 5
E_Q	Quantization error	• 16 bit modes • ≤13 bit modes	— —	-1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16 bit differential mode • Avg=32 • Avg=4 16 bit single-ended mode • Avg=32 • Avg=4	12.8 11.9 12.2 11.4	14.5 13.8 13.9 13.1	— — — —	bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16 bit differential mode • Avg=32 16 bit single-ended mode • Avg=32	— —	–94 -85	— —	dB dB	7

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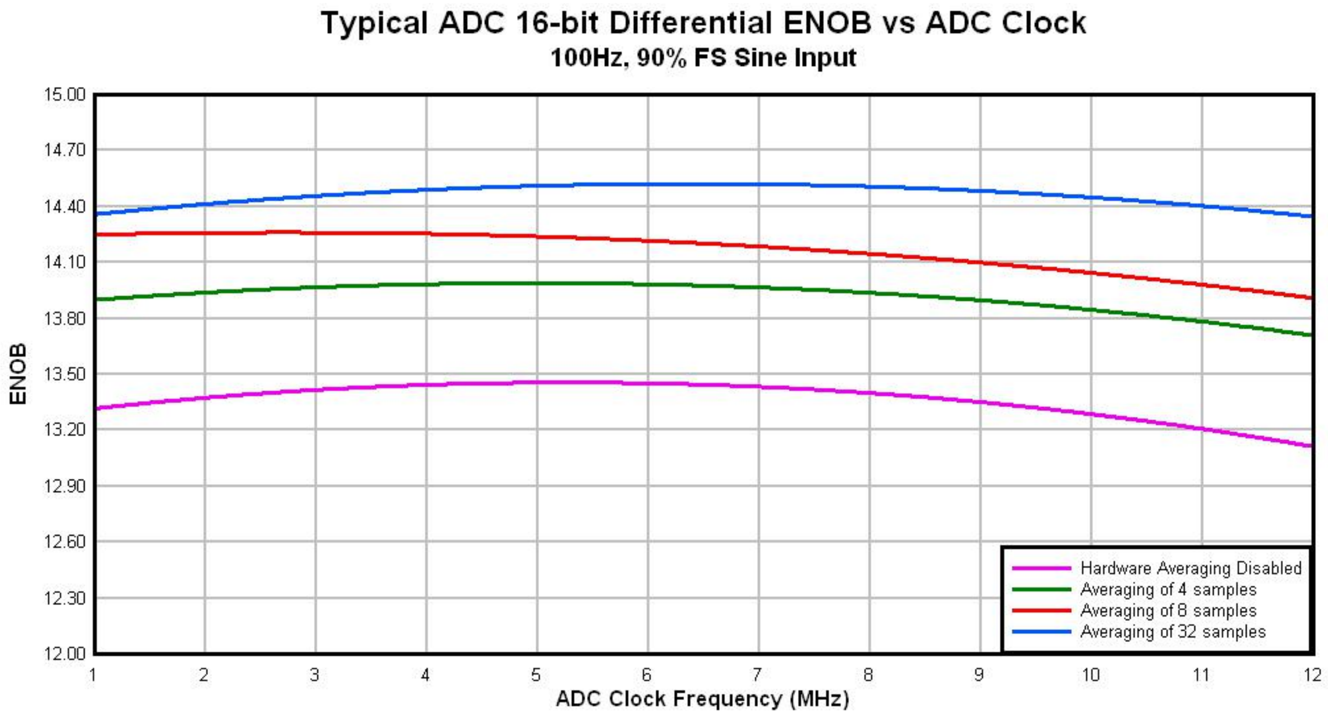

Figure 11. Typical ENOB vs. ADC_CLK for 16-bit differential mode

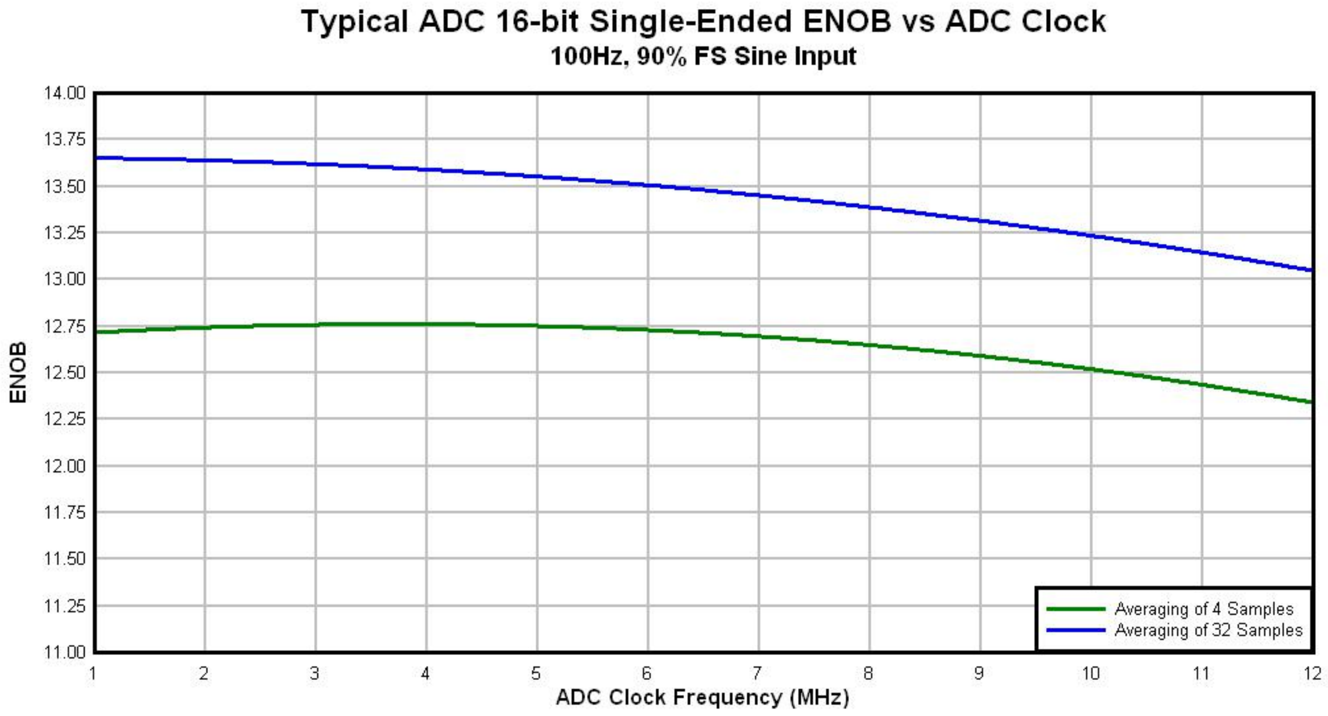

Figure 12. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

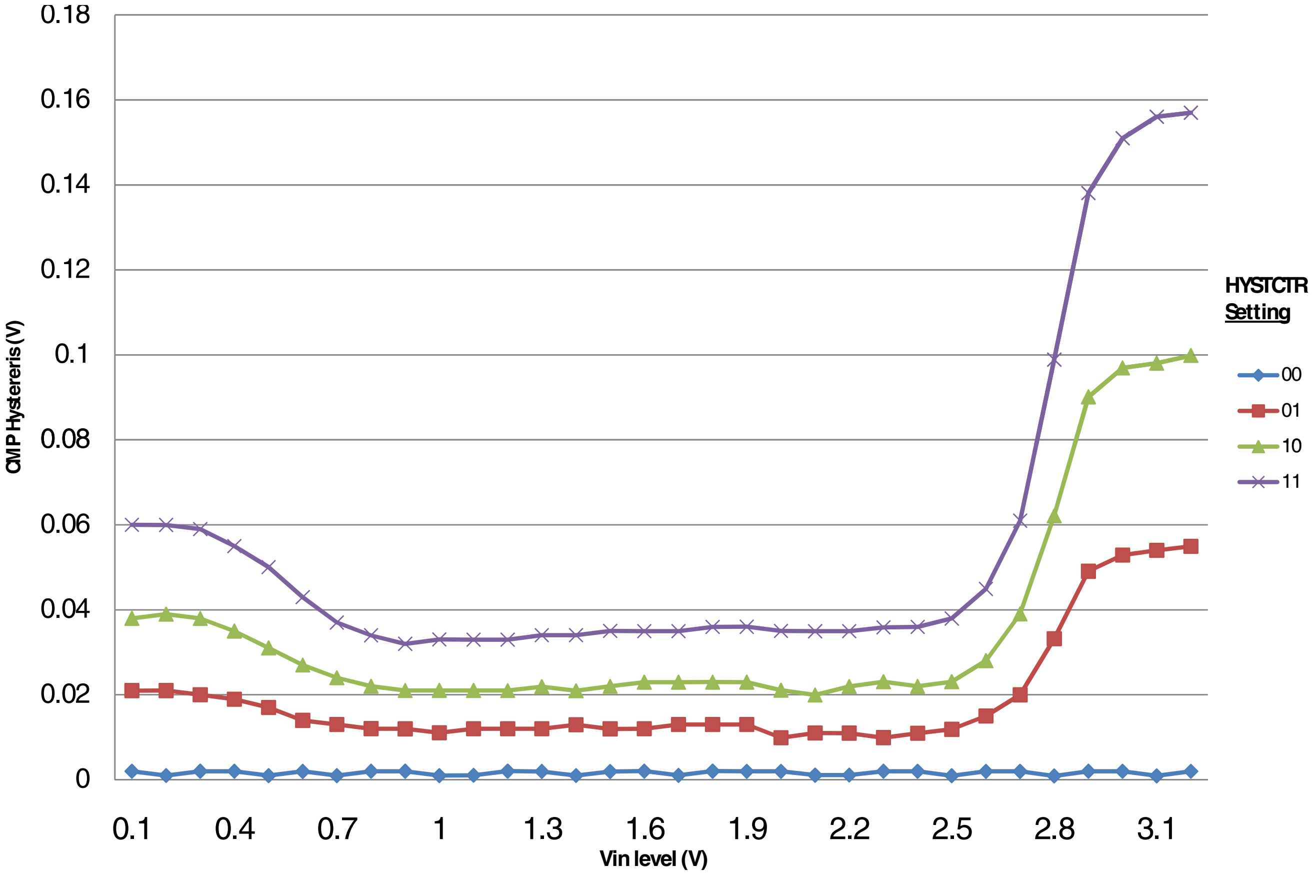

Figure 14. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=1)

6.6.3 Voltage reference electrical specifications

Table 26. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
T_A	Temperature	–40	105	°C	
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 27. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1915	1.195	1.1977	V	

Table continues on the next page...

6.8.1 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 30. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 2$	—	ns	1
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	$(t_{BUS} \times 2) - 2$	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	0	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	14	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

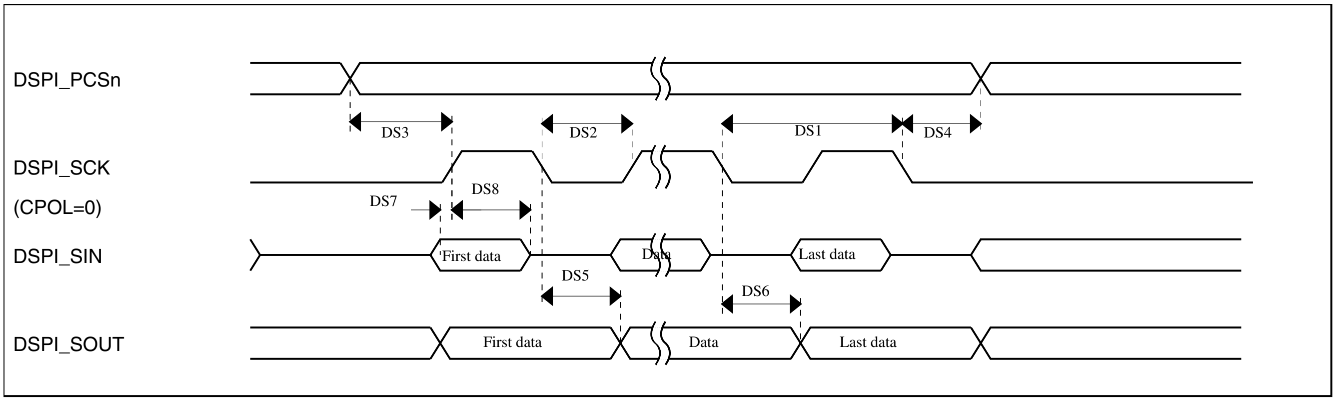

Figure 15. DSPI classic SPI timing — master mode

Table 31. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz

Table continues on the next page...

Table 31. Slave mode DSPI timing (limited voltage range) (continued)

Num	Description	Min.	Max.	Unit
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	14	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	14	ns

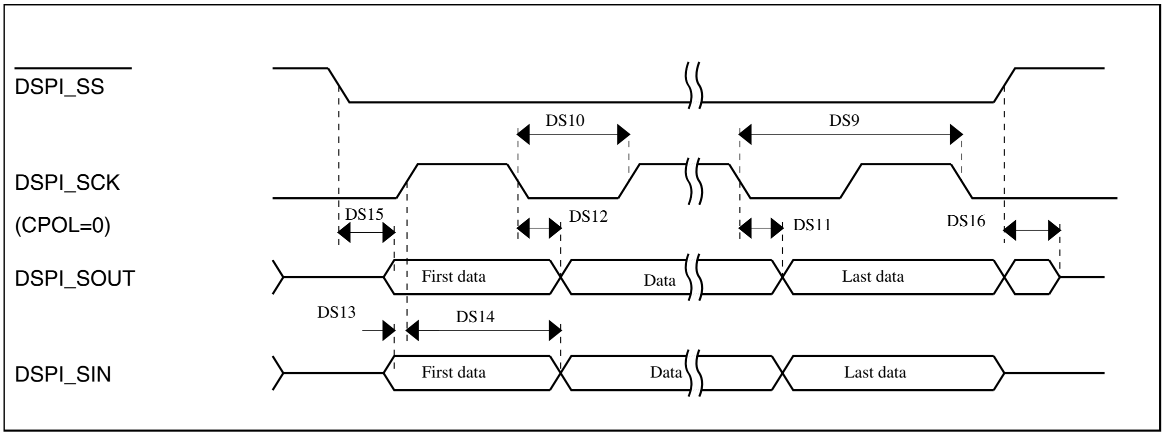

Figure 16. DSPI classic SPI timing — slave mode

6.8.2 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 32. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	4 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK/2}) + 4$	ns	

Table continues on the next page...

Table 36. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	45	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

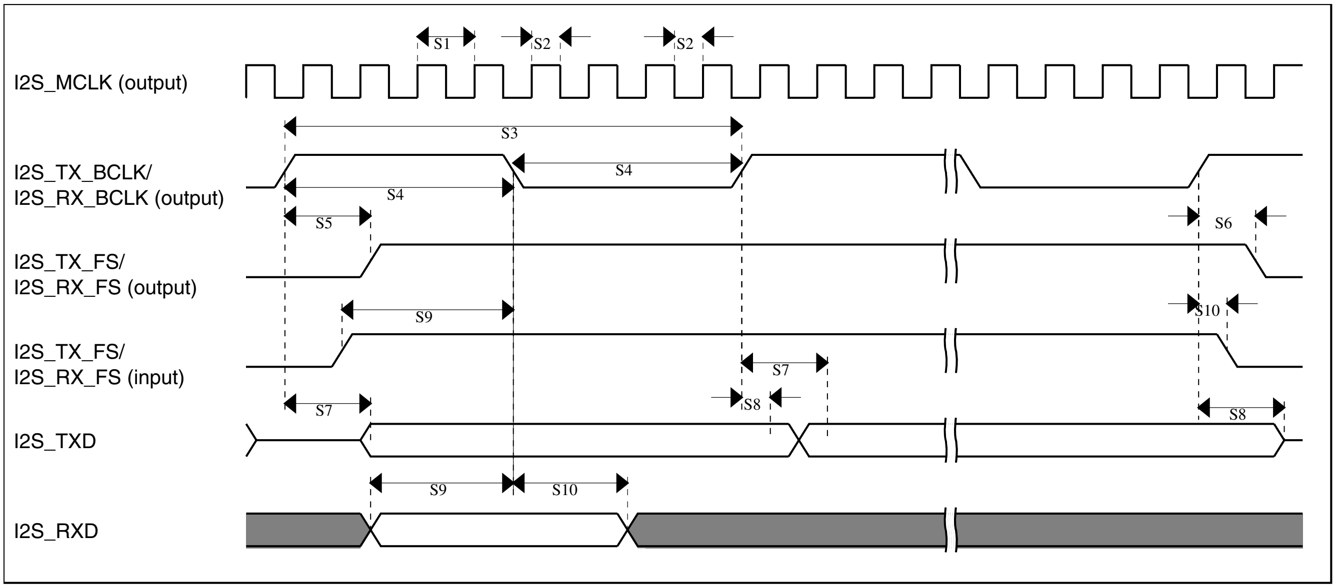

Figure 21. I2S/SAI timing — master modes

Table 37. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns

Table continues on the next page...

Table 38. TSI electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{REFmax}	Reference oscillator frequency	—	8	15	MHz	2, 3
f_{ELEmax}	Electrode oscillator frequency	—	1	1.8	MHz	2, 4
C_{REF}	Internal reference capacitor	—	1	—	pF	
V_{DELTA}	Oscillator delta voltage	—	500	—	mV	2, 5
I_{REF}	Reference oscillator current source base current • 2 μA setting (REFCHRG = 0) • 32 μA setting (REFCHRG = 15)	— —	2 36	3 50	μA	2, 6
I_{ELE}	Electrode oscillator current source base current • 2 μA setting (EXTCHRG = 0) • 32 μA setting (EXTCHRG = 15)	— —	2 36	3 50	μA	2, 7
Pres5	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	8
Pres20	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	9
Pres100	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	10
MaxSens	Maximum sensitivity	0.008	1.46	—	fF/count	11
Res	Resolution	—	—	16	bits	
T_{Con20}	Response time @ 20 pF	8	15	25	μs	12
I_{TSI_RUN}	Current added in run mode	—	55	—	μA	
I_{TSI_LP}	Low power mode current adder	—	1.3	2.5	μA	13

1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.
2. Fixed external capacitance of 20 pF.
3. REFCHRG = 2, EXTCHRG=0.
4. REFCHRG = 0, EXTCHRG = 10.
5. V_{DD} = 3.0 V.
6. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.
7. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current.
8. Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; Iext = 16.
9. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; Iext = 16.
10. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; Iext = 16.
11. Sensitivity defines the minimum capacitance change when a single count from the TSI module changes. Sensitivity depends on the configuration used. The documented values are provided as examples calculated for a specific configuration of operating conditions using the following equation: $(C_{ref} * I_{ext})/(I_{ref} * PS * NSCN)$

    The typical value is calculated with the following configuration:

    $I_{ext} = 6$ μA (EXTCHRG = 2), PS = 128, NSCN = 2, $I_{ref} = 16$ μA (REFCHRG = 7), C_{ref} = 1.0 pF

    The minimum value is calculated with the following configuration:

    $I_{ext} = 2$ μA (EXTCHRG = 0), PS = 128, NSCN = 32, $I_{ref} = 32$ μA (REFCHRG = 15), C_{ref} = 0.5 pF

    The highest possible sensitivity is the minimum value because it represents the smallest possible capacitance that can be measured by a single count.
12. Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, EXTCHRG = 7.
13. REFCHRG=0, EXTCHRG=4, PS=7, NSCN=0F, LPSCNITV=F, LPO is selected (1 kHz), and fixed external capacitance of 20 pF. Data is captured with an average of 7 periods window.

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to http://www.freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
64-pin LQFP	98ASS23234W
64-pin MAPBGA	98ASA00420D

8 Pinout

8.1 K10 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

64 MAP BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
A1	1	PTE0	DISABLED		PTE0		UART1_TX				RTC_CLKOUT	
B1	2	PTE1/ LLWU_P0	DISABLED		PTE1/ LLWU_P0		UART1_RX					
C5	3	VDD	VDD	VDD								
C4	4	VSS	VSS	VSS								
E1	5	PTE16	ADC0_SE4a	ADC0_SE4a	PTE16	SPI0_PCS0	UART2_TX	FTM_CLKIN0		FTM0_FLT3		
D1	6	PTE17	ADC0_SE5a	ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	FTM_CLKIN1		LPTMR0_ ALT3		
E2	7	PTE18	ADC0_SE6a	ADC0_SE6a	PTE18	SPI0_SOUT	UART2_CTS_ b	I2C0_SDA				
D2	8	PTE19	ADC0_SE7a	ADC0_SE7a	PTE19	SPI0_SIN	UART2_RTS_ b	I2C0_SCL				
G1	9	ADC0_DP0	ADC0_DP0	ADC0_DP0								
F1	10	ADC0_DM0	ADC0_DM0	ADC0_DM0								
G2	11	ADC0_DP3	ADC0_DP3	ADC0_DP3								

64 MAP BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
							UART0_COL_b					
E6	39	PTB16	TSI0_CH9	TSI0_CH9	PTB16		UART0_RX			EWM_IN		
D7	40	PTB17	TSI0_CH10	TSI0_CH10	PTB17		UART0_TX			EWM_OUT_b		
D6	41	PTB18	TSI0_CH11	TSI0_CH11	PTB18			I2S0_TX_BCLK				
C7	42	PTB19	TSI0_CH12	TSI0_CH12	PTB19			I2S0_TX_FS				
D8	43	PTC0	ADC0_SE14/TSI0_CH13	ADC0_SE14/TSI0_CH13	PTC0	SPI0_PCS4	PDB0_EXTRG					
C6	44	PTC1/LLWU_P6	ADC0_SE15/TSI0_CH14	ADC0_SE15/TSI0_CH14	PTC1/LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0		I2S0_TXD0		
B7	45	PTC2	ADC0_SE4b/CMP1_IN0/TSI0_CH15	ADC0_SE4b/CMP1_IN0/TSI0_CH15	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1		I2S0_TX_FS		
C8	46	PTC3/LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2		I2S0_TX_BCLK		
E3	47	VSS	VSS	VSS								
E4	48	VDD	VDD	VDD								
B8	49	PTC4/LLWU_P8	DISABLED		PTC4/LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT		
A8	50	PTC5/LLWU_P9	DISABLED		PTC5/LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0		CMP0_OUT		
A7	51	PTC6/LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_BCLK		I2S0_MCLK		
B6	52	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN		I2S0_RX_FS				
A6	53	PTC8	CMP0_IN2	CMP0_IN2	PTC8			I2S0_MCLK				
B5	54	PTC9	CMP0_IN3	CMP0_IN3	PTC9			I2S0_RX_BCLK				
B4	55	PTC10	DISABLED		PTC10			I2S0_RX_FS				
A5	56	PTC11/LLWU_P11	DISABLED		PTC11/LLWU_P11							
C3	57	PTD0/LLWU_P12	DISABLED		PTD0/LLWU_P12	SPI0_PCS0	UART2_RTS_b					
A4	58	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_b					
C2	59	PTD2/LLWU_P13	DISABLED		PTD2/LLWU_P13	SPI0_SOUT	UART2_RX					
B3	60	PTD3	DISABLED		PTD3	SPI0_SIN	UART2_TX					
A3	61	PTD4/LLWU_P14	DISABLED		PTD4/LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4		EWM_IN		
C1	62	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_b/UART0_COL_b	FTM0_CH5		EWM_OUT_b		
B2	63	PTD6/LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6		FTM0_FLT0		

64 MAP BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
A2	64	PTD7	DISABLED		PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		

8.2 K10 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.