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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | DMA, I²S, LVD, POR, PWM, WDT |
| Number of I/O | 44 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 19x16b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mk10dx128vlh5 |

# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.freescale.com and perform a part number search for the following device numbers: PK10 and MK10 .

# 2 Part identification

## 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

## 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

| Field | Description | Values |
|---|---|---|
| Q | Qualification status | • M = Fully qualified, general market flow<br>• P = Prequalification |
| K## | Kinetis family | • K10 |
| A | Key attribute | • D = Cortex-M4 w/ DSP<br>• F = Cortex-M4 w/ DSP and FPU |
| M | Flash memory type | • N = Program flash only<br>• X = Program flash and FlexMemory |

*Table continues on the next page...*

## 3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

### 3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | 0.9 | 1.1 | V |

## 3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

### 3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $I_{WP}$ | Digital I/O weak pullup/ pulldown current | 10 | 130 | µA |

## 3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

### 3.3.1 Example

This is an example of an attribute:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| CIN_D | Input capacitance: digital pins | — | 7 | pF |

## 3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

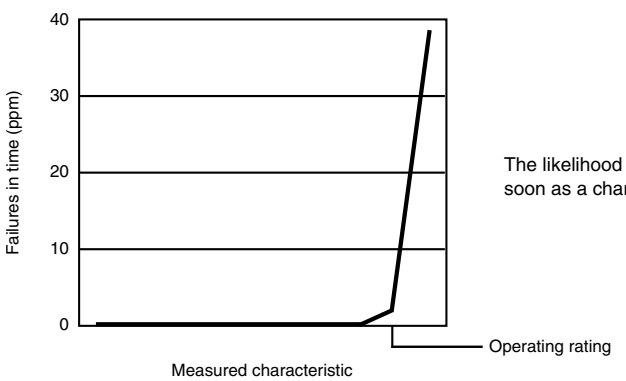
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

### 3.4.1 Example

This is an example of an operating rating:

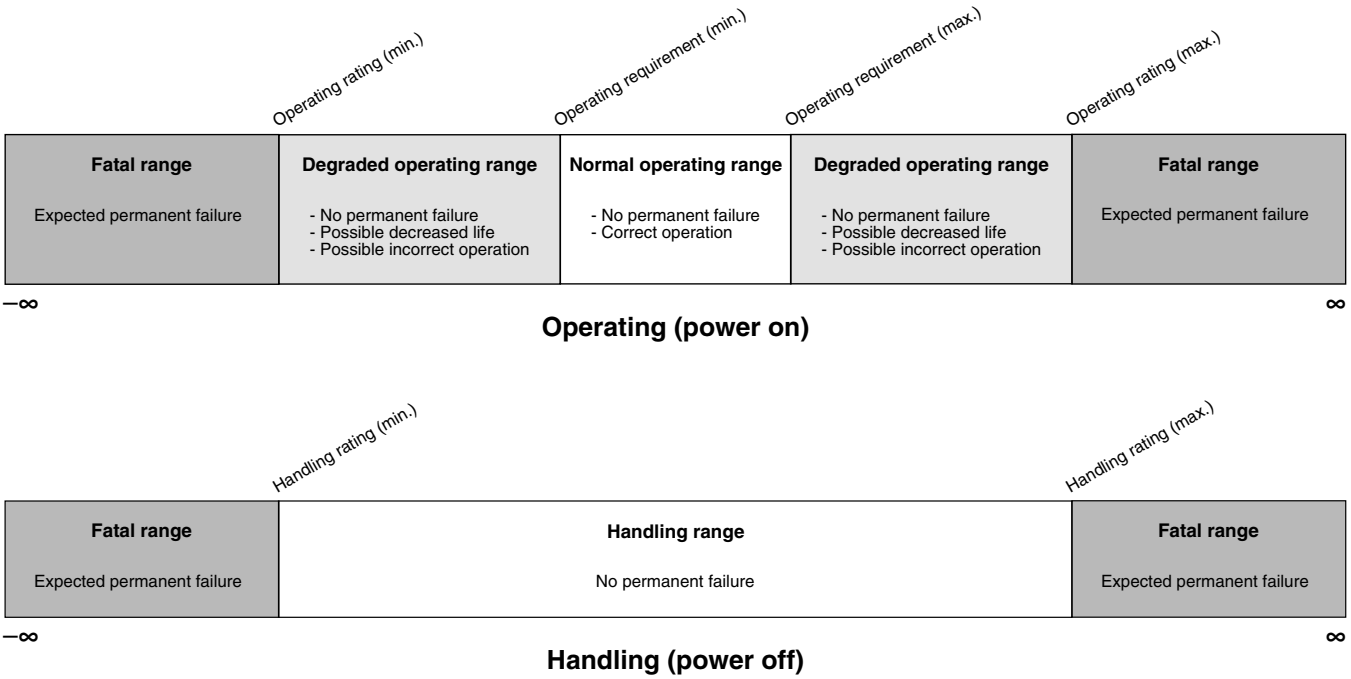
| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | –0.3 | 1.2 | V |

## 3.5 Result of exceeding a rating




The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

## 3.6 Relationship between ratings and operating requirements




## 3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

## 3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

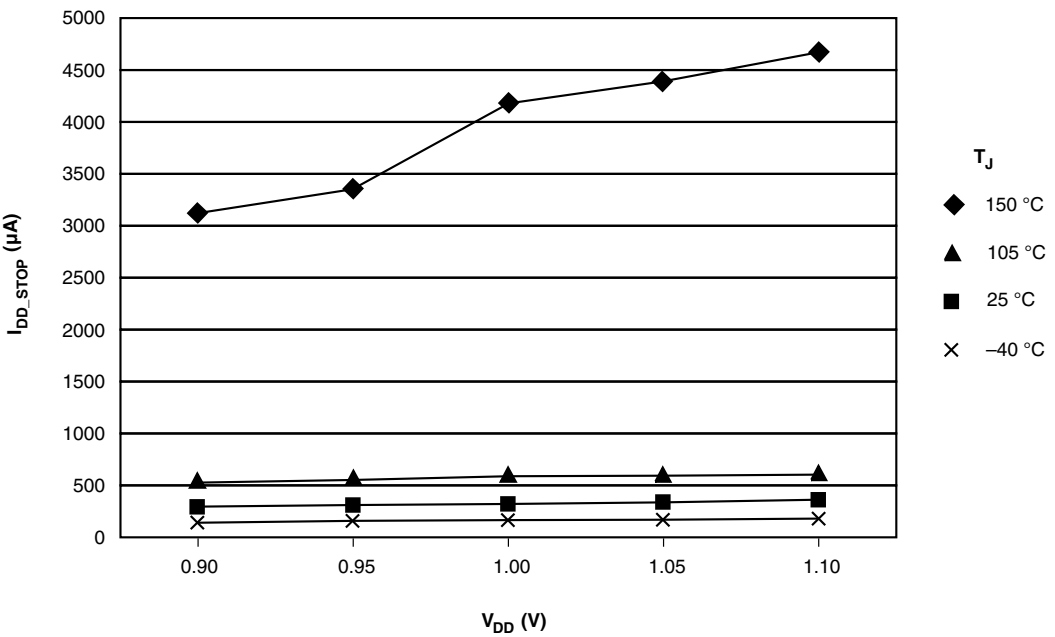
### 3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{WP}$ | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | µA |

### 3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:




## 3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient temperature | 25 | °C |
| $V_{DD}$ | 3.3 V supply voltage | 3.3 | V |

### Table 5. Power mode transition operating behaviors

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $t_{POR}$ | After a POR event, amount of time from the point $V_{DD}$ reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip. | — | 300 | µs | 1 |
| | • VLLS0 → RUN | — | 130 | µs | |
| | • VLLS1 → RUN | — | 130 | µs | |
| | • VLLS2 → RUN | — | 70 | µs | |
| | • VLLS3 → RUN | — | 70 | µs | |
| | • LLS → RUN | — | 6 | µs | |
| | • VLPS → RUN | — | 5.2 | µs | |
| | • STOP → RUN | — | 5.2 | µs | |

1. Normal boot (FTFL_OPT[LPBOOT]=1)

## 5.2.5 Power consumption operating behaviors

### Table 6. Power consumption operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DDA}$ | Analog supply current | — | — | See note | mA | 1 |
| $I_{DD\_RUN}$ | Run mode current — all peripheral clocks disabled, code executing from flash | | | | | 2 |
| | • @ 1.8V | — | 13.7 | 15.1 | mA | |
| | • @ 3.0V | — | 13.9 | 15.3 | mA | |
| $I_{DD\_RUN}$ | Run mode current — all peripheral clocks enabled, code executing from flash | | | | | 3, 4 |
| | • @ 1.8V | — | 16.1 | 18.2 | mA | |
| | • @ 3.0V | — | 16.3 | 17.7 | mA | |
| | • @ 25°C | — | 16.7 | 18.4 | mA | |
| | • @ 125°C | | | | | |
| $I_{DD\_WAIT}$ | Wait mode high frequency current at 3.0 V — all peripheral clocks disabled | — | 7.5 | 8.4 | mA | 2 |
| $I_{DD\_WAIT}$ | Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled | — | 5.6 | 6.4 | mA | 5 |

*Table continues on the next page...*

emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. $V_{DD}$ = 3.3 V, $T_A$ = 25 °C, $f_{OSC}$ = 12 MHz (crystal), $f_{SYS}$ = 48 MHz, $f_{BUS}$ = 48MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

### 5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to http://www.freescale.com.
2. Perform a keyword search for "EMC design."

### 5.2.8 Capacitance attributes

**Table 8. Capacitance attributes**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_{IN\_A}$ | Input capacitance: analog pins | — | 7 | pF |
| $C_{IN\_D}$ | Input capacitance: digital pins | — | 7 | pF |

## 5.3 Switching specifications

### 5.3.1 Device clock specifications

**Table 9. Device clock specifications**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| Normal run mode | | | | | |
| $f_{SYS}$ | System and core clock | — | 50 | MHz | |
| $f_{BUS}$ | Bus clock | — | 50 | MHz | |
| $f_{FLASH}$ | Flash clock | — | 25 | MHz | |
| $f_{LPTMR}$ | LPTMR clock | — | 25 | MHz | |
| VLPR mode[1] | | | | | |
| $f_{SYS}$ | System and core clock | — | 4 | MHz | |
| $f_{BUS}$ | Bus clock | — | 4 | MHz | |
| $f_{FLASH}$ | Flash clock | — | 1 | MHz | |
| $f_{ERCLK}$ | External reference clock | — | 16 | MHz | |

*Table continues on the next page...*

**Table 9. Device clock specifications (continued)**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $f_{LPTMR\_pin}$ | LPTMR clock | — | 25 | MHz | |
| $f_{LPTMR\_ERCLK}$ | LPTMR external reference clock | — | 16 | MHz | |
| $f_{I2S\_MCLK}$ | I2S master clock | — | 12.5 | MHz | |
| $f_{I2S\_BCLK}$ | I2S bit clock | — | 4 | MHz | |

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

## 5.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CMT, and $I^2C$ signals.

**Table 10. General switching specifications**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5 | — | Bus clock cycles | 1, 2 |
| | GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path | 100 | — | ns | 3 |
| | GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path | 50 | — | ns | 3 |
| | External reset pulse width (digital glitch filter disabled) | 100 | — | ns | 3 |
| | Mode select ($\overline{EZP\_CS}$) hold time after reset deassertion | 2 | — | Bus clock cycles | |
| | Port rise and fall time (high drive strength)<br>• Slew disabled<br>• $1.71 \le V_{DD} \le 2.7V$<br>• $2.7 \le V_{DD} \le 3.6V$<br>• Slew enabled<br>• $1.71 \le V_{DD} \le 2.7V$<br>• $2.7 \le V_{DD} \le 3.6V$ | <br><br><br>—<br>—<br><br>—<br>— | <br><br><br>13<br><br>7<br><br>36<br>24 | <br><br><br>ns<br>ns<br><br>ns<br>ns | 4 |

*Table continues on the next page...*

| Board type | Symbol | Description | 64 MAPBGA | 64 LQFP | Unit | Notes |
|---|---|---|---|---|---|---|
| Single-layer (1s) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./ min. air speed) | 90 | 53 | °C/W | 1,3 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./ min. air speed) | 51 | 40 | °C/W | , |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 31 | 28 | °C/W | 5 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 31 | 15 | °C/W | 6 |
| — | $\Psi_{JT}$ | Thermal characterization parameter, junction to package top outside center (natural convection) | 6 | 3 | °C/W | 7 |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. For the LQFP, the board meets the JESD51-3 specification. For the MAPBGA, the board meets the JESD51-9 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
5. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
6. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
7. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

# 6 Peripheral operating requirements and behaviors

## 6.1 Core modules

### 6.1.1 JTAG electricals

**Table 12. JTAG voltage range electricals**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 2.7 | 5.5 | V |
| J1 | TCLK frequency of operation<br>• JTAG<br>• CJTAG | <br>—<br>— | <br>10<br>5 | MHz |
| J2 | TCLK cycle period | 1/J1 | — | ns |
| J3 | TCLK clock pulse width<br>• JTAG<br>• CJTAG | <br>100<br>200 | <br>—<br>— | <br>ns<br>ns<br>ns |
| J4 | TCLK rise and fall times | — | 1 | ns |
| J5 | TMS input data setup time to TCLK rise<br>• JTAG<br>• CJTAG | <br>53<br>112 | <br>—<br>— | ns |
| J6 | TDI input data setup time to TCLK rise | 8 | — | ns |
| J7 | TMS input data hold time after TCLK rise<br>• JTAG<br>• CJTAG | <br>3.4<br>3.4 | <br>—<br>— | ns |
| J8 | TDI input data hold time after TCLK rise | 3.4 | — | ns |
| J9 | TCLK low to TMS data valid<br>• JTAG<br>• CJTAG | <br>—<br>— | <br>48<br>85 | ns |
| J10 | TCLK low to TDO data valid | — | 48 | ns |
| J11 | Output data hold/invalid time after clock edge[1] | — | 3 | ns |

1. They are common for JTAG and CJTAG. Input transition = 1 ns and Output load = 50pf

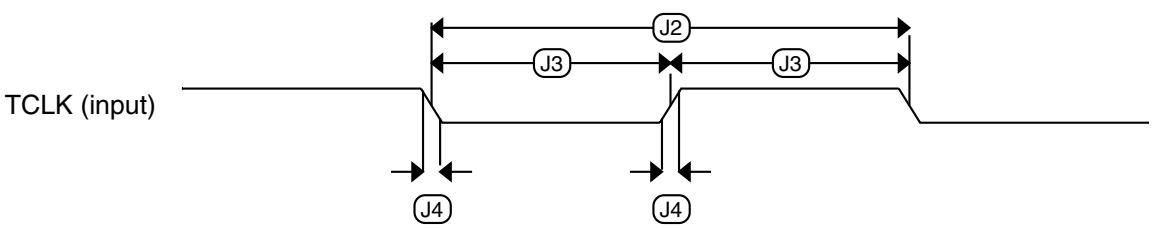



**Figure 4. Test clock input timing**

## Table 13. MCG specifications (continued)

| Symbol | Description | | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $f_{fll\_ref}$ | FLL reference frequency range | | 31.25 | — | 39.0625 | kHz | |
| $f_{dco}$ | DCO output frequency range | Low range (DRS=00)<br>640 × $f_{fll\_ref}$ | 20 | 20.97 | 25 | MHz | 2, 3 |
| | | Mid range (DRS=01)<br>1280 × $f_{fll\_ref}$ | 40 | 41.94 | 50 | MHz | |
| | | Mid-high range (DRS=10)<br>1920 × $f_{fll\_ref}$ | 60 | 62.91 | 75 | MHz | |
| | | High range (DRS=11)<br>2560 × $f_{fll\_ref}$ | 80 | 83.89 | 100 | MHz | |
| $f_{dco\_t\_DMX32}$ | DCO output frequency | Low range (DRS=00)<br>732 × $f_{fll\_ref}$ | — | 23.99 | — | MHz | 4, 5 |
| | | Mid range (DRS=01)<br>1464 × $f_{fll\_ref}$ | — | 47.97 | — | MHz | |
| | | Mid-high range (DRS=10)<br>2197 × $f_{fll\_ref}$ | — | 71.99 | — | MHz | |
| | | High range (DRS=11)<br>2929 × $f_{fll\_ref}$ | — | 95.98 | — | MHz | |
| $J_{cyc\_fll}$ | FLL period jitter<br>• $f_{VCO}$ = 48 MHz<br>• $f_{VCO}$ = 98 MHz | | —<br>— | 180<br>150 | —<br>— | ps | |
| $t_{fll\_acquire}$ | FLL target frequency acquisition time | | — | — | 1 | ms | 6 |
| PLL | | | | | | | |
| $f_{vco}$ | VCO operating frequency | | 48.0 | — | 100 | MHz | |
| $I_{pll}$ | PLL operating current<br>• PLL @ 96 MHz ($f_{osc\_hi\_1}$ = 8 MHz, $f_{pll\_ref}$ = 2 MHz, VDIV multiplier = 48) | | — | 1060 | — | µA | 7 |
| $I_{pll}$ | PLL operating current<br>• PLL @ 48 MHz ($f_{osc\_hi\_1}$ = 8 MHz, $f_{pll\_ref}$ = 2 MHz, VDIV multiplier = 24) | | — | 600 | — | µA | 7 |
| $f_{pll\_ref}$ | PLL reference frequency range | | 2.0 | — | 4.0 | MHz | |
| $J_{cyc\_pll}$ | PLL period jitter (RMS)<br>• $f_{vco}$ = 48 MHz<br>• $f_{vco}$ = 100 MHz | | —<br>— | 120<br>50 | —<br>— | ps<br>ps | 8 |

*Table continues on the next page...*

**Table 19. Flash command timing specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | Word-write to FlexRAM for EEPROM operation | | | | | |
| $t_{eewr16bers}$ | Word-write to erased FlexRAM location execution time | — | 175 | 260 | µs | |
| | Word-write to FlexRAM execution time: | | | | | |
| $t_{eewr16b8k}$ | • 8 KB EEPROM backup | — | 340 | 1700 | µs | |
| $t_{eewr16b16k}$ | • 16 KB EEPROM backup | — | 385 | 1800 | µs | |
| $t_{eewr16b32k}$ | • 32 KB EEPROM backup | — | 475 | 2000 | µs | |
| | Longword-write to FlexRAM for EEPROM operation | | | | | |
| $t_{eewr32bers}$ | Longword-write to erased FlexRAM location execution time | — | 360 | 540 | µs | |
| | Longword-write to FlexRAM execution time: | | | | | |
| $t_{eewr32b8k}$ | • 8 KB EEPROM backup | — | 545 | 1950 | µs | |
| $t_{eewr32b16k}$ | • 16 KB EEPROM backup | — | 630 | 2050 | µs | |
| $t_{eewr32b32k}$ | • 32 KB EEPROM backup | — | 810 | 2250 | µs | |

1. Assumes 25MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

### 6.4.1.3 Flash high voltage current behaviors

**Table 20. Flash high voltage current behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{DD\_PGM}$ | Average current adder during high voltage flash programming operation | — | 2.5 | 6.0 | mA |
| $I_{DD\_ERS}$ | Average current adder during high voltage flash erase operation | — | 1.5 | 4.0 | mA |

### 6.4.1.4 Reliability specifications

**Table 21. NVM reliability specifications**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | Program Flash | | | | | |
| $t_{nvmretp10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | |
| $t_{nvmretp1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | |
| $n_{nvmcycp}$ | Cycling endurance | 10 K | 50 K | — | cycles | 2 |
| | Data Flash | | | | | |
| $t_{nvmretd10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | |

*Table continues on the next page...*

- EEPROM — allocated FlexNVM based on DEPART; entered with the Program Partition command
- EEESIZE — allocated FlexRAM based on DEPART; entered with the Program Partition command
- Write_efficiency —
  - 0.25 for 8-bit writes to FlexRAM
  - 0.50 for 16-bit or 32-bit writes to FlexRAM
- $n_{nvmcycd}$ — data flash cycling endurance (the following graph assumes 10,000 cycles)

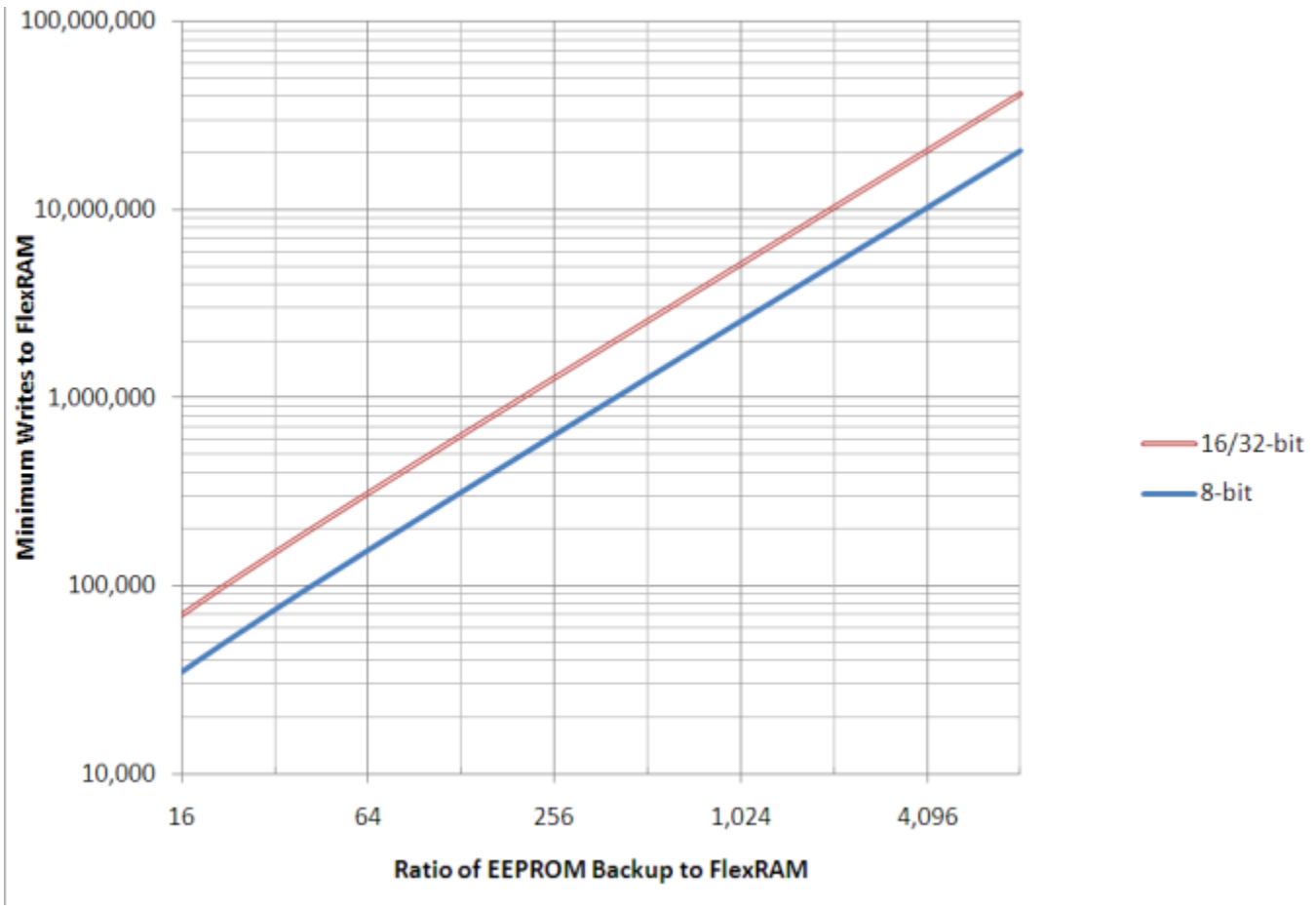



**Figure 8. EEPROM backup writes to FlexRAM**

## 6.4.2 EzPort Switching Specifications

**Table 22. EzPort switching specifications**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |

*Table continues on the next page...*

**Table 22. EzPort switching specifications (continued)**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| EP1 | EZP_CK frequency of operation (all commands except READ) | — | $f_{SYS}/2$ | MHz |
| EP1a | EZP_CK frequency of operation (READ command) | — | $f_{SYS}/8$ | MHz |
| EP2 | $\overline{\text{EZP\_CS}}$ negation to next $\overline{\text{EZP\_CS}}$ assertion | 2 x $t_{EZP\_CK}$ | — | ns |
| EP3 | $\overline{\text{EZP\_CS}}$ input valid to EZP_CK high (setup) | 5 | — | ns |
| EP4 | EZP_CK high to $\overline{\text{EZP\_CS}}$ input invalid (hold) | 5 | — | ns |
| EP5 | EZP_D input valid to EZP_CK high (setup) | 2 | — | ns |
| EP6 | EZP_CK high to EZP_D input invalid (hold) | 5 | — | ns |
| EP7 | EZP_CK low to EZP_Q output valid | — | 17 | ns |
| EP8 | EZP_CK low to EZP_Q output invalid (hold) | 0 | — | ns |
| EP9 | $\overline{\text{EZP\_CS}}$ negation to EZP_Q tri-state | — | 12 | ns |

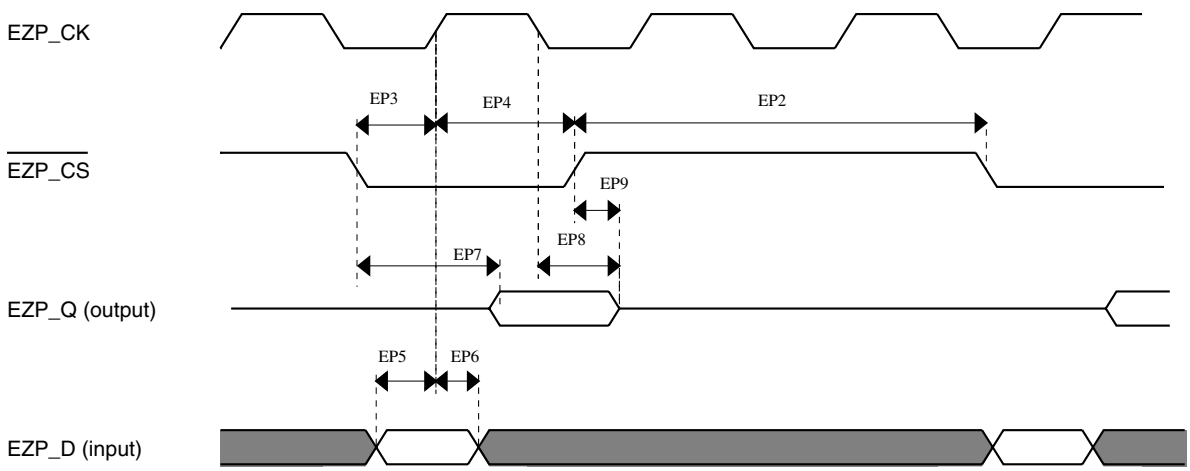



**Figure 9. EzPort Timing Diagram**

## 6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

## 6.6 Analog

## 6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 23 and Table 24 are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

### 6.6.1.1 16-bit ADC operating conditions

**Table 23. 16-bit ADC operating conditions**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| $\Delta V_{DDA}$ | Supply voltage | Delta to $V_{DD}$ ($V_{DD}$-$V_{DDA}$) | -100 | 0 | +100 | mV | 2 |
| $\Delta V_{SSA}$ | Ground voltage | Delta to $V_{SS}$ ($V_{SS}$-$V_{SSA}$) | -100 | 0 | +100 | mV | 2 |
| $V_{REFH}$ | ADC reference voltage high | | 1.13 | $V_{DDA}$ | $V_{DDA}$ | V | |
| $V_{REFL}$ | Reference voltage low | | $V_{SSA}$ | $V_{SSA}$ | $V_{SSA}$ | V | |
| $V_{ADIN}$ | Input voltage | | $V_{REFL}$ | — | $V_{REFH}$ | V | |
| $C_{ADIN}$ | Input capacitance | • 16 bit modes<br>• 8/10/12 bit modes | —<br>— | 8<br>4 | 10<br>5 | pF | |
| $R_{ADIN}$ | Input resistance | | — | 2 | 5 | kΩ | |
| $R_{AS}$ | Analog source resistance | 13/12 bit modes<br>$f_{ADCK}$ < 4MHz | — | — | 5 | kΩ | 3 |
| $f_{ADCK}$ | ADC conversion clock frequency | ≤ 13 bit modes | 1.0 | — | 18.0 | MHz | 4 |
| $f_{ADCK}$ | ADC conversion clock frequency | 16 bit modes | 2.0 | — | 12.0 | MHz | 4 |
| $C_{rate}$ | ADC conversion rate | ≤ 13 bit modes<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time | 20.000 | — | 818.330 | Ksps | 5 |

*Table continues on the next page...*

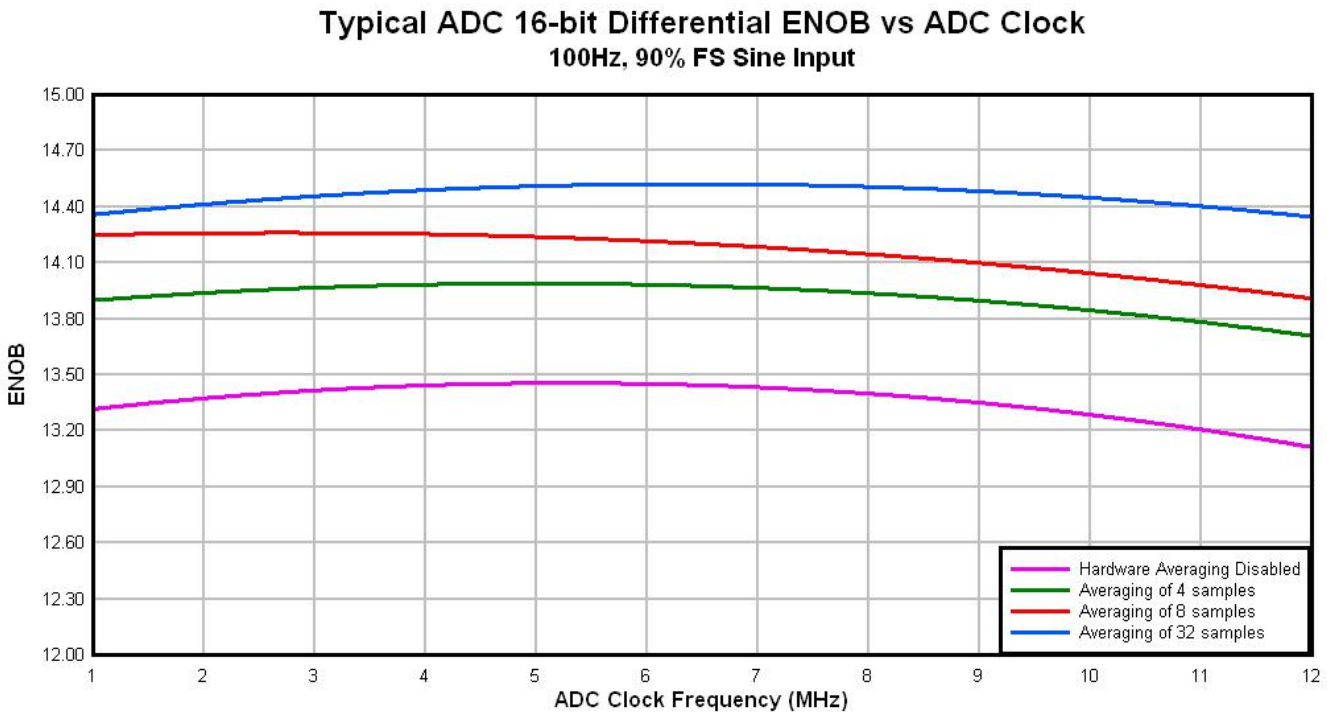



**Figure 11. Typical ENOB vs. ADC_CLK for 16-bit differential mode**

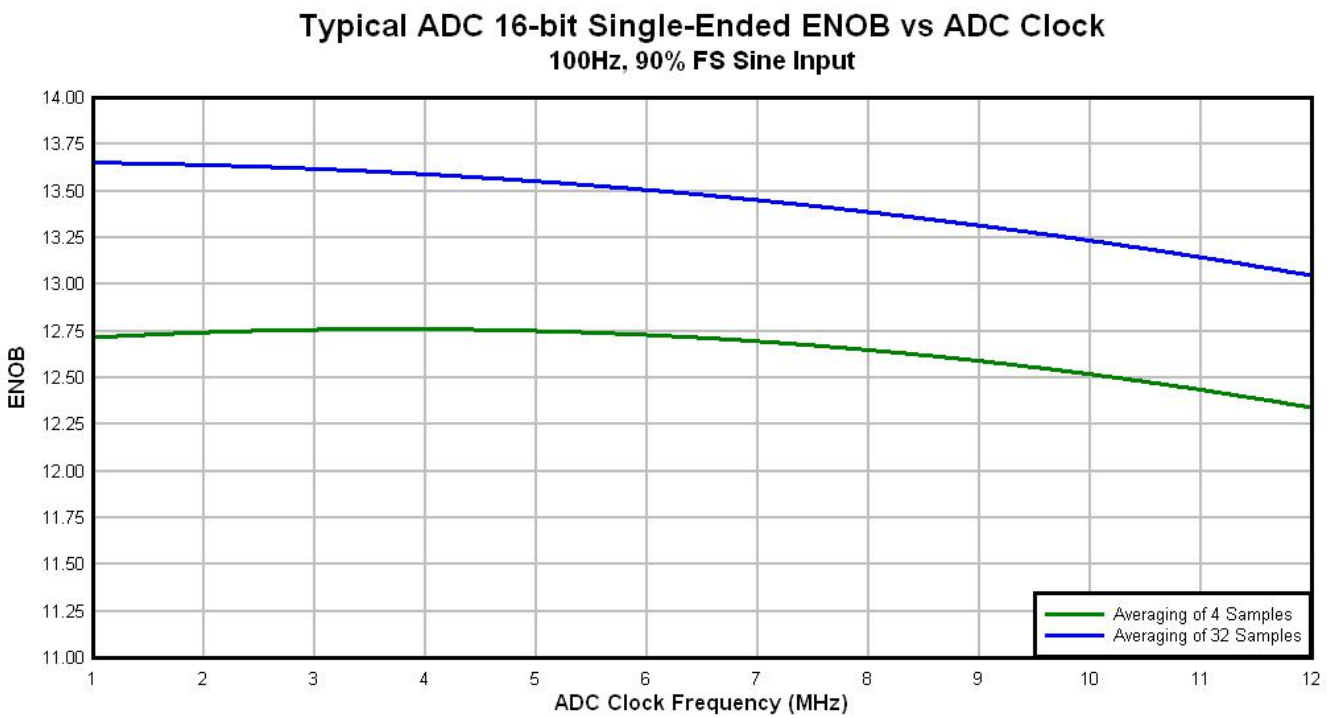



**Figure 12. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode**

## 6.6.2 CMP and 6-bit DAC electrical specifications

### Table 25. Comparator and 6-bit DAC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V |
| $I_{DDHS}$ | Supply current, High-speed mode (EN=1, PMODE=1) | — | — | 200 | µA |
| $I_{DDLS}$ | Supply current, low-speed mode (EN=1, PMODE=0) | — | — | 20 | µA |
| $V_{AIN}$ | Analog input voltage | $V_{SS}$ – 0.3 | — | $V_{DD}$ | V |
| $V_{AIO}$ | Analog input offset voltage | — | — | 20 | mV |
| $V_H$ | Analog comparator hysteresis[1] | | | | |
| | • CR0[HYSTCTR] = 00 | — | 5 | — | mV |
| | • CR0[HYSTCTR] = 01 | — | 10 | — | mV |
| | • CR0[HYSTCTR] = 10 | — | 20 | — | mV |
| | • CR0[HYSTCTR] = 11 | — | 30 | — | mV |
| $V_{CMPOh}$ | Output high | $V_{DD}$ – 0.5 | — | — | V |
| $V_{CMPOl}$ | Output low | — | — | 0.5 | V |
| $t_{DHS}$ | Propagation delay, high-speed mode (EN=1, PMODE=1) | 20 | 50 | 200 | ns |
| $t_{DLS}$ | Propagation delay, low-speed mode (EN=1, PMODE=0) | 80 | 250 | 600 | ns |
| | Analog comparator initialization delay[2] | — | — | 40 | µs |
| $I_{DAC6b}$ | 6-bit DAC current adder (enabled) | — | 7 | — | µA |
| INL | 6-bit DAC integral non-linearity | –0.5 | — | 0.5 | LSB[3] |
| DNL | 6-bit DAC differential non-linearity | –0.3 | — | 0.3 | LSB |

1. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD}$-0.6V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

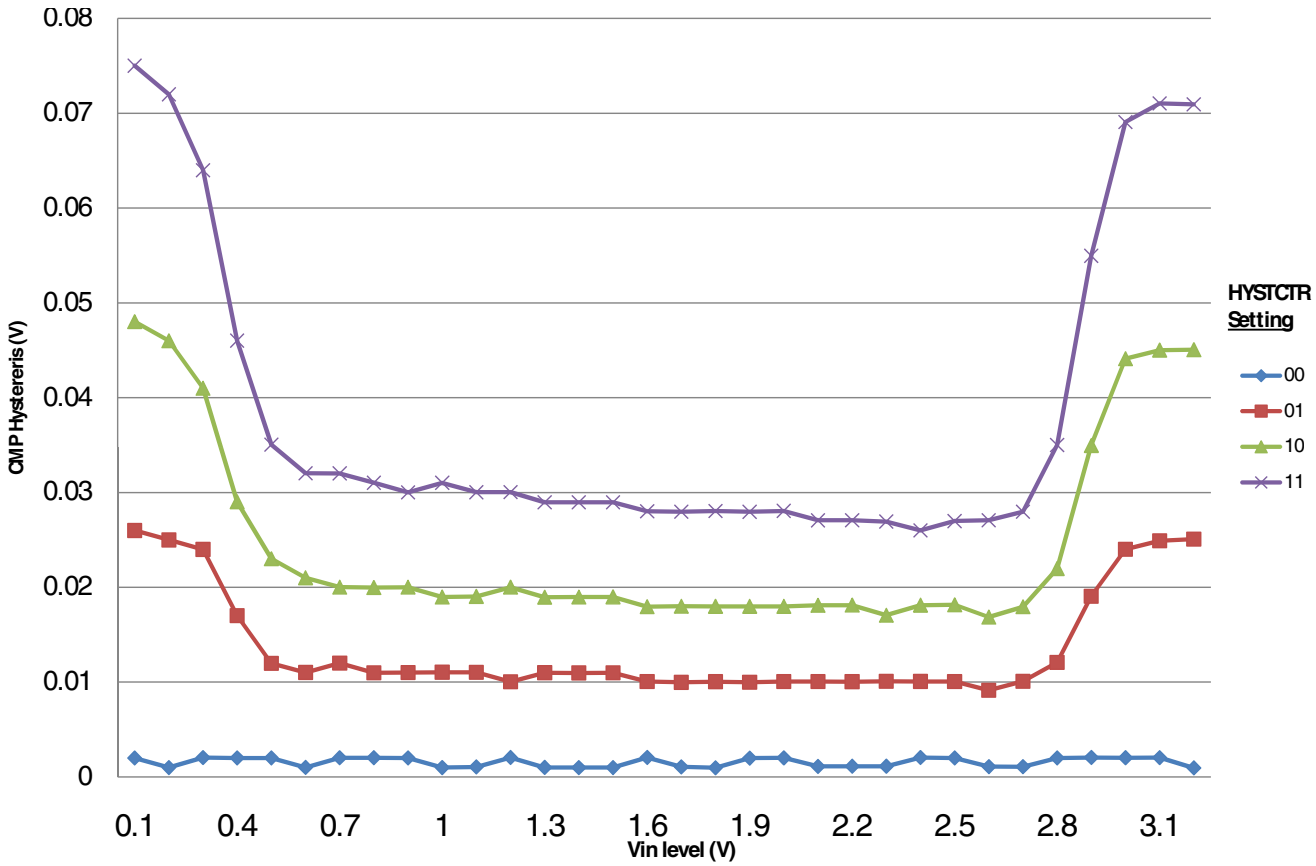



**Figure 13. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=0)**

**Table 37. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)**

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| S12 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK | 30 | — | ns |
| S14 | I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK | 3 | — | ns |
| S15 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid | — | 63 | ns |
| S16 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid | 0 | — | ns |
| S17 | I2S_RXD setup before I2S_RX_BCLK | 30 | — | ns |
| S18 | I2S_RXD hold after I2S_RX_BCLK | 2 | — | ns |
| S19 | I2S_TX_FS input assertion to I2S_TXD output valid[1] | — | 72 | ns |

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

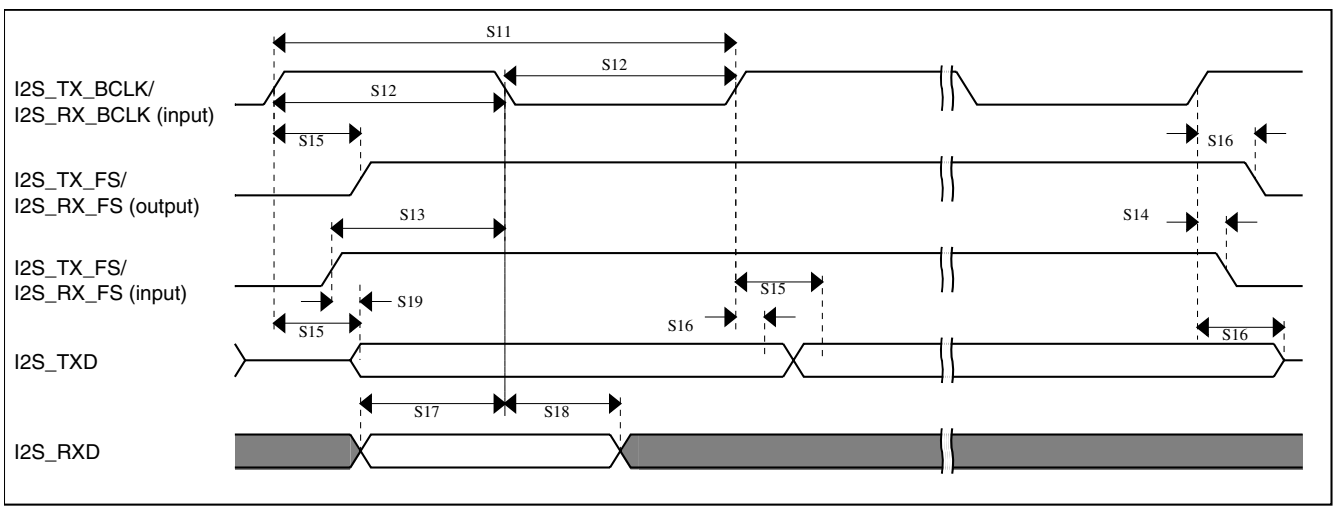



**Figure 22. I2S/SAI timing — slave modes**

# 6.9 Human-machine interfaces (HMI)

## 6.9.1 TSI electrical specifications

**Table 38. TSI electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DDTSI}$ | Operating voltage | 1.71 | — | 3.6 | V | |
| $C_{ELE}$ | Target electrode capacitance range | 1 | 20 | 500 | pF | 1 |

*Table continues on the next page...*

# 7 Dimensions

## 7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to http://www.freescale.com and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|---|---|
| 64-pin LQFP | 98ASS23234W |
| 64-pin MAPBGA | 98ASA00420D |

# 8 Pinout

## 8.1 K10 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

| 64 MAP BGA | 64 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 | 1 | PTE0 | DISABLED | | PTE0 | | UART1_TX | | | | RTC_CLKOUT | |
| B1 | 2 | PTE1/ LLWU_P0 | DISABLED | | PTE1/ LLWU_P0 | | UART1_RX | | | | | |
| C5 | 3 | VDD | VDD | VDD | | | | | | | | |
| C4 | 4 | VSS | VSS | VSS | | | | | | | | |
| E1 | 5 | PTE16 | ADC0_SE4a | ADC0_SE4a | PTE16 | SPI0_PCS0 | UART2_TX | FTM_CLKIN0 | | FTM0_FLT3 | | |
| D1 | 6 | PTE17 | ADC0_SE5a | ADC0_SE5a | PTE17 | SPI0_SCK | UART2_RX | FTM_CLKIN1 | | LPTMR0_ ALT3 | | |
| E2 | 7 | PTE18 | ADC0_SE6a | ADC0_SE6a | PTE18 | SPI0_SOUT | UART2_CTS_ b | I2C0_SDA | | | | |
| D2 | 8 | PTE19 | ADC0_SE7a | ADC0_SE7a | PTE19 | SPI0_SIN | UART2_RTS_ b | I2C0_SCL | | | | |
| G1 | 9 | ADC0_DP0 | ADC0_DP0 | ADC0_DP0 | | | | | | | | |
| F1 | 10 | ADC0_DM0 | ADC0_DM0 | ADC0_DM0 | | | | | | | | |
| G2 | 11 | ADC0_DP3 | ADC0_DP3 | ADC0_DP3 | | | | | | | | |