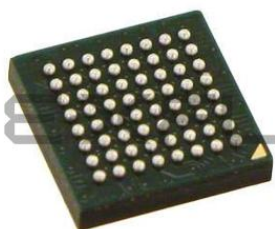


Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?



"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 19x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LFBGA
Supplier Device Package	64-MAPBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk10dx32vmp5

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I _{WP}	Digital I/O weak pullup/pulldown current	10	130	μA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

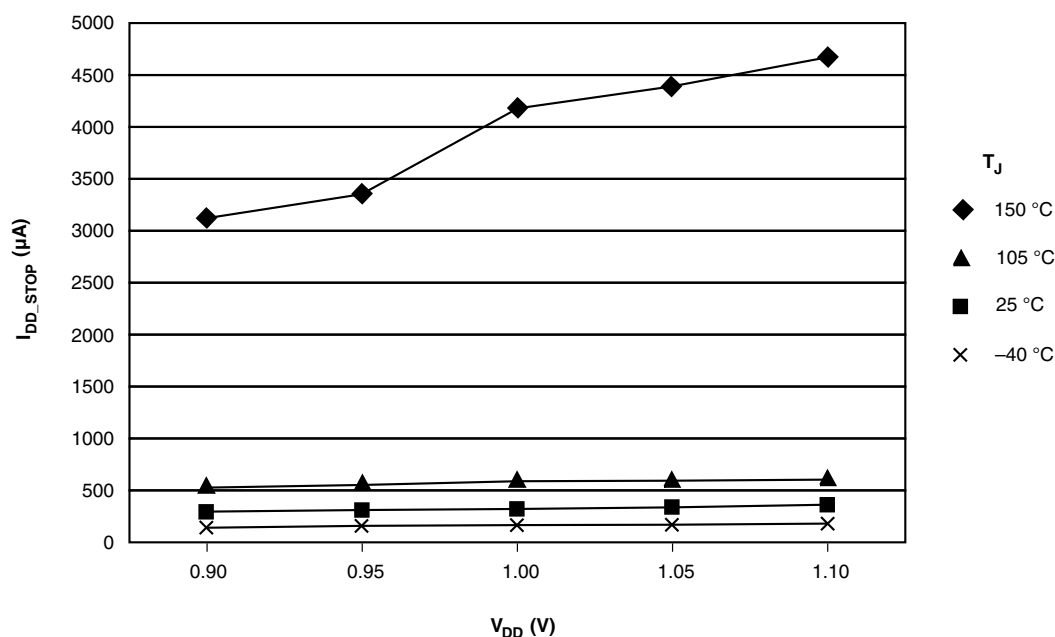
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	–55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	–2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	–100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V _{DD}	Digital supply voltage	–0.3	3.8	V

Table continues on the next page...

5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -9\text{ mA}$	$V_{DD} - 0.5$	—	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -3\text{ mA}$	$V_{DD} - 0.5$	—	V	
	Output high voltage — low drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -2\text{ mA}$	$V_{DD} - 0.5$	—	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -0.6\text{ mA}$	$V_{DD} - 0.5$	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — high drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 9\text{ mA}$	—	0.5	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 3\text{ mA}$	—	0.5	V	
	Output low voltage — low drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 2\text{ mA}$	—	0.5	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 0.6\text{ mA}$	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin)				
	• @ full temperature range	—	1.0	μA	1
	• @ 25 °C	—	0.1	μA	
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	
I_{OZ}	Total Hi-Z (off-state) leakage current (all input pins)	—	4	μA	
R_{PU}	Internal pullup resistors	22	50	k Ω	2
R_{PD}	Internal pulldown resistors	22	50	k Ω	3

1. Tested by ganged leakage method

2. Measured at $V_{input} = V_{SS}$

3. Measured at $V_{input} = V_{DD}$

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR} , and $V_{LLSx} \rightarrow \text{RUN}$ recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock = 50 MHz
- Flash clock = 25 MHz

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	μs	1
	• VLLS0 → RUN	—	130	μs	
	• VLLS1 → RUN	—	130	μs	
	• VLLS2 → RUN	—	70	μs	
	• VLLS3 → RUN	—	70	μs	
	• LLS → RUN	—	6	μs	
	• VLPS → RUN	—	5.2	μs	
	• STOP → RUN	—	5.2	μs	

1. Normal boot (FTFL_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash	—	13.7	15.1	mA	2
	• @ 1.8V	—	13.9	15.3	mA	
	• @ 3.0V					
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash	—	16.1	18.2	mA	3, 4
	• @ 1.8V					
	• @ 3.0V	—	16.3	17.7	mA	
	• @ 25°C	—	16.7	18.4	mA	
	• @ 125°C					
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	7.5	8.4	mA	2
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	5.6	6.4	mA	5

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	867	—	μA	6
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.1	—	mA	7
I _{DD_VLPW}	Very-low-power wait mode current at 3.0 V	—	509	—	μA	8
I _{DD_STOP}	Stop mode current at 3.0 V					
	• @ -40 to 25°C	—	310	426	μA	
	• @ 70°C	—	384	458	μA	
	• @ 105°C	—	629	1100	μA	
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• @ -40 to 25°C	—	3.5	22.6	μA	
	• @ 70°C	—	20.7	52.9	μA	
	• @ 105°C	—	85	220	μA	
I _{DD_LLS}	Low leakage stop mode current at 3.0 V					
	• @ -40 to 25°C	—	2.1	3.7	μA	
	• @ 70°C	—	7.7	43.1	μA	
	• @ 105°C	—	32.2	68	μA	
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					
	• @ -40 to 25°C	—	1.5	2.9	μA	
	• @ 70°C	—	4.8	22.5	μA	
	• @ 105°C	—	20	37.8	μA	
I _{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	• @ -40 to 25°C	—	1.4	2.8	μA	
	• @ 70°C	—	4.1	19.2	μA	
	• @ 105°C	—	17.3	32.4	μA	
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• @ -40 to 25°C	—	0.678	1.3	μA	
	• @ 70°C	—	2.8	13.6	μA	
	• @ 105°C	—	13.6	24.5	μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled					
	• @ -40 to 25°C	—	0.367	1.0	μA	
	• @ 70°C	—	2.4	13.3	μA	
	• @ 105°C	—	13.2	24.1	μA	

Table continues on the next page...

Table 9. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
$f_{\text{LPTMR_pin}}$	LPTMR clock	—	25	MHz	
$f_{\text{LPTMR_ERCLK}}$	LPTMR external reference clock	—	16	MHz	
$f_{\text{I2S_MCLK}}$	I2S master clock	—	12.5	MHz	
$f_{\text{I2S_BCLK}}$	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

5.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CMT, and I²C signals.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Mode select ($\overline{\text{EZP_CS}}$) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time (high drive strength) <ul style="list-style-type: none"> Slew disabled <ul style="list-style-type: none"> $1.71 \leq V_{\text{DD}} \leq 2.7\text{V}$ — 13 ns $2.7 \leq V_{\text{DD}} \leq 3.6\text{V}$ — ns Slew enabled <ul style="list-style-type: none"> $1.71 \leq V_{\text{DD}} \leq 2.7\text{V}$ — ns $2.7 \leq V_{\text{DD}} \leq 3.6\text{V}$ — 36 ns 				4

Table continues on the next page...

Table 10. General switching specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	Port rise and fall time (low drive strength)				5
	<ul style="list-style-type: none"> Slew disabled <ul style="list-style-type: none"> $1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$ Slew enabled <ul style="list-style-type: none"> $1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$ 	—	12	ns	
		—	6	ns	
		—	36	ns	
		—	24	ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75pF load
5. 15pF load

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	−40	125	°C
T_A	Ambient temperature	−40	105	°C

5.4.2 Thermal attributes

Board type	Symbol	Description	64 MAPBGA	64 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	107	65	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	56	46	°C/W	1, 3

Table continues on the next page...

Table 13. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f _{fill_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f _{dco}	DCO output frequency range	Low range (DRS=00) 640 × f _{fill_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f _{fill_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f _{fill_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f _{fill_ref}	80	83.89	100	MHz	
f _{dco_t_DMx3} 2	DCO output frequency	Low range (DRS=00) 732 × f _{fill_ref}	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f _{fill_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f _{fill_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f _{fill_ref}	—	95.98	—	MHz	
J _{cyc_fill}	FLL period jitter <ul style="list-style-type: none">f_{VCO} = 48 MHzf_{VCO} = 98 MHz		— —	180 150	— —	ps	
t _{fill_acquire}	FLL target frequency acquisition time		—	—	1	ms	6
PLL							
f _{vco}	VCO operating frequency		48.0	—	100	MHz	
I _{pll}	PLL operating current <ul style="list-style-type: none">PLL @ 96 MHz (f_{osc_hi_1} = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 48)		—	1060	—	μA	7
I _{pll}	PLL operating current <ul style="list-style-type: none">PLL @ 48 MHz (f_{osc_hi_1} = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 24)		—	600	—	μA	7
f _{pll_ref}	PLL reference frequency range		2.0	—	4.0	MHz	
J _{cyc_pll}	PLL period jitter (RMS)						8
	<ul style="list-style-type: none">f_{vco} = 48 MHzf_{vco} = 100 MHz		— —	120 50	— —	ps ps	

Table continues on the next page...

Table 13. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
J_{acc_pll}	PLL accumulated jitter over 1 μ s (RMS) <ul style="list-style-type: none"> $f_{vco} = 48$ MHz $f_{vco} = 100$ MHz 	—	1350	—	ps	8
		—	600	—	ps	
D_{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll_ref})$	s	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

6.3.2.1 Oscillator DC electrical specifications

Table 14. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	μ A	
	• 8 MHz (RANGE=01)	—	300	—	μ A	
	• 16 MHz	—	950	—	μ A	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	

Table continues on the next page...

Table 14. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	—	μA	
	• 4 MHz	—	400	—	μA	
	• 8 MHz (RANGE=01)	—	500	—	μA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C _x	EXTAL load capacitance	—	—	—		2, 3
C _y	XTAL load capacitance	—	—	—		2, 3
R _F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R _S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V _{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V _{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V _{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C

2. See crystal or resonator manufacturer's recommendation

3. C_x,C_y can be provided by using either the integrated capacitors or by using external components.4. When low power mode is selected, R_F is integrated and must not be attached externally.

Table 16. 32kHz oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp} ¹	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.3.2 32kHz oscillator frequency specifications

Table 17. 32kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$f_{ec_extal32}$	Externally provided input clock frequency	—	32.768	—	kHz	2
$V_{ec_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT} .

6.4 Memories and memory interfaces

6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 18. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvp4gm}	Longword Program high-voltage time	—	7.5	18	μs	
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversblk32k}$	Erase Block high-voltage time for 32 KB	—	52	452	ms	1
$t_{hversblk128k}$	Erase Block high-voltage time for 128 KB	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

6.4.1.2 Flash timing specifications — commands

Table 19. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1blk32k}$	Read 1s Block execution time	—	—	0.5	ms	
$t_{rd1blk128k}$	<ul style="list-style-type: none"> 32 KB data flash 128 KB program flash 	—	—	1.7	ms	
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	μs	1
t_{pgmchk}	Program Check execution time	—	—	45	μs	1
t_{rdsrc}	Read Resource execution time	—	—	30	μs	1
t_{pgm4}	Program Longword execution time	—	65	145	μs	
$t_{ersblk32k}$	Erase Flash Block execution time	—	55	465	ms	2
$t_{ersblk128k}$	<ul style="list-style-type: none"> 32 KB data flash 128 KB program flash 	—	61	495	ms	
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
$t_{pgmsec512}$	Program Section execution time	—	4.7	—	ms	
$t_{pgmsec1k}$	<ul style="list-style-type: none"> 512 B flash 1 KB flash 	—	9.3	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t_{rdonce}	Read Once execution time	—	—	25	μs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	μs	
t_{ersall}	Erase All Blocks execution time	—	115	1000	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1
$t_{pgmpart32k}$	Program Partition for EEPROM execution time	—	70	—	ms	
$t_{setramff}$	Set FlexRAM Function execution time:	—	50	—	μs	
$t_{setram8k}$	<ul style="list-style-type: none"> Control Code 0xFF 8 KB EEPROM backup 	—	0.3	0.5	ms	
$t_{setram32k}$	<ul style="list-style-type: none"> 32 KB EEPROM backup 	—	0.7	1.0	ms	
Byte-write to FlexRAM for EEPROM operation						
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time	—	175	260	μs	3
$t_{eewr8b8k}$	Byte-write to FlexRAM execution time:	—	340	1700	μs	
$t_{eewr8b16k}$	<ul style="list-style-type: none"> 8 KB EEPROM backup 16 KB EEPROM backup 	—	385	1800	μs	
$t_{eewr8b32k}$	<ul style="list-style-type: none"> 32 KB EEPROM backup 	—	475	2000	μs	

Table continues on the next page...

Table 21. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
$t_{\text{nvmretd1k}}$	Data retention after up to 1 K cycles	20	100	—	years	
n_{nvmcyed}	Cycling endurance	10 K	50 K	—	cycles	2
FlexRAM as EEPROM						
$t_{\text{nvmretee100}}$	Data retention up to 100% of write endurance	5	50	—	years	
$t_{\text{nvmretee10}}$	Data retention up to 10% of write endurance	20	100	—	years	
	Write endurance					3
$n_{\text{nvmwree16}}$	• EEPROM backup to FlexRAM ratio = 16	35 K	175 K	—	writes	
$n_{\text{nvmwree128}}$	• EEPROM backup to FlexRAM ratio = 128	315 K	1.6 M	—	writes	
$n_{\text{nvmwree512}}$	• EEPROM backup to FlexRAM ratio = 512	1.27 M	6.4 M	—	writes	
$n_{\text{nvmwree4k}}$	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	—	writes	
$n_{\text{nvmwree8k}}$	• EEPROM backup to FlexRAM ratio = 8192	20 M	100 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$.
3. Write endurance represents the number of writes to each FlexRAM location at $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup. Minimum and typical values assume all byte-writes to FlexRAM.

6.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the flash memory module to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

$$\text{Writes_FlexRAM} = \frac{\text{EEPROM} - 2 \times \text{EEESIZE}}{\text{EEESIZE}} \times \text{Write_efficiency} \times n_{\text{nvmcyed}}$$

where

- Writes_FlexRAM — minimum number of writes to each FlexRAM location

- EEPROM — allocated FlexNVM based on DEPART; entered with the Program Partition command
- EEESIZE — allocated FlexRAM based on DEPART; entered with the Program Partition command
- Write_efficiency —
 - 0.25 for 8-bit writes to FlexRAM
 - 0.50 for 16-bit or 32-bit writes to FlexRAM
- n_{nvmcycd} — data flash cycling endurance (the following graph assumes 10,000 cycles)

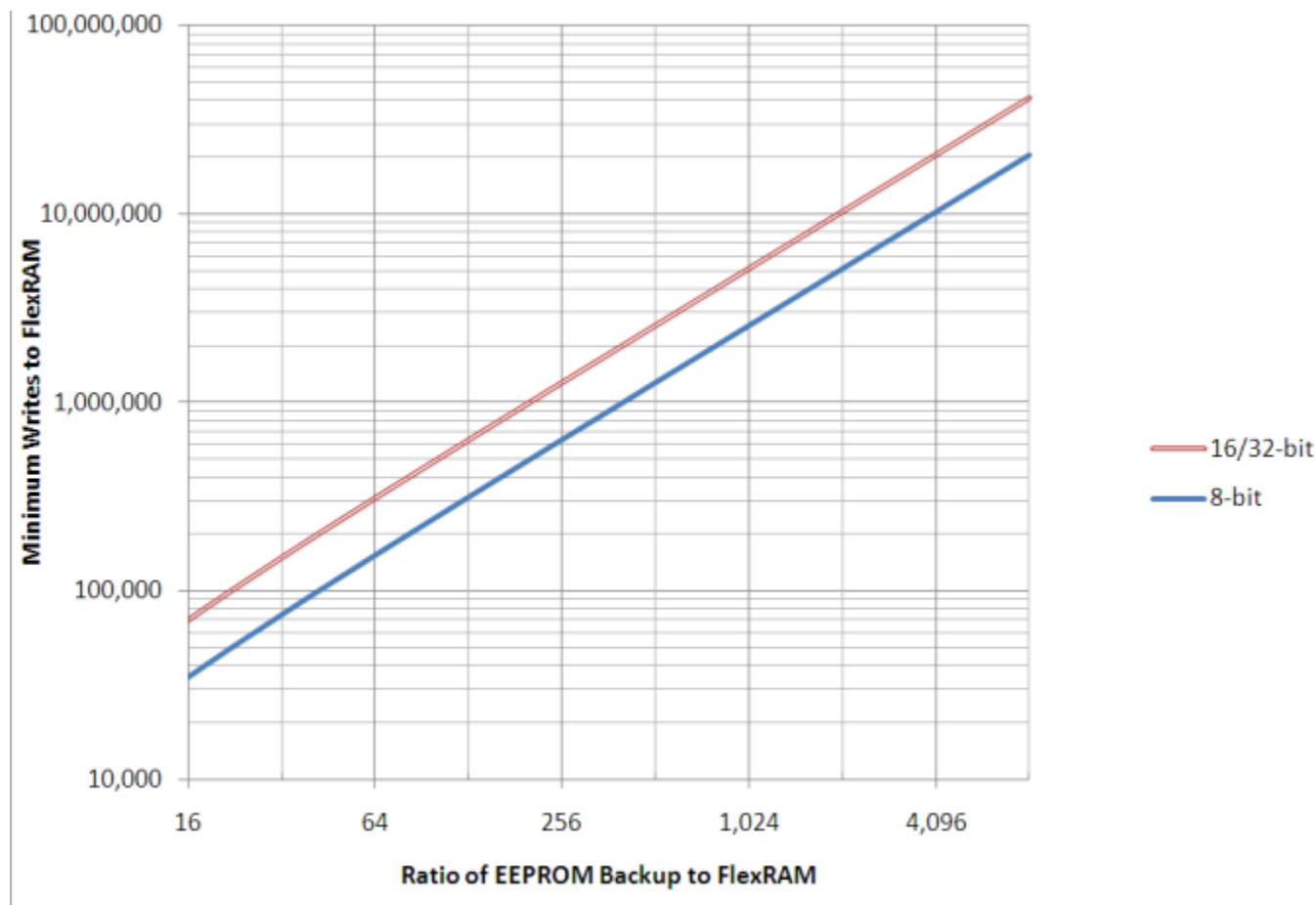


Figure 8. EEPROM backup writes to FlexRAM

6.4.2 EzPort Switching Specifications

Table 22. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V

Table continues on the next page...

Table 24. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

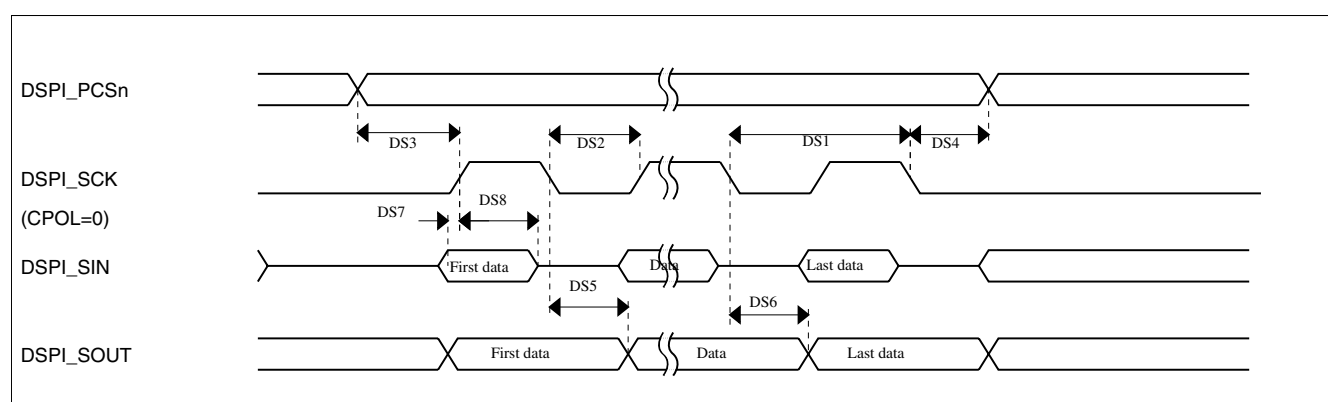
Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
SFDR	Spurious free dynamic range	16 bit differential mode • Avg=32	82	95	—	dB	7
		16 bit single-ended mode • Avg=32	78	90	—	dB	
E_{IL}	Input leakage error		$I_{in} \times R_{AS}$			mV	I_{in} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	–40°C to 105°C	—	1.715	—	mV/°C	
V_{TEMP25}	Temp sensor voltage	25°C	—	719	—	mV	

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume $V_{DDA} = 3.0$ V, Temp = 25°C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit should be set, the HSC bit should be clear with 1MHz ADC conversion clock speed.
4. $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock <16MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock <12MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock <12MHz.

Table 32. Master mode DSPI timing (full voltage range) (continued)

Num	Description	Min.	Max.	Unit	Notes
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 4$	—	ns	2
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{BUS} \times 2) - 4$	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-1.2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	19.1	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

**Figure 17. DSPI classic SPI timing — master mode****Table 33. Slave mode DSPI timing (full voltage range)**

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	6.25	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK}/2) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	24	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	3.2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	19	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	19	ns

64 MAP BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
A2	64	PTD7	DISABLED		PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		

8.2 K10 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

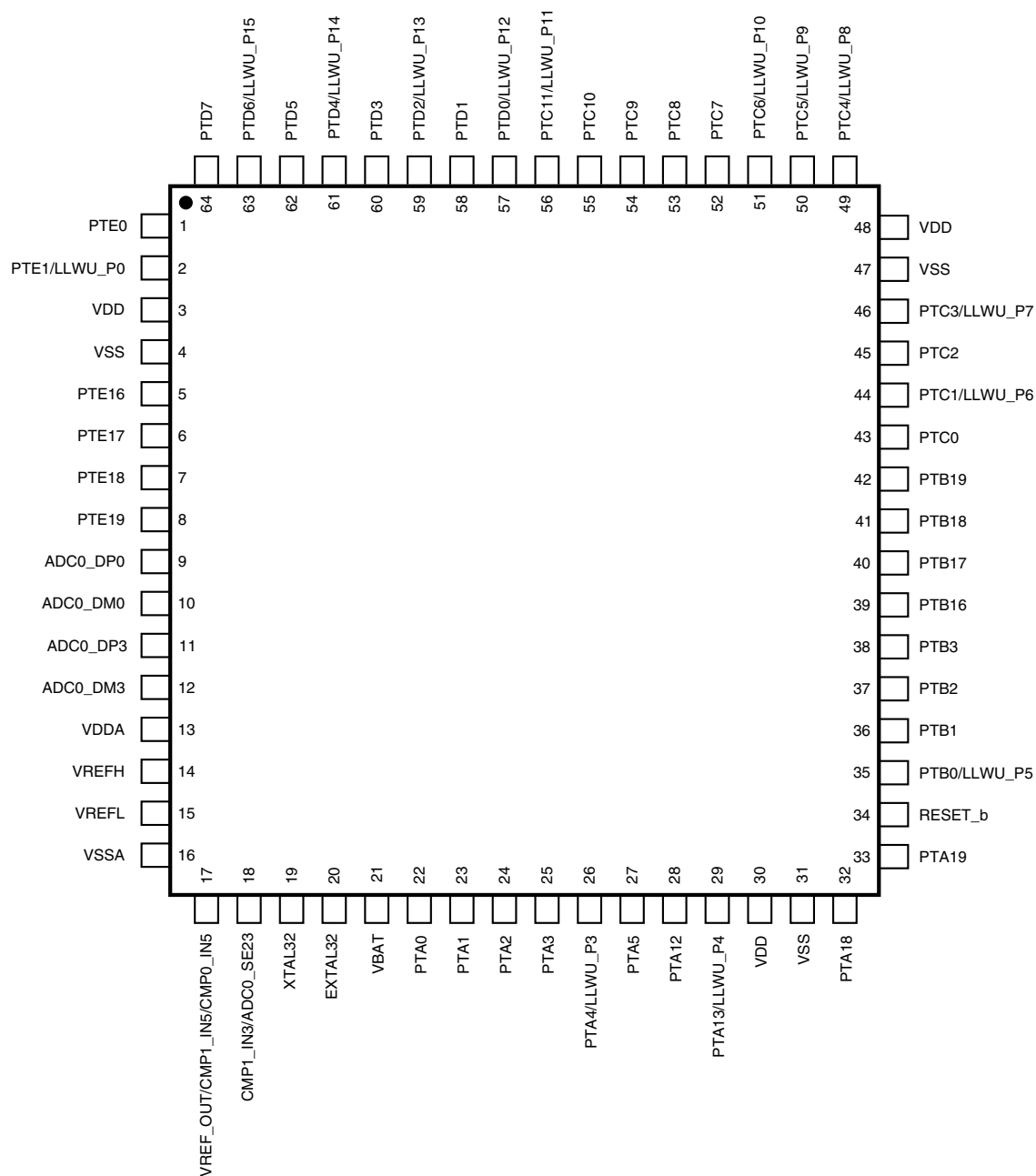


Figure 23. K10 64 LQFP Pinout Diagram

How to Reach Us:

Home Page:

www.freescale.com

Web Support:

<http://www.freescale.com/support>

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductors products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claims alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics as their non-RoHS-complaint and/or non-Pb-free counterparts. For further information, see <http://www.freescale.com> or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to <http://www.freescale.com/epp>.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© 2011–2012 Freescale Semiconductor, Inc.

