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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	70
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2318vf25v

Item	Page	Revision (See Manual for Details)
17.24.2 User Program Mode	729	Programming Procedure in User Program Mode: Description amended (g) Initialization • The general registers other than ER0 and ER1 are saved in the initialization program.
	730	(l) Programming • The general registers other than ER0 and ER1 are saved in the programming program.
17.25 Protection	738	Description amended There are three kinds of flash memory program/erase protection: hardware, software protection, and error protection.
17.29.1 Serial Communication Interface Specification for Boot Mode	754	Status Description amended (2) Inquiry/Selection State ... required for erasure to the on-chip RAM and erases ... (3) Programming/erasing state ... the programming/erasing programs to the on-chip RAM by commands ...
	759	Inquiry and Selection States Description amended (2) Device Selection • Size (1 byte): Amount of device-code data This is fixed to 4
	760	(3) Clock Mode Inquiry (Before) Response | H'31 | Size | A number of modes | Mode | SUM (After) Response | H'31 | Size | Mode | SUM • Size (1 byte): Amount of data that represents the modes • Mode (1 byte): Values of the supported ...

Item	Page	Revision (See Manual for Details)
20.3.6 Flash Memory Characteristics Table 20.29 Flash Memory Characteristics	860	Table 20.29 amended Item | Symbol | Min | Typ | Max | Unit | Test Conditions Number of overwrites | NWEC | 100*3 | 10000*5 | — | Times Data retention time *4 | t_{DRP} | 10 | — | — | Years
		Note 5 added Note: 5. Reference value for 25°C (as a guideline, rewriting should normally function up to this value).
Appendix E Products Lineup Table E.1 H8S/2319 Group Products Lineup	1103	Table E.1 amended HD64F2319E*1 H8S/2317(S)*2
	1104	Notes amended Notes: 1. The on-chip debug function can be used with the E10A emulator (E10A compatible version). 2. H8S/2317S in mask ROM version.
F. Package Dimensions Figure F.4 TLP-113V Package Dimensions		Figure F.4 replaced

6.6 Idle Cycle

6.6.1 Operation

When the chip accesses external space, it can insert a 1-state idle cycle (T_I) between bus cycles in the following two cases: (1) when read accesses in different areas occur consecutively, and (2) when a write cycle occurs immediately after a read cycle. By inserting an idle cycle it is possible, for example, to avoid data collisions between ROM, with a long output floating time, and high-speed memory, I/O interfaces, and so on.

Consecutive Reads in Different Areas: If consecutive reads in different areas occur while the ICIS1 bit in BCRH is set to 1, an idle cycle is inserted at the start of the second read cycle. This is enabled in advanced mode.

Figure 6.16 shows an example of the operation in this case. In this example, bus cycle A is a read cycle from ROM with a long output floating time, and bus cycle B is a read cycle from SRAM, each being located in a different area. In (a), an idle cycle is not inserted, and a collision occurs in cycle B between the read data from ROM and that from SRAM. In (b), an idle cycle is inserted, and a data collision is prevented.

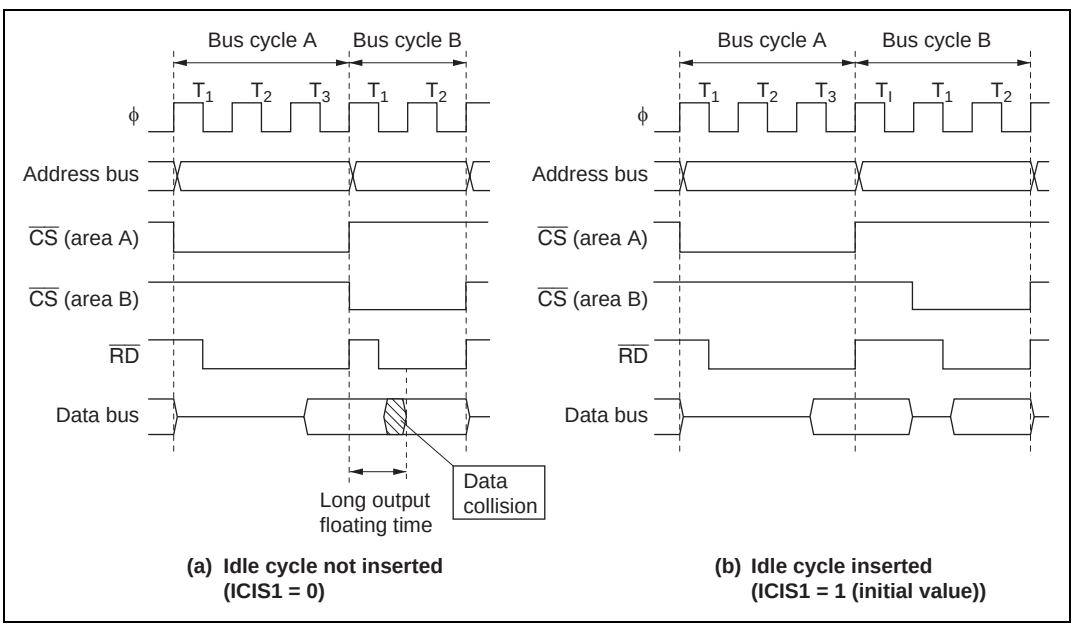

Figure 6.16 Example of Idle Cycle Operation (1)

Port 3 Register (PORT3)

Bit	:	7	6	5	4	3	2	1	0
		—	—	P35	P34	P33	P32	P31	P30
Initial value	:	Undefined	Undefined	—*	—*	—*	—*	—*	—*
R/W	:	—	—	R	R	R	R	R	R

Note: * Determined by state of pins P35 to P30.

PORT3 is an 8-bit read-only register that shows the pin states, and cannot be modified. Writing of output data for the port 3 pins (P35 to P30) must always be performed on P3DR.

Bits 7 and 6 are reserved; they return an undetermined value if read, and cannot be modified.

If a port 3 read is performed while P3DDR bits are set to 1, the P3DR values are read. If a port 3 read is performed while P3DDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORT3 contents are determined by the pin states, as P3DDR and P3DR are initialized. PORT3 retains its prior state in software standby mode.

Port 3 Open Drain Control Register (P3ODR)

Bit	:	7	6	5	4	3	2	1	0
		—	—	P35ODR	P34ODR	P33ODR	P32ODR	P31ODR	P30ODR
Initial value	:	Undefined	Undefined	0	0	0	0	0	0
R/W	:	—	—	R/W	R/W	R/W	R/W	R/W	R/W

P3ODR is an 8-bit readable/writable register that controls the PMOS on/off status for each port 3 pin (P35 to P30).

Bits 7 and 6 are reserved; they return an undetermined value if read, and cannot be modified.

Setting P3ODR bits to 1 makes the corresponding port 3 pins NMOS open-drain output pins, while clearing the bits to 0 makes the pins CMOS output pins.

P3ODR is initialized to H'00 (bits 5 to 0) by a reset, and in hardware standby mode. It retains its prior state in software standby mode.

Mode 6*: In mode 6, port C pins function as address outputs or input ports. Input or output can be specified on an individual bit basis. Setting PCDDR bits to 1 makes the corresponding port C pins address outputs, while clearing the bits to 0 makes the pins an input ports.

Port C pin functions in mode 6 are shown in figure 8.15.

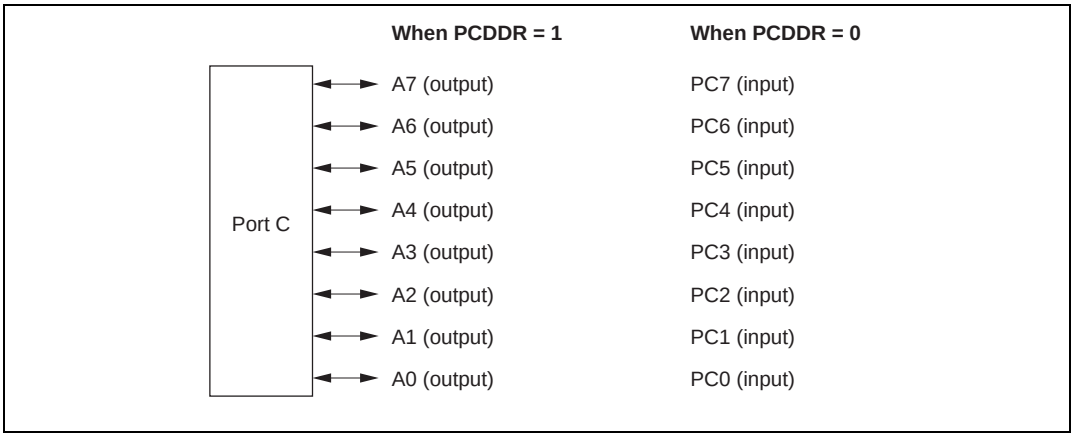

Figure 8.15 Port C Pin Functions (Mode 6)

Mode 7*: In mode 7, port C pins function as I/O ports. Input or output can be specified for each pin on an individual bit basis. Setting PCDDR bits to 1 makes the corresponding port C pins output ports, while clearing the bits to 0 makes the pins input ports.

Port C pin functions in mode 7 are shown in figure 8.16.

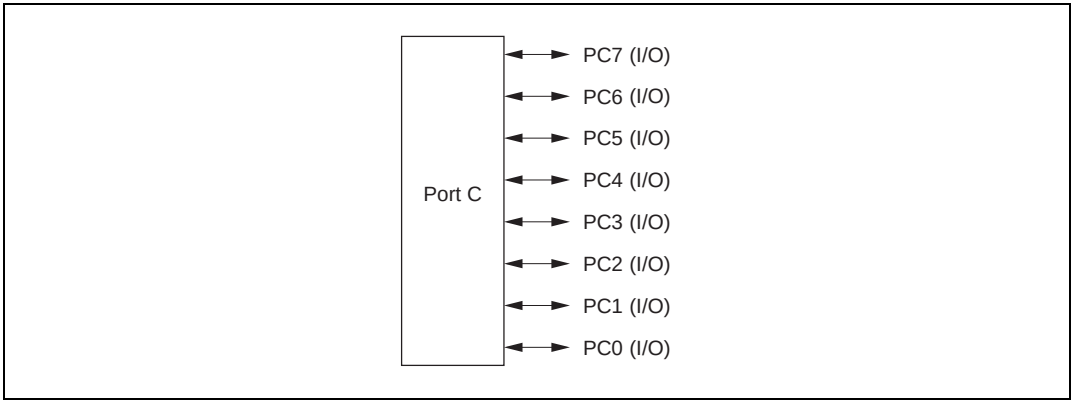

Figure 8.16 Port C Pin Functions (Mode 7)

Note: * Modes 6 and 7 are not available in the ROMless versions.

8.9.3 Pin Functions

Modes 4 to 6*: In modes 4 to 6, port D pins are automatically designated as data I/O pins.

Port D pin functions in modes 4 to 6 are shown in figure 8.18.

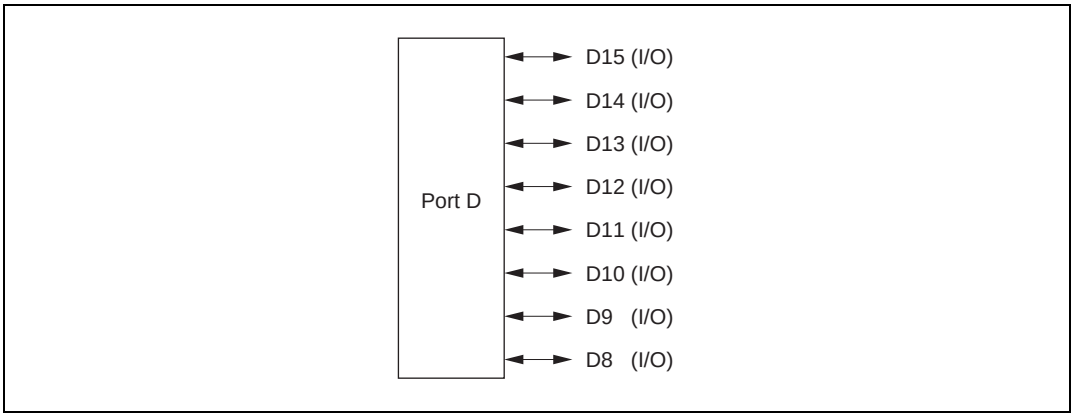

Figure 8.18 Port D Pin Functions (Modes 4 to 6)

Mode 7*: In mode 7, port D pins function as I/O ports. Input or output can be specified for each pin on an individual bit basis. Setting PDDDR bits to 1 makes the corresponding port D pins output ports, while clearing the bits to 0 makes the pins input ports.

Port D pin functions in mode 7 are shown in figure 8.19.

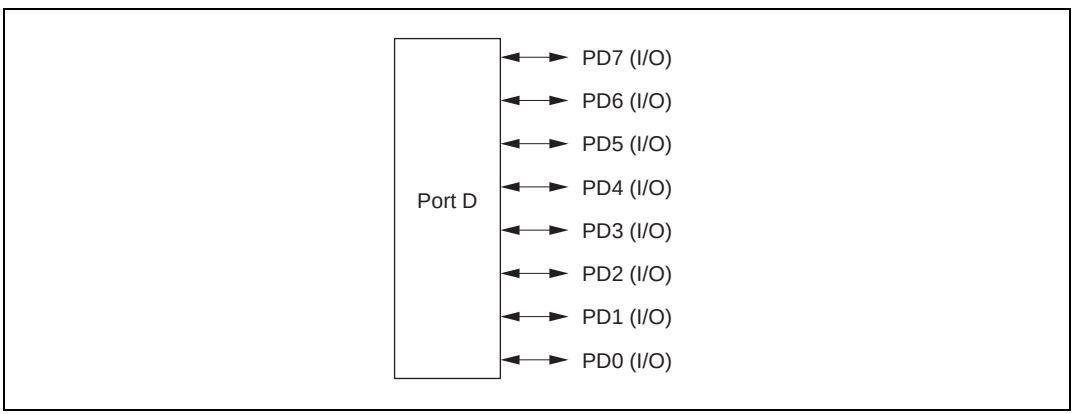

Figure 8.19 Port D Pin Functions (Mode 7)

Note: * Modes 6 and 7 are not available in the ROMless versions.

Channel	Name	Symbol	I/O	Function
3	Input capture/out compare match A3	TIOCA3	I/O	TGR3A input capture input/output compare output/PWM output pin
	Input capture/out compare match B3	TIOCB3	I/O	TGR3B input capture input/output compare output/PWM output pin
	Input capture/out compare match C3	TIOCC3	I/O	TGR3C input capture input/output compare output/PWM output pin
	Input capture/out compare match D3	TIOCD3	I/O	TGR3D input capture input/output compare output/PWM output pin
4	Input capture/out compare match A4	TIOCA4	I/O	TGR4A input capture input/output compare output/PWM output pin
	Input capture/out compare match B4	TIOCB4	I/O	TGR4B input capture input/output compare output/PWM output pin
5	Input capture/out compare match A5	TIOCA5	I/O	TGR5A input capture input/output compare output/PWM output pin
	Input capture/out compare match B5	TIOCB5	I/O	TGR5B input capture input/output compare output/PWM output pin

9.2.2 Timer Mode Registers (TMDR)

Channel 0: TMDR0

Channel 3: TMDR3

Bit	:	7	6	5	4	3	2	1	0
		—	—	BFB	BFA	MD3	MD2	MD1	MD0
Initial value	:	1	1	0	0	0	0	0	0
R/W	:	—	—	R/W	R/W	R/W	R/W	R/W	R/W

Channel 1: TMDR1

Channel 2: TMDR2

Channel 4: TMDR4

Channel 5: TMDR5

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	MD3	MD2	MD1	MD0
Initial value	:	1	1	0	0	0	0	0	0
R/W	:	—	—	—	—	R/W	R/W	R/W	R/W

The TMDR registers are 8-bit readable/writable registers that are used to set the operating mode for each channel. The TPU has six TMDR registers, one for each channel. The TMDR registers are initialized to H'C0 by a reset and in hardware standby mode.

TMDR register settings should be made only when TCNT operation is stopped.

Bits 7 and 6—Reserved: These bits cannot be modified and are always read as 1.

Bit 5—Buffer Operation B (BFB): Specifies whether TGRB is to operate in the normal way, or TGRB and TGRD are to be used together for buffer operation. When TGRD is used as a buffer register, TGRD input capture/output compare is not generated.

In channels 1, 2, 4, and 5, which have no TGRD, bit 5 is reserved. It is always read as 0 and cannot be modified.

Bit 5 BFB	Description	
0	TGRB operates normally	(Initial value)
1	TGRB and TGRD used together for buffer operation	

Status Flag Clearing Timing: After a status flag is read as 1 by the CPU, it is cleared by writing 0 to it. When the DTC is activated, the flag is cleared automatically. Figure 9.46 shows the timing for status flag clearing by the CPU, and figure 9.47 shows the timing for status flag clearing by the DTC.

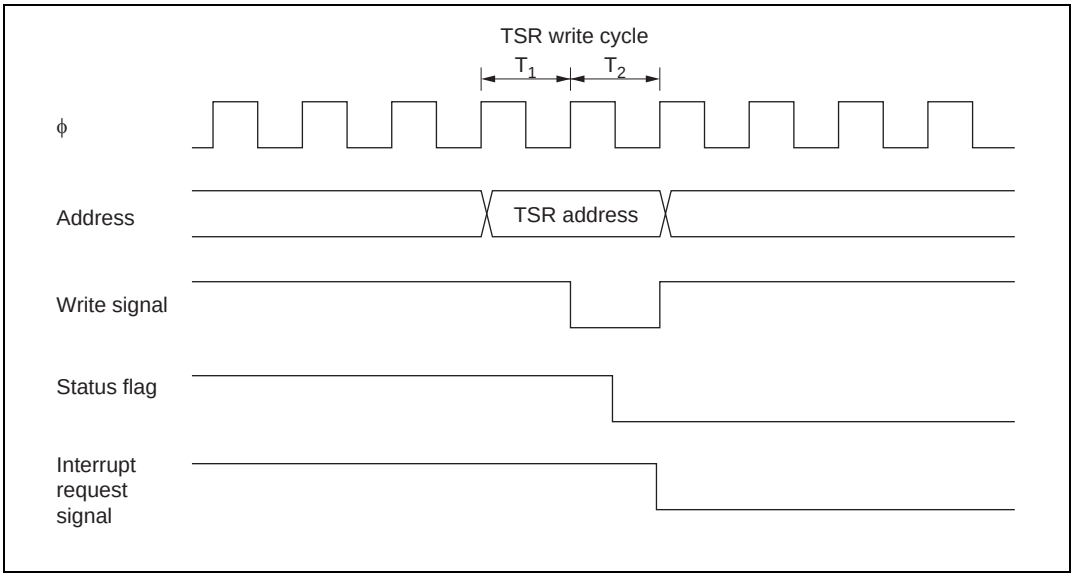

Figure 9.46 Timing for Status Flag Clearing by CPU

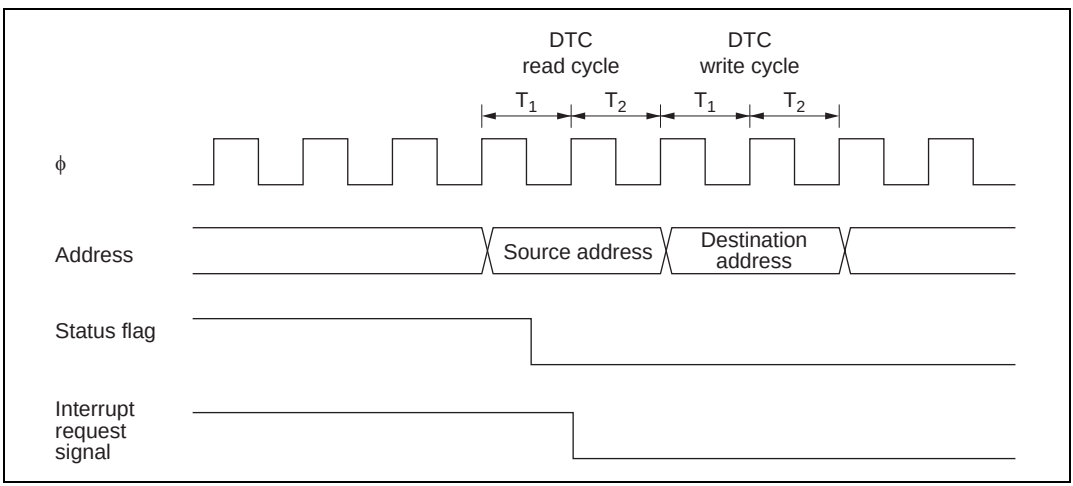

Figure 9.47 Timing for Status Flag Clearing by DTC Activation

11.1.3 Pin Configuration

Table 11.1 describes the WDT output pin.

Table 11.1 WDT Pin

Name	Symbol	I/O	Function
Watchdog timer overflow	$\overline{\text{WDTOVF}}$*	Output	Outputs counter overflow signal in watchdog timer mode

Note: * The $\overline{\text{WDTOVF}}$ function is not available in the F-ZTAT versions.

11.1.4 Register Configuration

The WDT has three registers, as summarized in table 11.2. These registers control clock selection, WDT mode switching, and the reset signal.

Table 11.2 WDT Registers

				Address*1	
Name	Abbreviation	R/W	Initial Value	Write*2	Read
Timer control/status register	TCSR	R/(W)*3	H'18	H'FFBC	H'FFBC
Timer counter	TCNT	R/W	H'00	H'FFBC	H'FFBD
Reset control/status register	RSTCSR	R/(W)*3	H'1F	H'FFBE	H'FFBF

Notes: 1. Lower 16 bits of the address.
2. For details of write operations, see section 11.2.4, Notes on Register Access.
3. Only a write of 0 is permitted to bit 7, to clear the flag.

Section 16 RAM

16.1 Overview

The chip has on-chip high-speed static RAM. The RAM is connected to the CPU by a 16-bit data bus, enabling one-state access by the CPU to both byte data and word data. This makes it possible to perform fast word data transfer.

The on-chip RAM can be enabled or disabled by means of the RAM enable bit (RAME) in the system control register (SYSCR).

Note: The amount of on-chip RAM is 16 kbytes in the H8S/2319C, 8 kbytes in the H8S/2319, H8S/2318, H8S/2317, H8S/2317S, H8S/2316S, H8S/2315, and H8S/2312S, 4 kbytes in the H8S/2314.

16.1.1 Block Diagram

Figure 16.1 shows a block diagram of 8 kbytes of on-chip RAM.

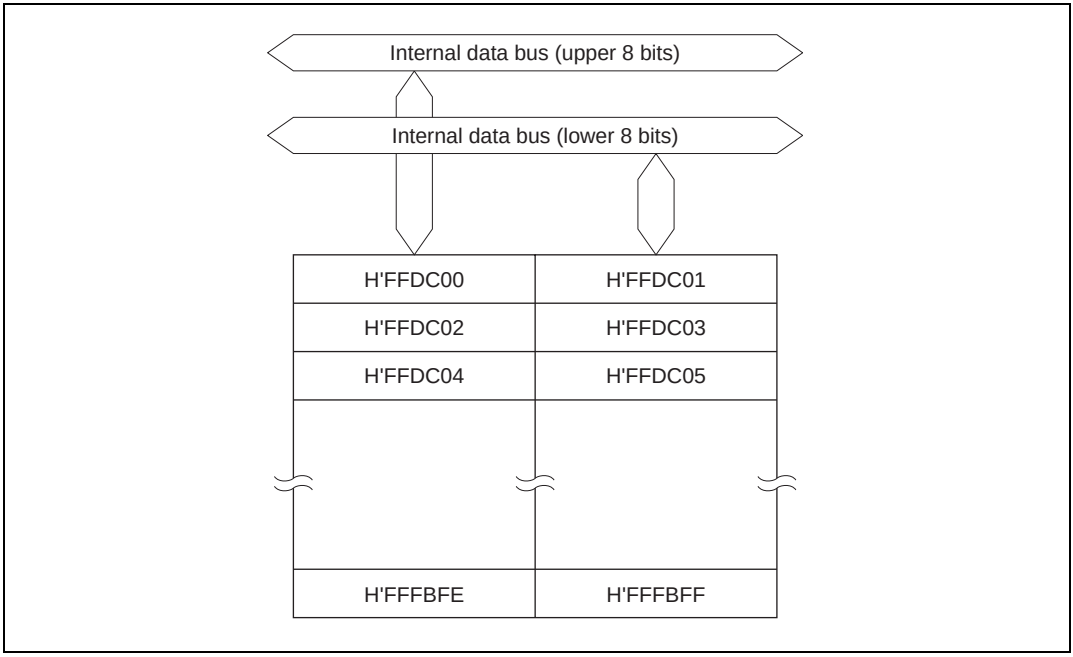

Figure 16.1 Block Diagram of RAM (8 kbytes)

Table 17.2 Operating Modes and ROM (H8S/2318 F-ZTAT, H8S/2317 F-ZTAT, H8S/2315 F-ZTAT, H8S/2314 F-ZTAT)

		Mode Pins				BCRL	
Mode	**Operating Mode**	**FWE**	**MD2**	**MD1**	**MD0**	**EAE**	**On-Chip ROM**
1	—	0	0	0	1	—	—
2				1	0		
3					1		
4	Advanced expanded mode with on-chip ROM disabled		1	0	0	—	Disabled
5	Advanced expanded mode with on-chip ROM disabled				1		
6	Advanced expanded mode with on-chip ROM enabled			1	0	0	Enabled (256 kbytes)*1 *5
						1	Enabled (64 kbytes)
7	Advanced single-chip mode				1	0	Enabled (256 kbytes) *1 *5
						1	Enabled (64 kbytes)
8	—	1	0	0	0	—	—
9					1		
10	Boot mode (advanced expanded mode with on-chip ROM enabled)*3			1	0	0	Enabled (256 kbytes) *2 *5
						1	Enabled (64 kbytes)
11	Boot mode (advanced single-chip mode)*4				1	0	Enabled (256 kbytes) *2 *5
						1	Enabled (64 kbytes)
12	—		1	0	0	—	—
13					1		
14	User program mode (advanced expanded mode with on-chip ROM enabled)*3			1	0	0	Enabled (256 kbytes) *1 *5
						1	Enabled (64 kbytes)
15	User program mode (advanced single-chip mode)*4				1	0	Enabled (256 kbytes) *1 *5
						1	Enabled (64 kbytes)

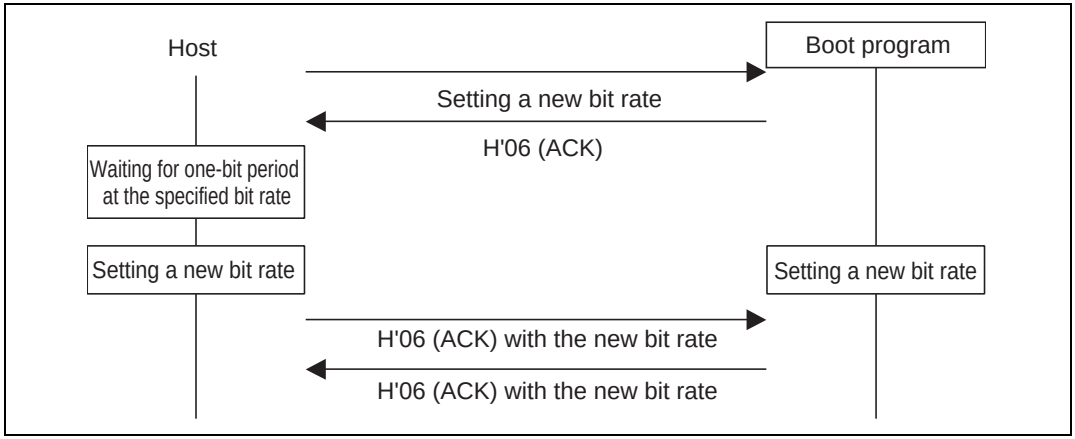

Figure 17.85 New Bit-Rate Selection Sequence

Transition to Programming/Erasing State

The boot program will transfer the erasing program, and erase the user MATs and user boot MATs in that order. On completion of this erasure, ACK will be returned and will enter the programming/erasing state.

The host should select the device code, clock mode, and new bit rate with device selection, clock-mode selection, and new bit-rate selection commands, and then send the command for the transition to programming/erasing state. These procedure should be carried out before sending of the programming selection command or program data.

Command	H'40

- Command, H'40, (1 byte): Transition to programming/erasing state

Response	H'06

- Response, H'06, (1 byte): Response to transition to programming/erasing state
  The boot program will send ACK when the user MAT and user boot MAT have been erased by the transferred erasing program.

Error Response	H'C0	H'51

- Error response, H'C0, (1 byte): Error response for user boot MAT blank check
- Error code, H'51, (1 byte): Erasing error
  An error occurred and erasure was not completed.

Transitions to the reset state, and hardware standby mode are inhibited during programming/erasing. When the reset signal is accidentally input to the chip, a longer period in the reset state than usual (100 μs) is needed before the reset signal is released.

(7) Switching of the MATs by FMATS should be needed when programming/erasing of the user boot MAT is operated in user-boot mode. The program which switches the MATs should be executed from the on-chip RAM. See section 17.27, Switching between User MAT and User Boot MAT. Please make sure you know which MAT is selected when switching between them.

(8) When the data storable area indicated by programming parameter FMPDR is within the flash memory area, an error will occur even when the data stored is normal. Therefore, the data should be transferred to the on-chip RAM to place the address that FMPDR indicates in an area other than the flash memory.

In consideration of these conditions, there are three factors; operating mode, the bank structure of the user MAT, and operations.

The areas in which the programming data can be stored for execution are shown in table 17.26.

Table 17.72 Executable MAT

	Initiated Modes	
Operation	**User Program Mode**	**User Boot Mode***
Programming	Table 17.73 (1)	Table 17.73 (3)
Erasing	Table 17.73 (2)	Table 17.73 (4)

Note: * Programming/Erasing is possible to user MATs.

20.1.2 DC Characteristics

Table 20.2 DC Characteristics

Conditions: V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*1, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	Ports 1, 2, $\overline{IRQ0}$ to $\overline{IRQ7}$	VT^-	$V_{CC} \times 0.2$	—	—	V	
		VT^+	—	—	$V_{CC} \times 0.7$	V	
		$VT^+ - VT^-$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD2 to MD0	V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
	Ports 3, A to G		2.2	—	$V_{CC} + 0.3$	V	
	Port 4		2.2	—	$AV_{CC} + 0.3$	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD2 to MD0	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, ports 3, 4, A to G		–0.3	—	$V_{CC} \times 0.2$	V	
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 μA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	10.0	μA	V_{in} = 0.5 V to V_{CC} – 0.5 V
	$\overline{STBY}$, NMI, MD2 to MD0		—	—	1.0	μA	
	Port 4		—	—	1.0	μA	V_{in} = 0.5 V to AV_{CC} – 0.5 V
Three-state leakage current (off state)	Ports 1, 2, 3, A to G	$\lvert I_{TSI} \rvert$	—	—	1.0	μA	V_{in} = 0.5 V to V_{CC} – 0.5 V

(3) Bus Timing

Table 20.15 Bus Timing

Condition B: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 MHz to 25 MHz, T_a = –20°C to 75°C (regular specifications), T_a = –40°C to 85°C (wide-range specifications)

Item	Symbol	Min	Max	Unit	Test Conditions
Address delay time	t_{AD}	—	20	ns	Figures 20.6 to 20.10
Address setup time	t_{AS}	$0.5 \times t_{cyc} - 15$	—	ns	
Address hold time	t_{AH}	$0.5 \times t_{cyc} - 8$	—	ns	
$\overline{CS}$ delay time 1	t_{CSD1}	—	15	ns	
$\overline{AS}$ delay time	t_{ASD}	—	15	ns	
$\overline{RD}$ delay time 1	t_{RSD1}	—	15	ns	
$\overline{RD}$ delay time 2	t_{RSD2}	—	15	ns	
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
Read data access time 1	t_{ACC1}	—	$1.0 \times t_{cyc} - 20$	ns	
Read data access time 2	t_{ACC2}	—	$1.5 \times t_{cyc} - 20$	ns	
Read data access time 3	t_{ACC3}	—	$2.0 \times t_{cyc} - 20$	ns	
Read data access time 4	t_{ACC4}	—	$2.5 \times t_{cyc} - 20$	ns	
Read data access time 5	t_{ACC5}	—	$3.0 \times t_{cyc} - 20$	ns	
$\overline{WR}$ delay time 1	t_{WRD1}	—	15	ns	
$\overline{WR}$ delay time 2	t_{WRD2}	—	15	ns	
$\overline{WR}$ pulse width 1	t_{WSW1}	$1.0 \times t_{cyc} - 15$	—	ns	
$\overline{WR}$ pulse width 2	t_{WSW2}	$1.5 \times t_{cyc} - 15$	—	ns	
Write data delay time	t_{WDD}	—	20	ns	
Write data setup time	t_{WDS}	$0.5 \times t_{cyc} - 15$	—	ns	
Write data hold time	t_{WDH}	$0.5 \times t_{cyc} - 8$	—	ns	
$\overline{WAIT}$ setup time	t_{WTS}	25	—	ns	Figure 20.8
$\overline{WAIT}$ hold time	t_{WTH}	5	—	ns	
$\overline{BREQ}$ setup time	t_{BRQS}	30	—	ns	Figure 20.11
$\overline{BACK}$ delay time	t_{BACD}	—	15	ns	
Bus floating time	t_{BZD}	—	40	ns	
$\overline{BREQO}$ delay time	t_{BRQOD}	—	25	ns	Figure 20.12

ABWCR—Bus Width Control Register **H'FED0** **Bus Controller**

Bit	:	7	6	5	4	3	2	1	0
		ABW7	ABW6	ABW5	ABW4	ABW3	ABW2	ABW1	ABW0
Modes 5 to 7*									
Initial value	:	1	1	1	1	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Mode 4									
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Area 7 to 0 Bus Width Control

0	Area n is designated for 16-bit access
1	Area n is designated for 8-bit access

(n = 7 to 0)

Note: * Modes 6 and 7 cannot be used in the ROMless versions.

ASTCR—Access State Control Register **H'FED1** **Bus Controller**

Bit	:	7	6	5	4	3	2	1	0
		AST7	AST6	AST5	AST4	AST3	AST2	AST1	AST0
Initial value	:	1	1	1	1	1	1	1	1
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Area 7 to 0 Access State Control

0	Area n is designated for 2-state access Wait state insertion in area n external space is disabled
1	Area n is designated for 3-state access Wait state insertion in area n external space is enabled

(n = 7 to 0)

TDR0—Transmit Data Register 0 H'FF7B SCI0, Smart Card Interface 0

Bit	:	7	6	5	4	3	2	1	0
Initial value	:	1	1	1	1	1	1	1	1
Read/Write	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Stores data for serial transmission