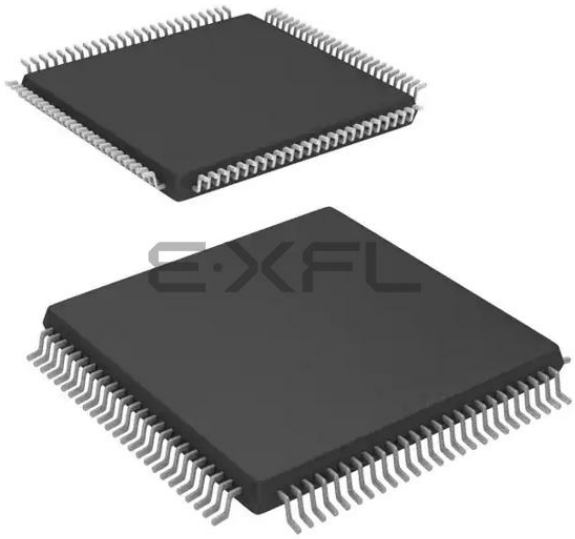

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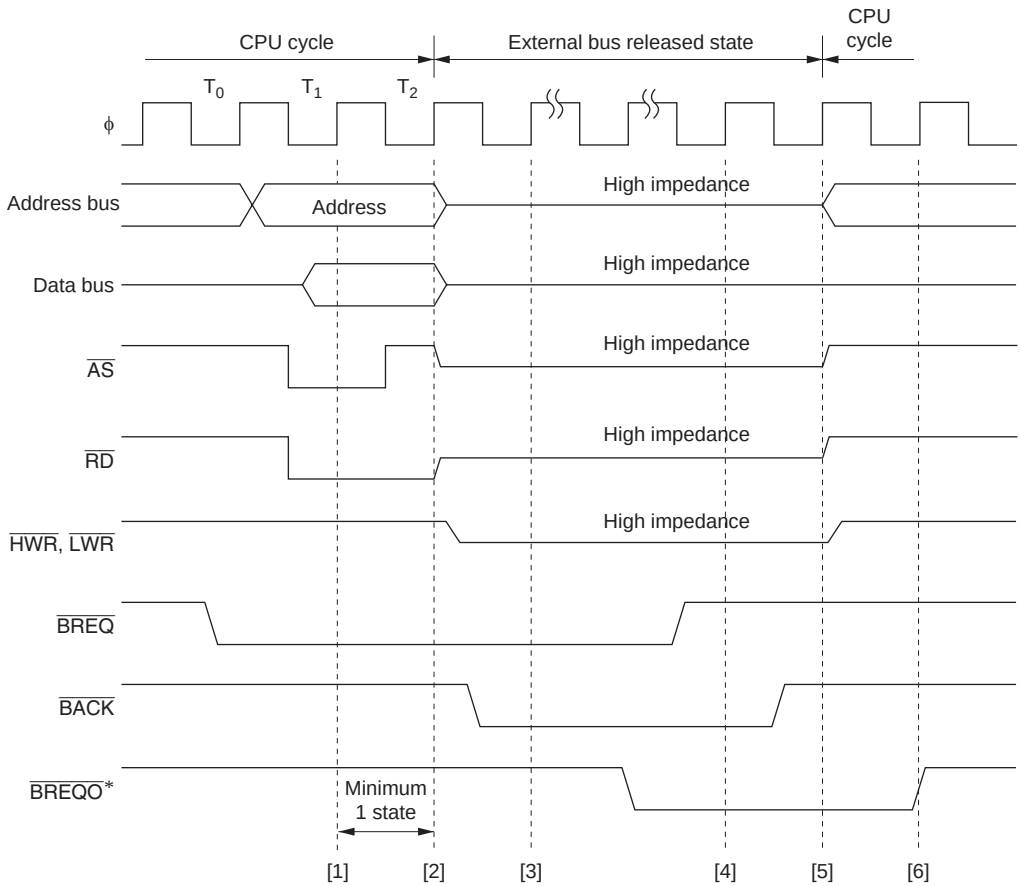
Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	70
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2318vte25iv

6.7.4 Transition Timing

Figure 6.19 shows the timing for transition to the bus released state.



[1] Low level of $\overline{\text{BREQ}}$ pin is sampled at rise of T_2 state.

[2] $\overline{\text{BACK}}$ pin is driven low at end of CPU read cycle, releasing bus to external bus master.

[3] $\overline{\text{BREQ}}$ pin state is still sampled in external bus released state.

[4] High level of $\overline{\text{BREQ}}$ pin is sampled.

[5] $\overline{\text{BACK}}$ pin is driven high, ending bus release cycle.

[6] $\overline{\text{BREQO}}$ signal goes high 1.5 clocks after $\overline{\text{BACK}}$ signal goes high.

Note: * Output only when BREQOE is set to 1.

Figure 6.19 Bus Released State Transition Timing

7.1.3 Register Configuration

Table 7.1 summarizes the DTC registers.

Table 7.1 DTC Registers

Name	Abbreviation	R/W	Initial Value	Address*1
DTC mode register A	MRA	—*2	Undefined	—*3
DTC mode register B	MRB	—*2	Undefined	—*3
DTC source address register	SAR	—*2	Undefined	—*3
DTC destination address register	DAR	—*2	Undefined	—*3
DTC transfer count register A	CRA	—*2	Undefined	—*3
DTC transfer count register B	CRB	—*2	Undefined	—*3
DTC enable registers	DTCER	R/W	H'00	H'FF30 to H'FF34
DTC vector register	DTVECR	R/W	H'00	H'FF37
Module stop control register	MSTPCR	R/W	H'3FFF	H'FF3C

Notes: 1. Lower 16 bits of the address.
2. Registers within the DTC cannot be read or written to directly.
3. Register information is located in on-chip RAM addresses H'F800 to H'FBFF. It cannot be located in external space. When the DTC is used, do not clear the RAME bit in SYSCR to 0.

Pin	Selection Method and Pin Functions
P24/TIOCA4/ TMRI1	This pin is used as the 8-bit timer counter reset pin when bits CCLR1 and CCLR0 in TCR1 are both set to 1. The pin function is switched as shown below according to the combination of the TPU channel 4 setting by bits MD3 to MD0 in TMDR4, bits IOA3 to IOA0 in TIOR4, bits CCLR1 and CCLR0 in TCR4, and bit P24DDR.

TPU Channel 4 Setting	Table Below (1)	Table Below (2)	
P24DDR	—	0	1
Pin function	TIOCA4 output	P24 input	P24 output
		TIOCA4 input *1	
	TMRI1 input		

TPU Channel 4 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000, B'01××		B'001×	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1×××	B'0001 to B'0011 B'0101 to B'0111	B'××00	Other than B'××00		
CCLR1, CCLR0	—	—	—	—	Other than B'01	B'01
Output function	—	Output compare output	—	PWM mode 1 output*2	PWM mode 2 output	—

×: Don't care

Notes: 1. TIOCA4 input when MD3 to MD0 = B'0000 or B'01×× and IOA3 to IOA0 = B'10××.
2. TIOCB4 output is disabled.

8.8.4 MOS Input Pull-Up Function

Port C has a built-in MOS input pull-up function that can be controlled by software. This MOS input pull-up function can be used in modes 6 and 7, and can be specified as on or off on an individual bit basis.

When PCDDR bits are cleared to 0 in mode 6 or 7, setting the corresponding PCPCR bits to 1 turns on the MOS input pull-up for that pins.

The MOS input pull-up function is in the off state after a reset, and in hardware standby mode. The prior state is retained in software standby mode.

Table 8.14 summarizes the MOS input pull-up states.

Table 8.14 MOS Input Pull-Up States (Port C)

Modes	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
4, 5	OFF	OFF	OFF	OFF
6, 7			ON/OFF	ON/OFF

Legend:
OFF: MOS input pull-up is always off.
ON/OFF: On when PCDDR = 0 and PCPCR = 1; otherwise off.

9.1.2 Block Diagram

Figure 9.1 shows a block diagram of the TPU.

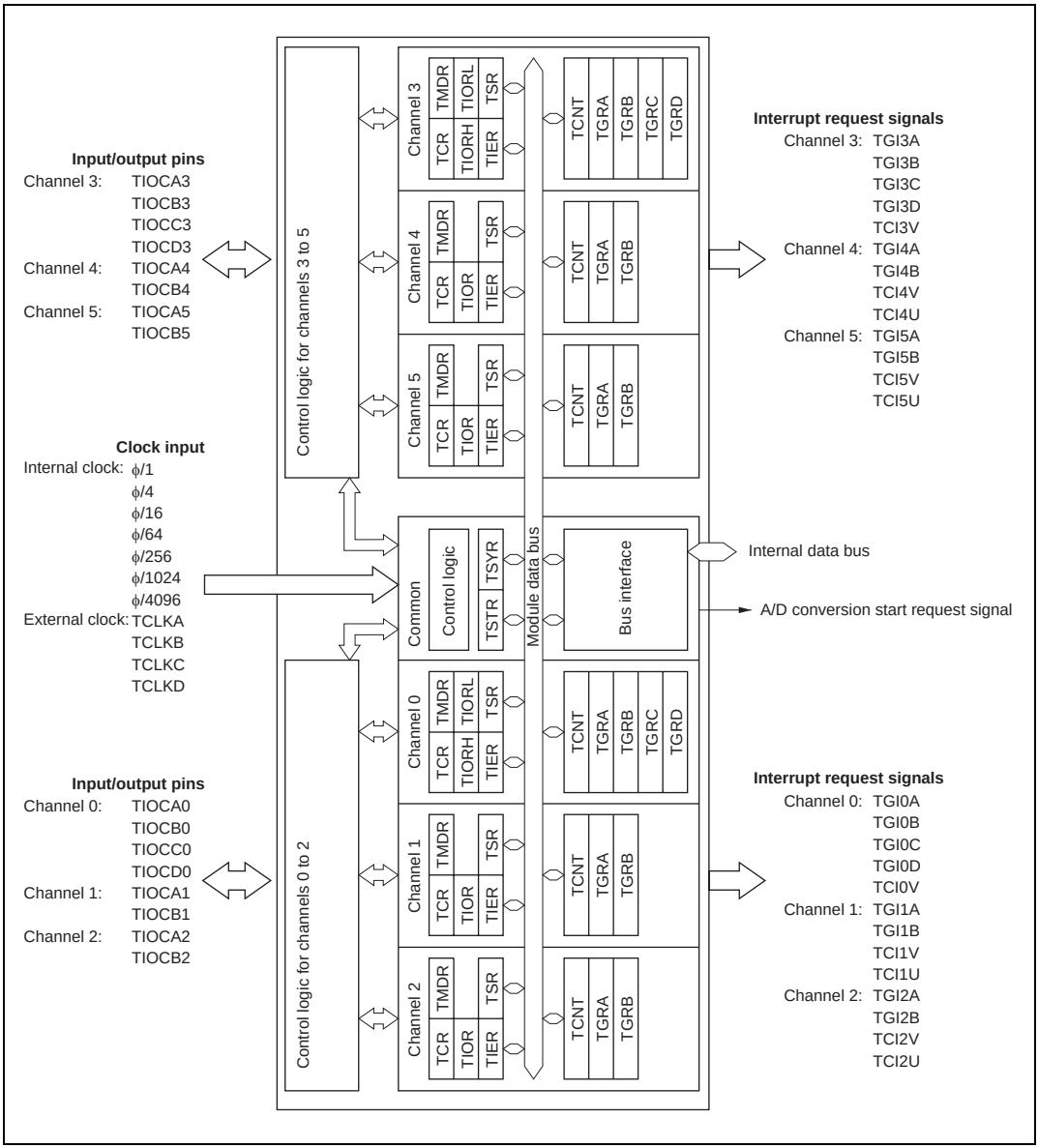


Figure 9.1 Block Diagram of TPU

Channel	Bit 7 IOD3	Bit 6 IOD2	Bit 5 IOD1	Bit 4 IOD0	Description		
3	0	0	0	0	TGR3D is output compare register*2	Output disabled	(Initial value)
				1		Initial output is 0 output	0 output at compare match
			1	0			1 output at compare match
				1			Toggle output at compare match
		1	0	0		Output disabled	
				1		Initial output is 1 output	0 output at compare match
			1	0			1 output at compare match
				1			Toggle output at compare match
	1	0	0	0	TGR3D is input capture register*2	Capture input source is TIOCD3 pin	Input capture at rising edge
				1			Input capture at falling edge
			1	×			Input capture at both edges
		1	×	×		Capture input source is channel 4/count clock	Input capture at TCNT4 count-up/count-down*1

×: Don't care

Notes: 1. When bits TPSC2 to TPSC0 in TCR4 are set to B'000 and φ/1 is used as the TCNT4 count clock, this setting is invalid and input capture is not generated.

2. When the BFB bit in TMDR3 is set to 1 and TGR3D is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

10.5 Sample Application

In the example below, the 8-bit timer is used to generate a pulse output with a selected duty cycle, as shown in figure 10.9. The control bits are set as follows:

[1] In TCR, bit CCLR1 is cleared to 0 and bit CCLR0 is set to 1 so that the timer counter is cleared when its value matches the constant in TCORA.

[2] In TCSR, bits OS3 to OS0 are set to B'0110, causing the output to change to 1 at a TCORA compare match and to 0 at a TCORB compare match.

With these settings, the 8-bit timer provides output of pulses at a rate determined by TCORA with a pulse width determined by TCORB. No software intervention is required.

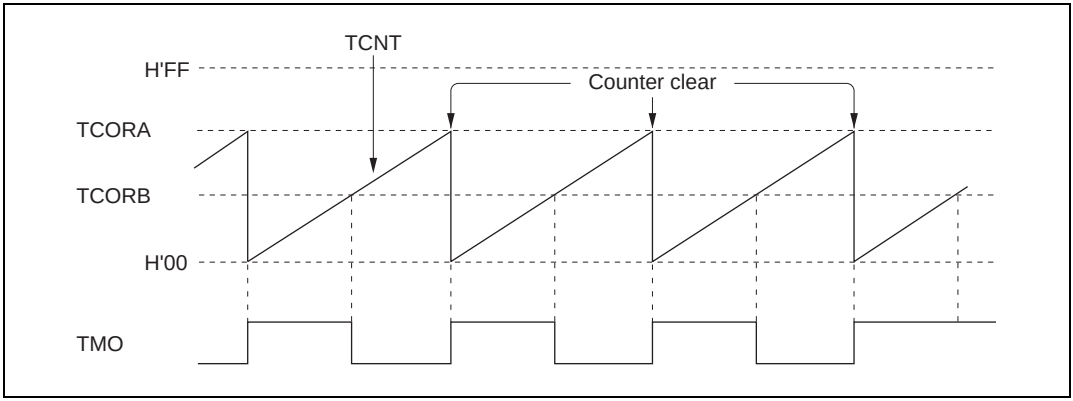


Figure 10.9 Example of Pulse Output

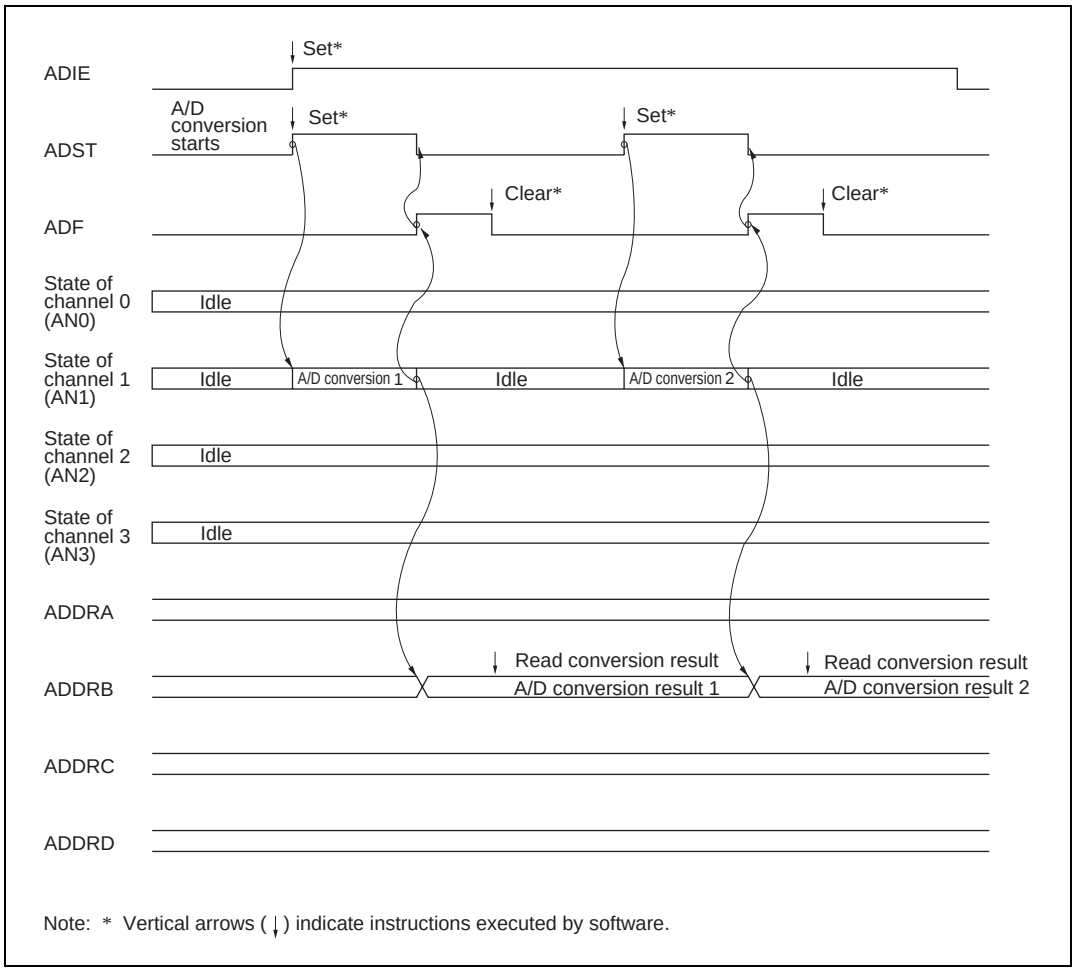


Figure 14.3 Example of A/D Converter Operation (Single Mode, Channel 1 Selected)

17.13 Overview of Flash Memory (H8S/2319 F-ZTAT)

17.13.1 Features

The H8S/2319 F-ZTAT has 512 kbytes of on-chip flash memory. The features of the flash memory are summarized below.

- Four flash memory operating modes
  - Program mode
  - Erase mode
  - Program-verify mode
  - Erase-verify mode
- Programming/erase methods

  The flash memory is programmed 128 bytes at a time. Erasing is performed by block erase (in single-block units). To erase the entire flash memory, the individual blocks must be erased sequentially. Block erasing can be performed as required on 4-kbyte, 32-kbyte, and 64-kbyte blocks.
- Programming/erase times

  The flash memory programming time is 10.0 ms (typ.) for simultaneous 128-byte programming, equivalent to 78 μs (typ.) per byte, and the erase time is 50 ms (typ.).
- Reprogramming capability

  The flash memory can be reprogrammed a minimum of 100 times.
- On-board programming modes

  There are two modes in which flash memory can be programmed/erased/verified on-board:
  - Boot mode
  - User program mode
- Automatic bit rate adjustment

  With data transfer in boot mode, the bit rate of the chip can be automatically adjusted to match the transfer bit rate of the host.
- Flash memory emulation by RAM

  Part of the RAM area can be overlapped onto flash memory, to emulate flash memory updates in real time.
- Protect modes

  There are three protect modes, hardware, software, and error protect, which allow protected status to be designated for flash memory program/erase/verify operations.

17.28.2 PROM Mode Operation

Table 17.57 shows the settings for the operating modes of PROM mode, and table 17.58 lists the commands used in PROM mode. The following sections provide detailed information on each mode.

- Memory-read mode: This mode supports reading, in units of bytes, from the user MAT or user boot MAT.
- Auto-program mode: This mode supports the simultaneous programming of the user MAT and user boot MAT in 128-byte units. Status polling is used to confirm the end of automatic programming.
- Auto-erase mode: This mode only supports the automatic erasing of the entire user MAT or user boot MAT. Status polling is used to confirm the end of automatic erasing.
- Status-read mode: Status polling is used with automatic programming and automatic erasure. Normal completion can be detected by reading the signal on the I/O_6 pin. In status-read mode, error information is output when an error has occurred.

Table 17.57 Settings for Each Operating Mode of PROM Mode

	Pin Name				
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**$\overline{WE}$**	**I/O7 to 0**	**A18 to 0**
Read	L	L	H	Data output	Ain
Output disable	L	H	H	Hi-Z	X
Command write	L	H	L	Data input	Ain*2
Chip disable*1	H	X	X	Hi-Z	X

Notes: 1. The chip-disable mode is not a standby state; internally, it is an operational state.
2. Ain indicates that there is also an address input in auto-program mode.

19.2.3 Module Stop Control Register (MSTPCR)

	MSTPCRH								MSTPCRL							
Bit :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value :	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W :	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MSTPCR is a 16-bit readable/writable register that performs module stop mode control.

MSTPCR is initialized to H'3FFF by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bits 15 to 0—Module Stop (MSTP 15 to MSTP 0): These bits specify module stop mode. See table 19.3 for the method of selecting on-chip supporting modules.

Bits 15 to 0 MSTP15 to MSTP0	Description
0	Module stop mode cleared
1	Module stop mode set

19.3 Medium-Speed Mode

When the SCK2 to SCK0 bits in SCKCR are set to 1, the operating mode changes to medium-speed mode as soon as the current bus cycle ends. In medium-speed mode, the CPU operates on the operating clock ($\phi/2$, $\phi/4$, $\phi/8$, $\phi/16$, or $\phi/32$) specified by the SCK2 to SCK0 bits. The bus masters other than the CPU (the DTC) also operate in medium-speed mode. On-chip supporting modules other than the bus masters always operate on the high-speed clock (ϕ).

In medium-speed mode, a bus access is executed in the specified number of states with respect to the bus master operating clock. For example, if $\phi/4$ is selected as the operating clock, on-chip memory is accessed in 4 states, and internal I/O registers in 8 states.

Medium-speed mode is cleared by clearing all of bits SCK2 to SCK0 to 0. A transition is made to high-speed mode and medium-speed mode is cleared at the end of the current bus cycle.

If a SLEEP instruction is executed when the SSBY bit in SBYCR is cleared to 0, a transition is made to sleep mode. When sleep mode is cleared by an interrupt, medium-speed mode is restored.

19.5 Module Stop Mode

19.5.1 Module Stop Mode

Module stop mode can be set for individual on-chip supporting modules.

When the corresponding MSTP bit in MSTPCR is set to 1, module operation stops at the end of the bus cycle and a transition is made to module stop mode. The CPU continues operating independently.

Table 19.3 shows MSTP bits and the corresponding on-chip supporting modules.

When the corresponding MSTP bit is cleared to 0, module stop mode is cleared and the module starts operating at the end of the bus cycle. In module stop mode, the internal states of modules other than the SCI and A/D converter are retained.

After reset clearance, all modules other than DTC are in module stop mode.

When an on-chip supporting module is in module stop mode, read/write access to its registers is disabled.

Do not make a transition to sleep mode with MSTPCR set to H'FFFF or H'EFFF, as this will halt operation of the bus controller.

Mnemonic		Operand Size	Addressing Mode/ Instruction Length (Bytes)								Operation	Condition Code						No. of States*1
			#xx	Rn	@ERn	@(d,ERn)	@-ERn/@ERn+	@aa	@(d,PC)	@@aa		I	H	N	Z	V	C	Advanced
SUB	SUB.W Rs,Rd	W	2								Rd16-Rs16→Rd16	—	[3]	↕	↕	↕	↕	1
	SUB.L #xx:32,ERd	L	6								ERd32-#xx:32→ERd32	—	[4]	↕	↕	↕	↕	3
	SUB.L ERs,ERd	L		2							ERd32-ERs32→ERd32	—	[4]	↕	↕	↕	↕	1
SUBX	SUBX #xx:8,Rd	B	2								Rd8-#xx:8-C→Rd8	—	↕	↕	[5]	↕	↕	1
	SUBX Rs,Rd	B		2							Rd8-Rs8-C→Rd8	—	↕	↕	[5]	↕	↕	1
SUBS	SUBS #1,ERd	L		2							ERd32-1→ERd32	—	—	—	—	—	—	1
	SUBS #2,ERd	L		2							ERd32-2→ERd32	—	—	—	—	—	—	1
	SUBS #4,ERd	L		2							ERd32-4→ERd32	—	—	—	—	—	—	1
DEC	DEC.B Rd	B		2							Rd8-1→Rd8	—	—	↕	↕	↕	—	1
	DEC.W #1,Rd	W		2							Rd16-1→Rd16	—	—	↕	↕	↕	—	1
	DEC.W #2,Rd	W		2							Rd16-2→Rd16	—	—	↕	↕	↕	—	1
	DEC.L #1,ERd	L		2							ERd32-1→ERd32	—	—	↕	↕	↕	—	1
	DEC.L #2,ERd	L		2							ERd32-2→ERd32	—	—	↕	↕	↕	—	1
DAS	DAS Rd	B		2							Rd8 decimal adjust→Rd8	—	*	↕	↕	*	—	1
MULXU	MULXU.B Rs,Rd	B		2							Rd8´Rs8→Rd16 (unsigned multiplication)	—	—	—	—	—	—	12
	MULXU.W Rs,ERd	W		2							Rd16´Rs16→ERd32 (unsigned multiplication)	—	—	—	—	—	—	20
MULXS	MULXS.B Rs,Rd	B		4							Rd8´Rs8→Rd16 (signed multiplication)	—	—	↕	↕	—	—	13
	MULXS.W Rs,ERd	W		4							Rd16´Rs16→ERd32 (signed multiplication)	—	—	↕	↕	—	—	21

Instruction	Mnemonic	Size	Instruction Format											
			1st byte		2nd byte		3rd byte	4th byte	5th byte	6th byte	7th byte	8th byte	9th byte	10th byte
ROTR	ROTR.B Rd	B	1	3	8	rd								
	ROTR.B #2, Rd	B	1	3	C	rd								
	ROTR.W Rd	W	1	3	9	rd								
	ROTR.W #2, Rd	W	1	3	D	rd								
	ROTR.L ERd	L	1	3	B	0 erd								
	ROTR.L #2, ERd	L	1	3	F	0 erd								
ROTXL	ROTXL.B Rd	B	1	2	0	rd								
	ROTXL.B #2, Rd	B	1	2	4	rd								
	ROTXL.W Rd	W	1	2	1	rd								
	ROTXL.W #2, Rd	W	1	2	5	rd								
	ROTXL.L ERd	L	1	2	3	0 erd								
	ROTXL.L #2, ERd	L	1	2	7	0 erd								
ROTXR	ROTXR.B Rd	B	1	3	0	rd								
	ROTXR.B #2, Rd	B	1	3	4	rd								
	ROTXR.W Rd	W	1	3	1	rd								
	ROTXR.W #2, Rd	W	1	3	5	rd								
	ROTXR.L ERd	L	1	3	3	0 erd								
	ROTXR.L #2, ERd	L	1	3	7	0 erd								
RTE	RTE	—	5	6	7	0								
RTS	RTS	—	5	4	7	0								
SHAL	SHAL.B Rd	B	1	0	8	rd								
	SHAL.B #2, Rd	B	1	0	C	rd								
	SHAL.W Rd	W	1	0	9	rd								
	SHAL.W #2, Rd	W	1	0	D	rd								
	SHAL.L ERd	L	1	0	B	0 erd								
	SHAL.L #2, ERd	L	1	0	F	0 erd								

TMDR5—Timer Mode Register 5 **H'FEA1** **TPU5**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	MD3	MD2	MD1	MD0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

Mode

0	0	0	0	Normal operation
			1	Reserved
		1	0	PWM mode 1
			1	PWM mode 2
	1	0	0	Phase counting mode 1
			1	Phase counting mode 2
		1	0	Phase counting mode 3
			1	Phase counting mode 4
1				—

: Don't care

Note: MD3 is a reserved bit. In a write, it should always be written with 0.

TIER5—Timer Interrupt Enable Register 5 H'FEA4 TPU5

Bit	7	6	5	4	3	2	1	0
	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
Initial value	0	1	0	0	0	0	0	0
Read/Write	R/W	—	R/W	R/W	—	—	R/W	R/W

TGR Interrupt Enable A

0	Interrupt request (TGIA) by TGFA bit disabled
1	Interrupt request (TGIA) by TGFA bit enabled

TGR Interrupt Enable B

0	Interrupt request (TGIB) by TGFB bit disabled
1	Interrupt request (TGIB) by TGFB bit enabled

Overflow Interrupt Enable

0	Interrupt request (TCIV) by TCFV disabled
1	Interrupt request (TCIV) by TCFV enabled

Underflow Interrupt Enable

0	Interrupt request (TCIU) by TCFU disabled
1	Interrupt request (TCIU) by TCFU enabled

A/D Conversion Start Request Enable

0	A/D conversion start request generation disabled
1	A/D conversion start request generation enabled

RAMER—RAM Emulation Register **H'FEDB** **Flash Memory**
(Valid only in F-ZTAT versions*)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	RAMS	RAM2	RAM1	RAM0
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	—	—	—	—	R/W	R/W	R/W	R/W

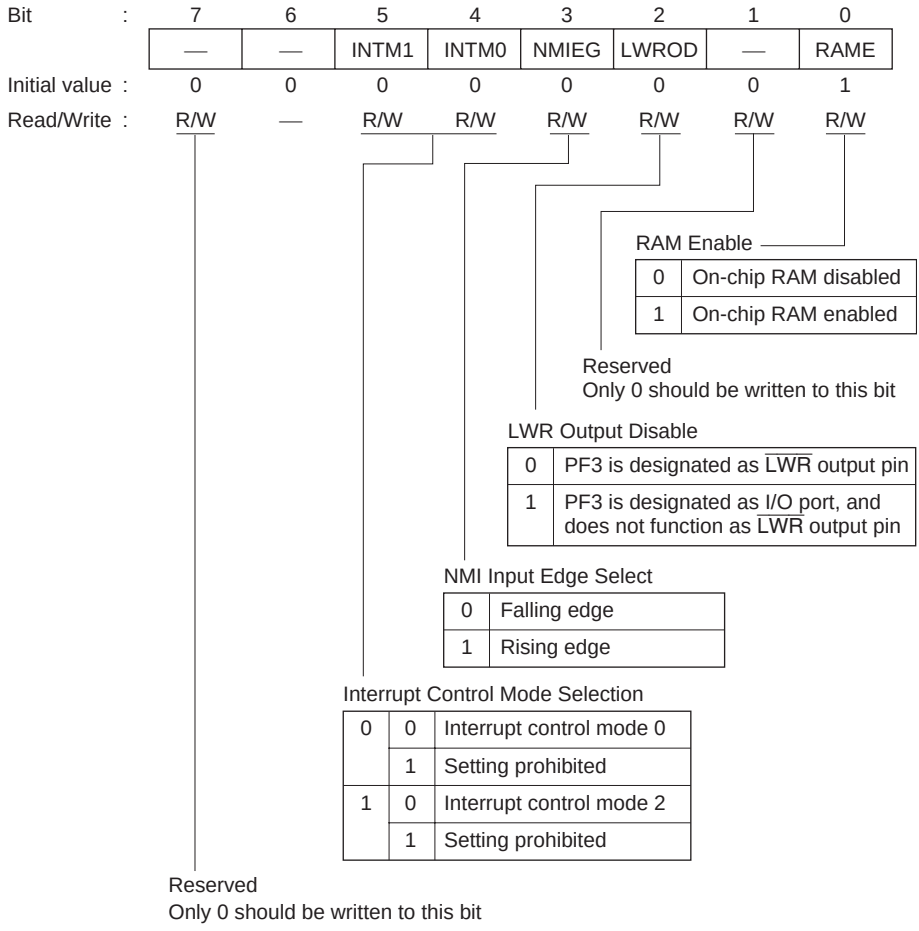
RAM Select, Flash Memory Area Select

RAMS	RAM2	RAM1	RAM0	RAM Area	Block Name
0				H'FFDC00 to H'FFEBFF	RAM area, 4 kbytes
1	0	0	0	H'000000 to H'000FFF	EB0 (4 kbytes)
			1	H'001000 to H'001FFF	EB1 (4 kbytes)
		1	0	H'002000 to H'002FFF	EB2 (4 kbytes)
			1	H'003000 to H'003FFF	EB3 (4 kbytes)
	1	0	0	H'004000 to H'004FFF	EB4 (4 kbytes)
			1	H'005000 to H'005FFF	EB5 (4 kbytes)
		1	0	H'006000 to H'006FFF	EB6 (4 kbytes)
			1	H'007000 to H'007FFF	EB7 (4 kbytes)

: Don't care

Note: * In the H8S/2314 F-ZTAT, this cannot be used and must not be accessed.

SYSCR—System Control Register **H'FF39** **MCU**



FLMCR1—Flash Memory Control Register 1 H'FFC8 Flash Memory (Valid in the H8S/2318 F-ZTAT, H8S/2317 F-ZTAT, H8S/2315 F-ZTAT, and H8S/2314 F-ZTAT only)

Bit	7	6	5	4	3	2	1	0
	FWE	SWE	ESU	PSU	EV	PV	E	P
Initial value	1/0*	0	0	0	0	0	0	0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Program*

0	Program mode cleared
1	Transition to program mode [Setting condition] When FWE = 1, SWE = 1, and PSU = 1

Note: * Valid for addresses H'000000 to H'03FFFF in H8S/2318 F-ZTAT, H'000000 to H'01FFFF in H8S/2317 F-ZTAT, and H'000000 to H'05FFFF in H8S/2315 F-ZTAT and H8S/2314 F-ZTAT.

Erase*

0	Erase mode cleared
1	Transition to erase mode [Setting condition] When FWE = 1, SWE = 1, and ESU = 1

Note: * Valid for addresses H'000000 to H'03FFFF in H8S/2318 F-ZTAT, H'000000 to H'01FFFF in H8S/2317 F-ZTAT, and H'000000 to H'05FFFF in H8S/2315 F-ZTAT and H8S/2314 F-ZTAT.

Program-Verify*

0	Program-verify mode cleared
1	Transition to program-verify mode [Setting condition] When FWE = 1 and SWE = 1

Note: * Valid for addresses H'000000 to H'03FFFF in H8S/2318 F-ZTAT, H'000000 to H'01FFFF in H8S/2317 F-ZTAT, and H'000000 to H'05FFFF in H8S/2315 F-ZTAT and H8S/2314 F-ZTAT.

Erase-Verify*

0	Erase-verify mode cleared
1	Transition to erase-verify mode [Setting condition] When FWE = 1 and SWE = 1

Note: * Valid for addresses H'000000 to H'03FFFF in H8S/2318 F-ZTAT, H'000000 to H'01FFFF in H8S/2317 F-ZTAT, and H'000000 to H'05FFFF in H8S/2315 F-ZTAT and H8S/2314 F-ZTAT.

Program Setup*

0	Program setup cleared
1	Program setup [Setting condition] When FWE = 1 and SWE = 1

Note: * Valid for addresses H'000000 to H'03FFFF in H8S/2318 F-ZTAT, H'000000 to H'01FFFF in H8S/2317 F-ZTAT, and H'000000 to H'05FFFF in H8S/2315 F-ZTAT and H8S/2314 F-ZTAT.

Erase Setup*

0	Erase setup cleared
1	Erase setup [Setting condition] When FWE = 1 and SWE = 1

Note: * Valid for addresses H'000000 to H'03FFFF in H8S/2318 F-ZTAT, H'000000 to H'01FFFF in H8S/2317 F-ZTAT, and H'000000 to H'05FFFF in H8S/2315 F-ZTAT and H8S/2314 F-ZTAT.

Software Write Enable*

0	Writes disabled
1	Writes enabled [Setting condition] When FWE = 1

Note: * Valid for addresses H'000000 to H'03FFFF in H8S/2318 F-ZTAT, H'000000 to H'01FFFF in H8S/2317 F-ZTAT, and H'000000 to H'05FFFF in H8S/2315 F-ZTAT and H8S/2314 F-ZTAT.

Flash Write Enable

0	When a low level is input to the FWE pin (hardware-protected state)
1	When a high level is input to the FWE pin

Note: * Determined by the state of the FWE pin.

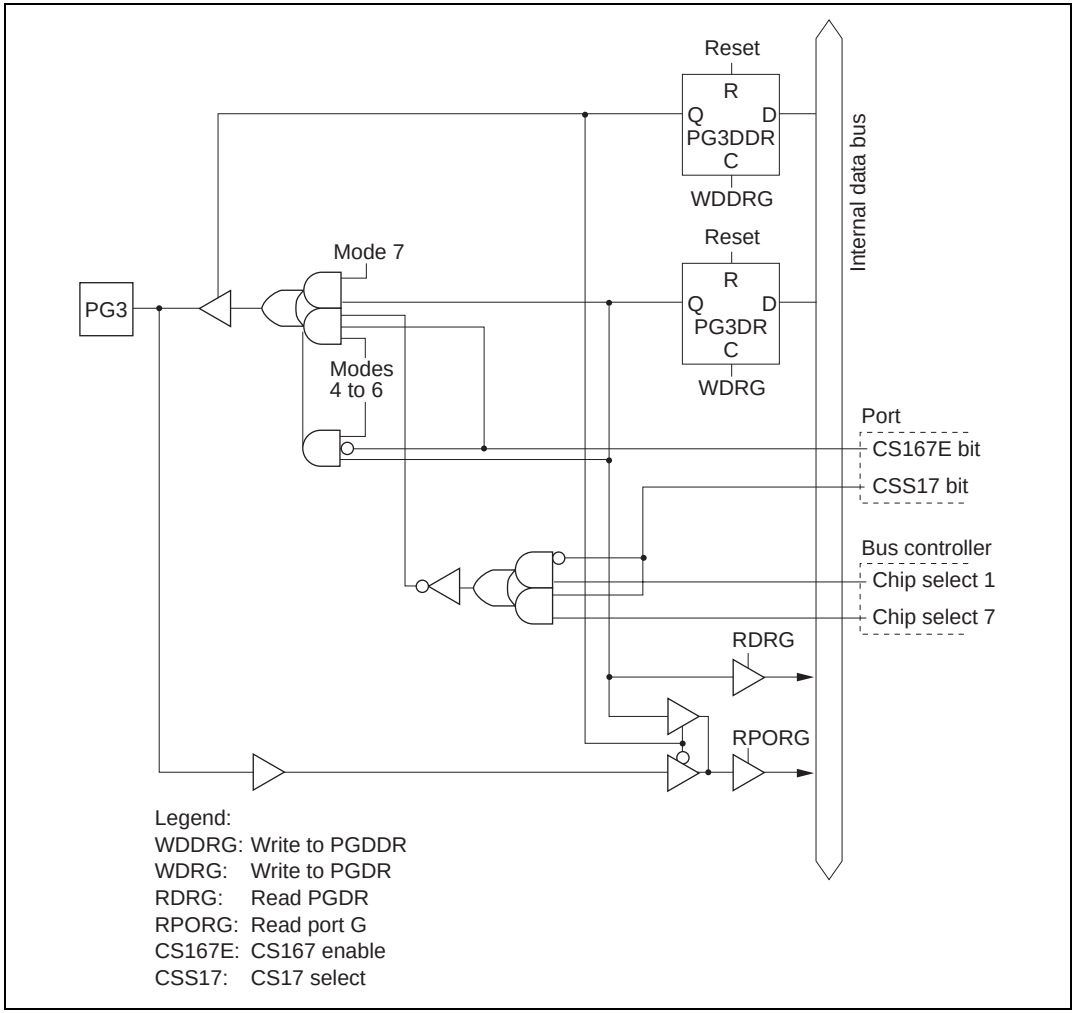


Figure C.11(d) Port G Block Diagram (Pin PG3)