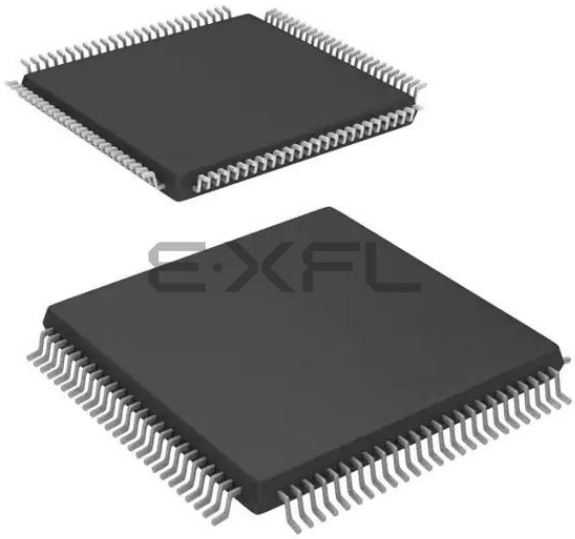

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	70
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2318vte25v

Contents

Table 5.4 Interrupt Sources, Vector Addresses, and Interrupt Priorities

Interrupt Source	Origin of Interrupt Source	Vector Number	Vector Address*	IPR	Priority	DTC Activation
Power-on reset		0	H'0000	—	High	—
Reserved		1	H'0004			
Reserved for system use		2	H'0008			
		3	H'000C			
		4	H'0010			
Trace		5	H'0014			
Reserved for system use		6	H'0018			
NMI	External pin	7	H'001C			
Trap instruction (4 sources)		8	H'0020			
		9	H'0024			
		10	H'0028			
		11	H'002C			
Reserved for system use		12	H'0030			
		13	H'0034			
		14	H'0038			
		15	H'003C			
IRQ0	External pin	16	H'0040	IPRA6 to IPRA4		○
IRQ1		17	H'0044	IPRA2 to IPRA0		○
IRQ2		18	H'0048	IPRB6 to IPRB4		○
IRQ3		19	H'004C			○
IRQ4		20	H'0050	IPRB2 to IPRB0		○
IRQ5		21	H'0054			○
IRQ6		22	H'0058	IPRC6 to IPRC4		○
IRQ7		23	H'005C		Low	○

6.4.5 Wait Control

When accessing external space, the H8S/2319 Group can extend the bus cycle by inserting one or more wait states (T_w). There are two ways of inserting wait states: program wait insertion and pin wait insertion using the $\overline{\text{WAIT}}$ pin.

Program Wait Insertion: From 0 to 3 wait states can be inserted automatically between the T_2 state and T_3 state on an individual area basis in 3-state access space, according to the settings of WCRH and WCRL.

Pin Wait Insertion: Setting the WAITE bit in BCRL to 1 enables wait insertion by means of the $\overline{\text{WAIT}}$ pin. When external space is accessed in this state, program wait insertion is first carried out according to the settings in WCRH and WCRL. Then, if the $\overline{\text{WAIT}}$ pin is low at the falling edge of ϕ in the last T_2 or T_w state, a T_w state is inserted. If the $\overline{\text{WAIT}}$ pin is held low, T_w states are inserted until it goes high.

This is useful when inserting four or more T_w states, or when changing the number of T_w states for different external devices.

The WAITE bit setting applies to all areas.

6.7 Bus Release

6.7.1 Overview

The chip can release the external bus in response to a bus request from an external device. In the external bus released state, the internal bus master continues to operate as long as there is no external access.

If an internal bus master wants to make an external access in the external bus released state, it can issue a bus request off-chip.

6.7.2 Operation

In external expansion mode, the bus can be released to an external device by setting the BRLE bit in BCRL to 1. Driving the $\overline{\text{BREQ}}$ pin low issues an external bus request to the chip. When the $\overline{\text{BREQ}}$ pin is sampled, at the prescribed timing the $\overline{\text{BACK}}$ pin is driven low, and the address bus, data bus, and bus control signals are placed in the high-impedance state, establishing the external bus released state.

In the external bus released state, an internal bus master can perform accesses using the internal bus. When an internal bus master wants to make an external access, it temporarily defers activation of the bus cycle, and waits for the bus request from the external bus master to be dropped.

If the BREQOE bit in BCRL is set to 1, when an internal bus master wants to make an external access in the external bus released state, the $\overline{\text{BREQO}}$ pin is driven low and a request can be made off-chip to drop the bus request.

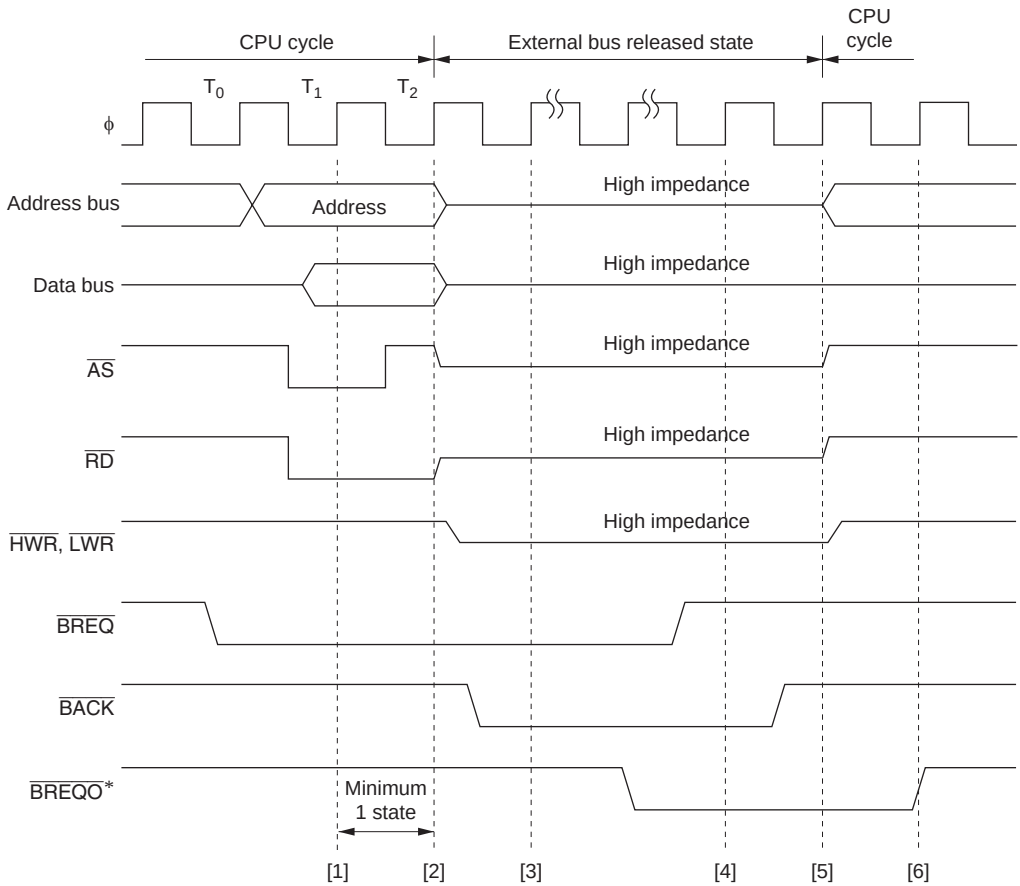
When the $\overline{\text{BREQ}}$ pin is driven high, the $\overline{\text{BACK}}$ pin is driven high at the prescribed timing and the external bus released state is terminated.

If an external bus release request and external access occur simultaneously, the order of priority is as follows:

(High) External bus release > Internal bus master external access (Low)

6.7.4 Transition Timing

Figure 6.19 shows the timing for transition to the bus released state.



[1] Low level of $\overline{\text{BREQ}}$ pin is sampled at rise of T_2 state.

[2] $\overline{\text{BACK}}$ pin is driven low at end of CPU read cycle, releasing bus to external bus master.

[3] $\overline{\text{BREQ}}$ pin state is still sampled in external bus released state.

[4] High level of $\overline{\text{BREQ}}$ pin is sampled.

[5] $\overline{\text{BACK}}$ pin is driven high, ending bus release cycle.

[6] $\overline{\text{BREQO}}$ signal goes high 1.5 clocks after $\overline{\text{BACK}}$ signal goes high.

Note: * Output only when BREQOE is set to 1.

Figure 6.19 Bus Released State Transition Timing

Port 2 Register (PORT2)

Bit	:	7	6	5	4	3	2	1	0
		P27	P26	P25	P24	P23	P22	P21	P20
Initial value	:	—*	—*	—*	—*	—*	—*	—*	—*
R/W	:	R	R	R	R	R	R	R	R

Note: * Determined by state of pins P27 to P20.

PORT2 is an 8-bit read-only register that shows the pin states. It cannot be written to. Writing of output data for the port 2 pins (P27 to P20) must always be performed on P2DR.

If a port 2 read is performed while P2DDR bits are set to 1, the P2DR values are read. If a port 2 read is performed while P2DDR bits are cleared to 0, the pin states are read.

After a reset and in hardware standby mode, PORT2 contents are determined by the pin states, as P2DDR and P2DR are initialized. PORT2 retains its prior state in software standby mode.

8.6.3 Pin Functions

Modes 4 and 5: In modes 4 and 5, the lower 4 bits of port A are designated as address outputs automatically.

Port A pin functions in modes 4 and 5 are shown in figure 8.6.

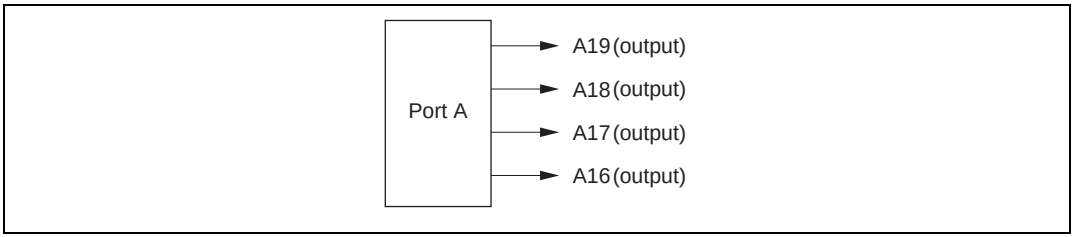


Figure 8.6 Port A Pin Functions (Modes 4 and 5)

Mode 6*: In mode 6*, port A pins function as address outputs or input ports. Input or output can be specified on an individual bit basis. Setting PADDR bits to 1 makes the corresponding port A pins address outputs, while clearing the bits to 0 makes the pins input ports.

Port A pin functions in mode 6 are shown in figure 8.7.

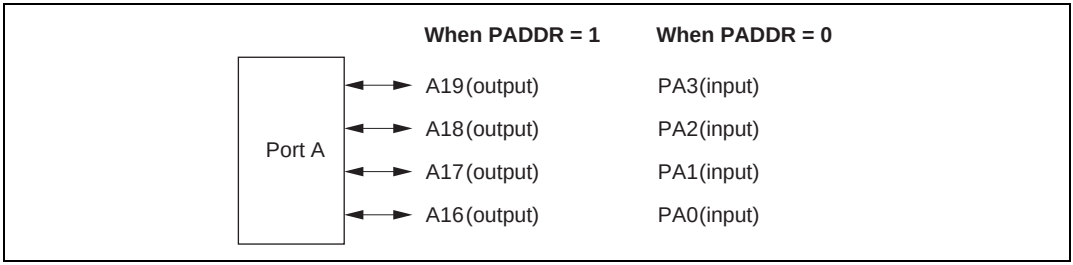


Figure 8.7 Port A Pin Functions (Mode 6)

Mode 7*: In mode 7*, port A pins function as I/O ports. Input or output can be specified for each pin on an individual bit basis. Setting PADDR bits to 1 makes the corresponding port A pins output ports, while clearing the bits to 0 makes the pins input ports.

Port A pin functions in mode 7 are shown in figure 8.8.

Port Function Control Register 1 (PFCR1)

Bit	:	7	6	5	4	3	2	1	0
		CSS17	CSS36	PF1CS5S	PF0CS4S	A23E	A22E	A21E	A20E
Initial value	:	0	0	0	0	1	1	1	1
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PFCR1 is an 8-bit readable/writable register that performs I/O port control. PFCR1 is initialized to H'0F by a reset, and in hardware standby mode.

Bit 7—CS17 Select (CSS17): Selects whether $\overline{CS1}$ or $\overline{CS7}$ is output from the PG3 pin. Change the CSS17 bit setting only when the corresponding DDR bit is 0. This bit is valid in modes 4 to 6.

Bit 7 CSS17	Description
0	PG3 is the PG3/$\overline{CS1}$ pin. $\overline{CS1}$ output is enabled when CS167E = 1 and PG3DDR = 1 (Initial value)
1	PG3 is the PG3/$\overline{CS7}$ pin. $\overline{CS7}$ output is enabled when CS167E = 1 and PG3DDR = 1

Bit 6—CS36 Select (CSS36): Selects whether $\overline{CS3}$ or $\overline{CS6}$ is output from the PG1 pin. Change the CSS36 bit setting only when the corresponding DDR bit is 0. This bit is valid in modes 4 to 6.

Bit 6 CSS36	Description
0	PG1 is the PG1/$\overline{IRQ7}$/$\overline{CS3}$ pin. $\overline{CS3}$ output is enabled when CS25E = 1 and PG1DDR = 1 (Initial value)
1	PG1 is the PG1/$\overline{IRQ7}$/$\overline{CS6}$ pin. $\overline{CS6}$ output is enabled when CS167E = 1 and PG1DDR = 1

Bit 5—Port F1 Chip Select 5 Select (PF1CS5S): Enables or disables $\overline{CS5}$ output. For details, see section 8.11, Port F.

Bit 4—Port F0 Chip Select 4 Select (PF0CS4S): Enables or disables $\overline{CS4}$ output. For details, see section 8.11, Port F.

Bit 3—Address 23 Enable (A23E): Enables or disables address output 23 (A23). For details, see section 8.2, Port 1.

Bit 2—Address 22 Enable (A22E): Enables or disables address output 22 (A22). For details, see section 8.2, Port 1.

9.1.2 Block Diagram

Figure 9.1 shows a block diagram of the TPU.

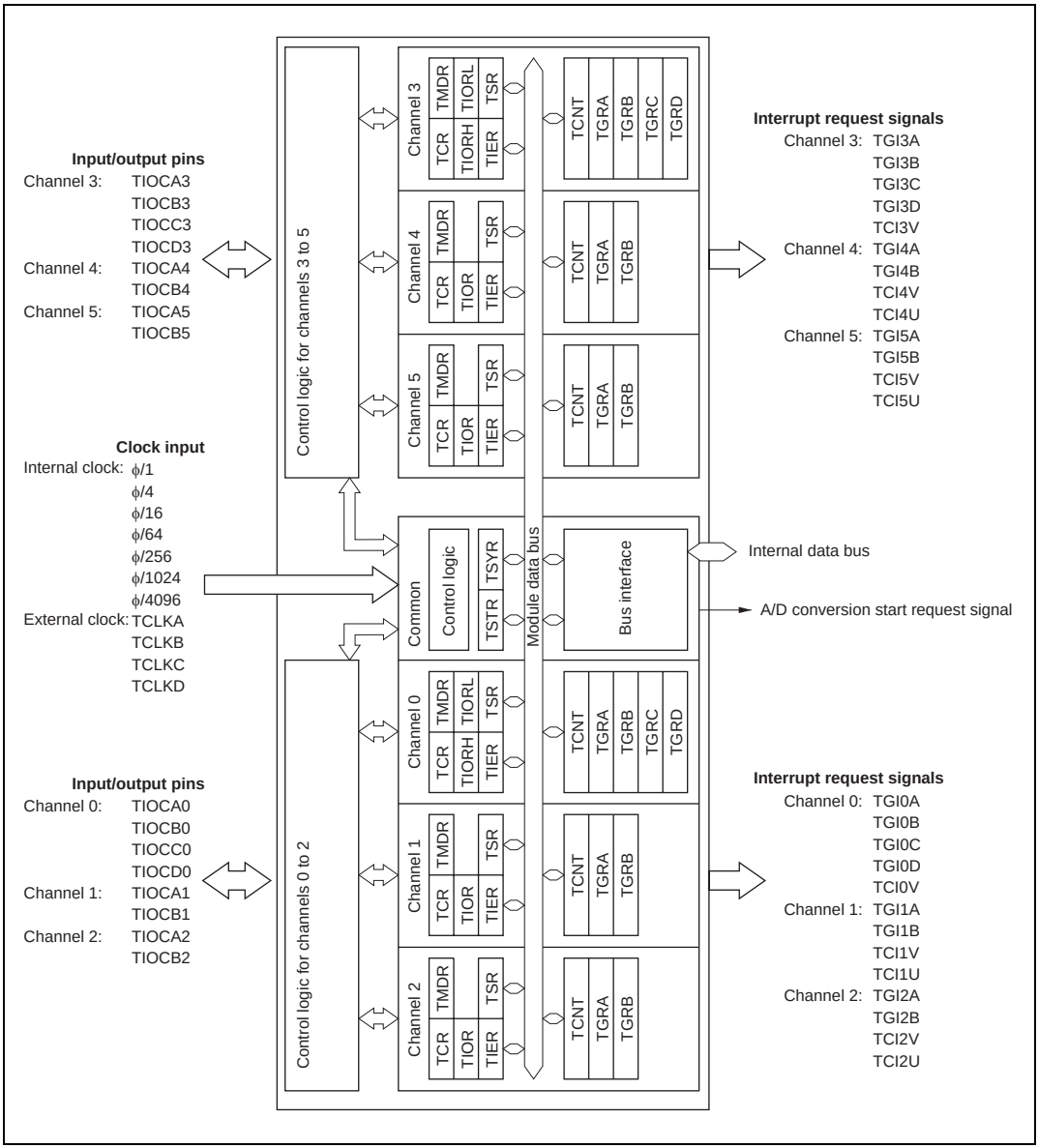


Figure 9.1 Block Diagram of TPU

Channel	Bit 7 IOD3	Bit 6 IOD2	Bit 5 IOD1	Bit 4 IOD0	Description		
3	0	0	0	0	TGR3D is output compare register*2	Output disabled	(Initial value)
				1		Initial output is 0 output	0 output at compare match
			1	0			1 output at compare match
				1			Toggle output at compare match
		1	0	0		Output disabled	
				1		Initial output is 1 output	0 output at compare match
			1	0			1 output at compare match
				1			Toggle output at compare match
	1	0	0	0	TGR3D is input capture register*2	Capture input source is TIOCD3 pin	Input capture at rising edge
				1			Input capture at falling edge
			1	×			Input capture at both edges
		1	×	×		Capture input source is channel 4/count clock	Input capture at TCNT4 count-up/count-down*1

×: Don't care

Notes: 1. When bits TPSC2 to TPSC0 in TCR4 are set to B'000 and φ/1 is used as the TCNT4 count clock, this setting is invalid and input capture is not generated.

2. When the BFB bit in TMDR3 is set to 1 and TGR3D is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Bit 6—Reserved: This bit cannot be modified and is always read as 1.

Bit 5—Underflow Flag (TCFU): Status flag that indicates that TCNT underflow has occurred when channels 1, 2, 4, and 5 are set to phase counting mode.

In channels 0 and 3, bit 5 is reserved. It is always read as 0 and cannot be modified.

Bit 5 TCFU	Description	
0	[Clearing condition] When 0 is written to TCFU after reading TCFU = 1	(Initial value)
1	[Setting condition] When the TCNT value underflows (changes from H'0000 to H'FFFF)	

Bit 4—Overflow Flag (TCFV): Status flag that indicates that TCNT overflow has occurred.

Bit 4 TCFV	Description	
0	[Clearing condition] When 0 is written to TCFV after reading TCFV = 1	(Initial value)
1	[Setting condition] When the TCNT value overflows (changes from H'FFFF to H'0000)	

Bit 3—Input Capture/Output Compare Flag D (TGFD): Status flag that indicates the occurrence of TGRD input capture or compare match in channels 0 and 3.

In channels 1, 2, 4, and 5, bit 3 is reserved. It is always read as 0 and cannot be modified.

Bit 3 TGFD	Description	
0	[Clearing conditions] • When DTC is activated by TGID interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFD after reading TGFD = 1	(Initial value)
1	[Setting conditions] • When TCNT = TGRD while TGRD is functioning as output compare register • When TCNT value is transferred to TGRD by input capture signal while TGRD is functioning as input capture register	

9.6 Operation Timing

9.6.1 Input/Output Timing

TCNT Count Timing: Figure 9.34 shows TCNT count timing in internal clock operation, and figure 9.35 shows TCNT count timing in external clock operation.

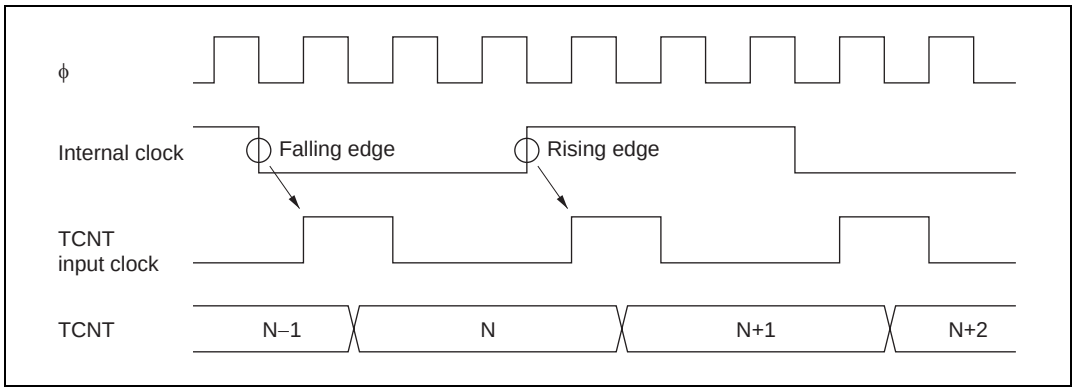


Figure 9.34 Count Timing in Internal Clock Operation

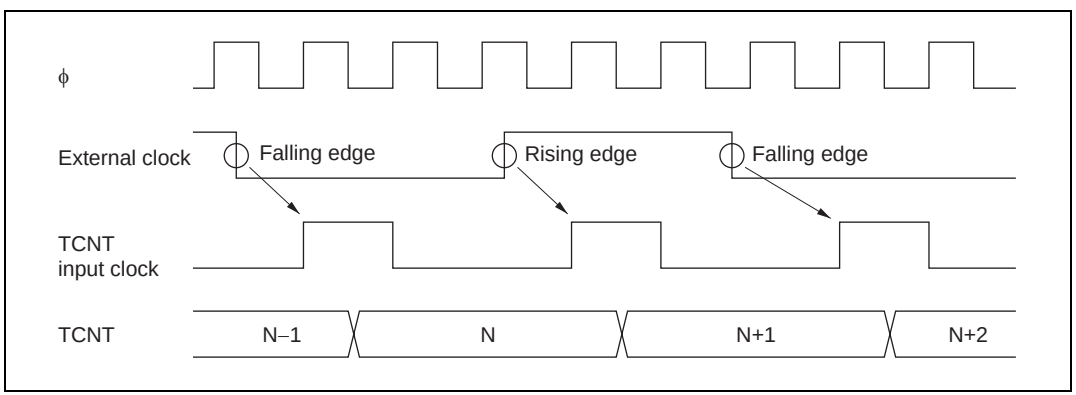


Figure 9.35 Count Timing in External Clock Operation

17.4.8 Pin Configuration

The flash memory is controlled by means of the pins shown in table 17.5.

Table 17.5 Flash Memory Pins

Pin Name	Abbreviation	I/O	Function
Reset	$\overline{\text{RES}}$	Input	Reset
Flash write enable	FWE	Input	Flash program/erase protection by hardware
Mode 2	MD2	Input	Sets MCU operating mode
Mode 1	MD1	Input	Sets MCU operating mode
Mode 0	MD0	Input	Sets MCU operating mode
Port F2	PF2	Input	Sets MCU operating mode in programmer mode
Port F1	PF1	Input	Sets MCU operating mode in programmer mode
Port F0	PF0	Input	Sets MCU operating mode in programmer mode
Transmit data	TxD1	Output	Serial transmit data output
Receive data	RxD1	Input	Serial receive data input

H8S/2318 F-ZTAT, H8S/2317 F-ZTAT, H8S/2315 F-ZTAT, H8S/2314 F-ZTAT			Socket Adapter (40-Pin Conversion)	HN27C4096HG (40 Pins)	
TFP-100B, TFP-100G	FP-100A	Pin Name		Pin No.	Pin Name
32	34	A_0		21	A_0
33	35	A_1		22	A_1
34	36	A_2		23	A_2
35	37	A_3		24	A_3
36	38	A_4		25	A_4
37	39	A_5		26	A_5
38	40	A_6		27	A_6
39	41	A_7		28	A_7
41	43	A_8		29	A_8
42	44	A_9		31	A_9
43	45	A_{10}		32	A_{10}
44	46	A_{11}		33	A_{11}
45	47	A_{12}		34	A_{12}
46	48	A_{13}		35	A_{13}
47	49	A_{14}		36	A_{14}
48	50	A_{15}		37	A_{15}
50	52	A_{16}		38	A_{16}
51	53	A_{17}		39	A_{17}
52	54	A_{18}		10	A_{18}
53	55	A_{19}		9	A_{19}
99	1	A_{20}		8	A_{20}
23	25	D_8		19	I/O_0
24	26	D_9		18	I/O_1
25	27	D_{10}		17	I/O_2
26	28	D_{11}		16	I/O_3
27	29	D_{12}		15	I/O_4
28	30	D_{13}		14	I/O_5
29	31	D_{14}		13	I/O_6
30	32	D_{15}		12	I/O_7
55	57	$\overline{CE}$		2	$\overline{CE}$
54	56	$\overline{OE}$		20	$\overline{OE}$
56	58	$\overline{WE}$		3	$\overline{WE}$
60	62	FWE		4	FWE
40, 63, 64, 65, 74, 77, 78, 98, 59	42, 65, 66, 67, 76, 79, 80, 100, 61	V_{CC}		1, 40	V_{CC}
				11, 30	V_{SS}
7, 18, 31, 49, 57, 58, 61, 68, ,75, 76, 87, 88, 90	9, 20, 33, 51, 59, 60, 63, 70, 77, 78, 89, 90, 92	V_{SS}		5, 6, 7	NC
62	64	$\overline{RES}$	Reset circuit *1		
66	68	XTAL	Oscillation circuit *2		
67	69	EXTAL			
Other pins		NC (OPEN)			

Legend:
FWE: Flash write enable
I/O_7 to I/O_0: Data input/output
A_{18} to A_0: Address input
$\overline{CE}$: Chip enable
$\overline{OE}$: Output enable
$\overline{WE}$: Write enable

Notes: This figure shows pin assignments, and does not show the entire socket adapter circuit.
1. A reset oscillation stabilization time (t_{osc1}) of at least 10 ms is required.
2. A 12-MHz crystal resonator should be used.

Figure 17.21 H8S/2318 F-ZTAT, H8S/2317 F-ZTAT, H8S/2315 F-ZTAT, H8S/2314 F-ZTAT Socket Adapter Pin Assignments

Bits 15 to 0—Frequency Set (F15 to F0): Set the operating frequency of the CPU. The setting value must be calculated as the following methods.

1. The operating frequency which is shown in MHz units must be rounded in a number to three decimal places and be shown in a number of two decimal places.
2. The centuplicated value is converted to the binary digit and is written to the FPEFEQ parameter (general register ER0). For example, when the operating frequency of the CPU is 25.000 MHz, the value is as follows.
   - The number to three decimal places of 25.000 is rounded and the value is thus 25.00.
   - The formula that 25.00 × 100 = 2500 is converted to the binary digit and b'0000,1001,1100,0100 (H'09C4) is set to ER0.

(b) Flash pass/fail parameter (FPFR: general register R0L of CPU)

This is the return value indicating the initialization result.

Bit :	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	FQ	SF
Initial value :	—	—	—	—	—	—	—	—
R/W :	—	—	—	—	—	—	R/W	R/W

Bits 7 to 2—Reserved: Return 0.

Bit 1—Frequency Error Detect (FQ): Returns the check result whether the specified operating frequency of the CPU is in the range of the supported operating frequency.

Bit 1

FQ	Description
0	Setting of operating frequency is normal
1	Setting of operating frequency is abnormal

Bit 0—Success/Fail (SF): Indicates whether initialization is completed normally.

Bit 0

SF	Description
0	Initialization is ended normally (no error)
1	Initialization is ended abnormally (error occurs)

17.26 Flash Memory Emulation in RAM

To provide real-time emulation in RAM of data that is to be written to the flash memory, a part of the RAM can be overlaid on an area of flash memory (user MAT) that has been specified by the RAM emulation register (RAMER). After the RAMER setting is made, the RAM is accessible in both the user MAT area and as the RAM area that has been overlaid on the user MAT area. Such emulation is possible in both user mode and user-program mode.

Figure 17.76 shows an example of the emulation of realtime programming of the user MAT area.

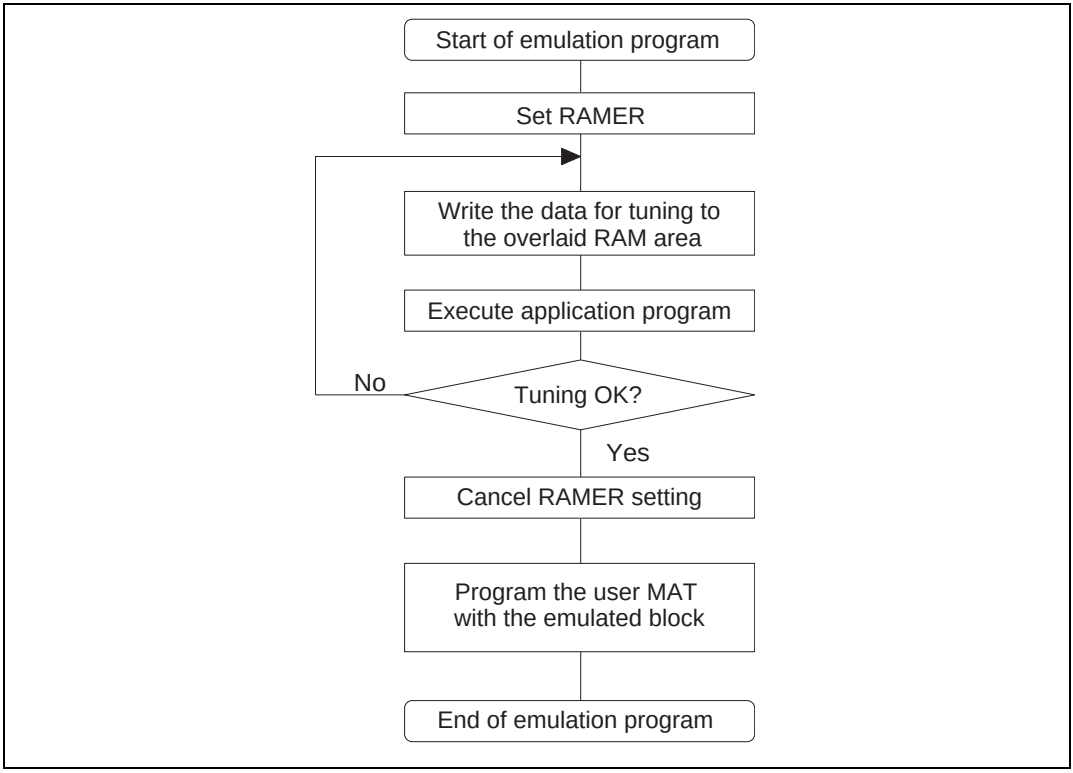


Figure 17.76 Emulation of Flash Memory in RAM

Instruction	Mnemonic	Instruction Fetch I	Branch Address Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
BIAND	BIAND #xx:3,Rd	1					
	BIAND #xx:3,@ERd	2			1		
	BIAND #xx:3,@aa:8	2			1		
	BIAND #xx:3,@aa:16	3			1		
	BIAND #xx:3,@aa:32	4			1		
BILD	BILD #xx:3,Rd	1					
	BILD #xx:3,@ERd	2			1		
	BILD #xx:3,@aa:8	2			1		
	BILD #xx:3,@aa:16	3			1		
	BILD #xx:3,@aa:32	4			1		
BIOR	BIOR #xx:8,Rd	1					
	BIOR #xx:8,@ERd	2			1		
	BIOR #xx:8,@aa:8	2			1		
	BIOR #xx:8,@aa:16	3			1		
	BIOR #xx:8,@aa:32	4			1		
BIST	BIST #xx:3,Rd	1					
	BIST #xx:3,@ERd	2			2		
	BIST #xx:3,@aa:8	2			2		
	BIST #xx:3,@aa:16	3			2		
	BIST #xx:3,@aa:32	4			2		
BIXOR	BIXOR #xx:3,Rd	1					
	BIXOR #xx:3,@ERd	2			1		
	BIXOR #xx:3,@aa:8	2			1		
	BIXOR #xx:3,@aa:16	3			1		
	BIXOR #xx:3,@aa:32	4			1		
BLD	BLD #xx:3,Rd	1					
	BLD #xx:3,@ERd	2			1		
	BLD #xx:3,@aa:8	2			1		
	BLD #xx:3,@aa:16	3			1		
	BLD #xx:3,@aa:32	4			1		

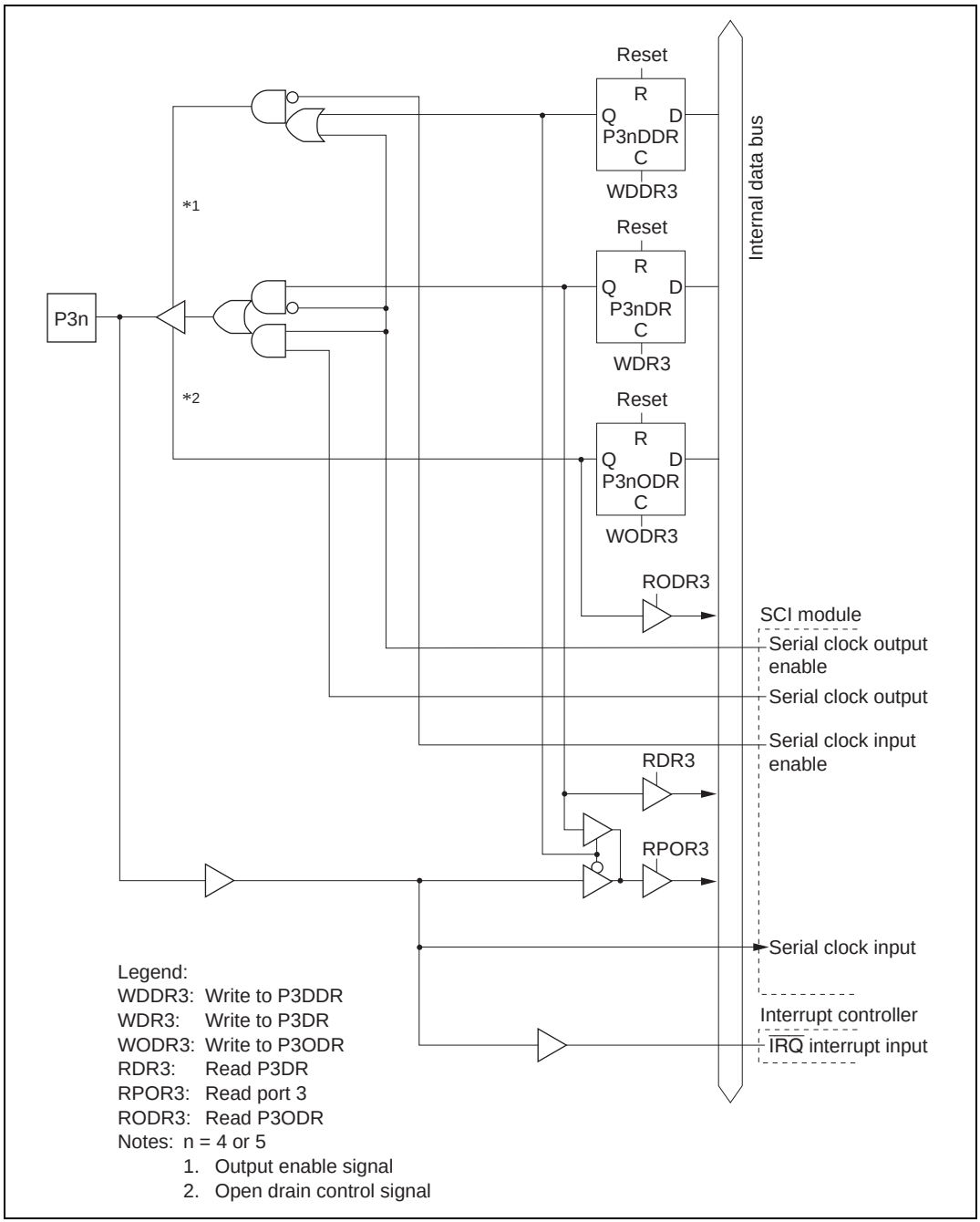


Figure C.3(c) Port 3 Block Diagram (Pins P34 and P35)