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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

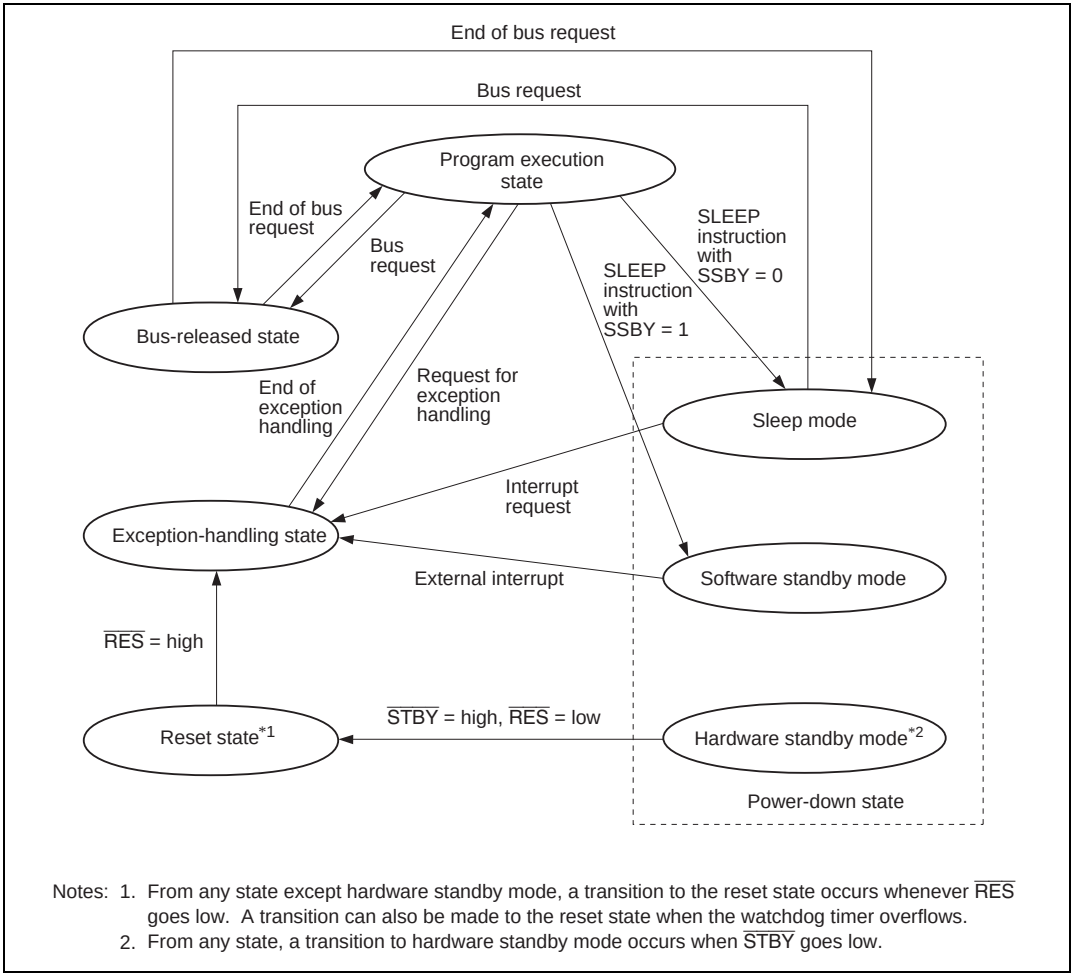
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	70
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2319evf25v

Item	Page	Revision (See Manual for Details)
17.8.3 Error Protection	604	Description amended (Before) • When a bus master other than the CPU (the DMAC or DTC) has control ... → (After) • When a bus master other than the CPU (the DTC) has control ...
17.11.2 Socket Adapters and Memory Map	609	Description added In programmer mode, ... figure 17.21. This enables the chip to fit a 40-pin socket. Figure 17.20 shows ...
17.13.1 Features	629	Description amended • Reprogramming capability The flash memory can be reprogrammed a minimum of 100 times.
17.17.3 Error Protection	664	Description amended (Before) • When a bus master other than the CPU (the DMAC or DTC) has control ... → (After) • When a bus master other than the CPU (the DTC) has control ...
17.20.2 Socket Adapters and Memory Map	670	Description added In programmer mode, ... figure 17.51. This enables the chip to fit a 40-pin socket. Figure 17.50 shows ...
17.22.1 Features	686	Description amended • Protection modes There are three protection modes: software protection by the register setting, hardware protection by reset/hardware standby, and error protection. The protection ...
17.22.4 Mode Comparison Table 17.46 Comparison of Programming Modes	690	Table 17.46 amended

	Boot mode	User program mode	User boot mode	PROM mode
Programming/ Erasing Environment	On-board programming	On-board programming	On-board programming	On-board programming
Programming/ Erasing Enable MAT	User MAT User boot MAT	User MAT	User MAT	User MAT User boot MAT
Program/Erase Control	Command method	Programming/ Erasing Interface	Programming/ Erasing Interface	Command method
All Erasure	○ (Automatic)	○	○	○ (Automatic)

17.23.2 Programming/Erasing Interface Parameter	704	Description amended ... the CPU except for ER0 and ER1 are stored. The return value of ... the registers except for ER0 and ER1, the stack area must be ...



Notes: 1. From any state except hardware standby mode, a transition to the reset state occurs whenever $\overline{RES}$ goes low. A transition can also be made to the reset state when the watchdog timer overflows.
2. From any state, a transition to hardware standby mode occurs when $\overline{STBY}$ goes low.

Figure 2.12 State Transitions

2.8.2 Reset State

When the $\overline{RES}$ input goes low all current processing stops and the CPU enters the reset state. All interrupts are masked in the reset state. Reset exception handling starts when the $\overline{RES}$ signal changes from low to high.

The reset state can also be entered by a watchdog timer overflow. For details, refer to section 11, Watchdog Timer.

As shown in table 5.3, multiple interrupts are assigned to one IPR. Setting a value in the range from H'0 to H'7 in the 3-bit groups of bits 6 to 4 and 2 to 0 sets the priority of the corresponding interrupt. The lowest priority level, level 0, is assigned by setting H'0, and the highest priority level, level 7, by setting H'7.

When interrupt requests are generated, the highest-priority interrupt according to the priority levels set in the IPR registers is selected. This interrupt level is then compared with the interrupt mask level set by the interrupt mask bits (I2 to I0) in the extend register (EXR) in the CPU, and if the priority level of the interrupt is higher than the set mask level, an interrupt request is issued to the CPU.

5.2.3 IRQ Enable Register (IER)

Bit	:	7	6	5	4	3	2	1	0
		IRQ7E	IRQ6E	IRQ5E	IRQ4E	IRQ3E	IRQ2E	IRQ1E	IRQ0E
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IER is an 8-bit readable/writable register that controls enabling and disabling of interrupt requests IRQ7 to IRQ0.

IER is initialized to H'00 by a reset and in hardware standby mode.

Bits 7 to 0—IRQ7 to IRQ0 Enable (IRQ7E to IRQ0E): These bits select whether IRQ7 to IRQ0 are enabled or disabled.

Bit n IRQnE	Description	
0	IRQn interrupts disabled	(Initial value)
1	IRQn interrupts enabled	

(n = 7 to 0)

Table 7.2 Chain Transfer Conditions

1st Transfer				2nd Transfer				
CHNE	**CHNS**	**DISEL**	**CR**	**CHNE**	**CHNS**	**DISEL**	**CR**	**DTC Transfer**
0	—	0	Not 0	—	—	—	—	Ends at 1st transfer
0	—	0	0	—	—	—	—	Ends at 1st transfer
0	—	1	—	—	—	—	—	Interrupt request to CPU
1	0	—	—	0	—	0	Not 0	Ends at 2nd transfer
				0	—	0	0	Ends at 2nd transfer
				0	—	1	—	Interrupt request to CPU
1	1	0	Not 0	—	—	—	—	Ends at 1st transfer
1	1	—	0	0	—	0	Not 0	Ends at 2nd transfer
				0	—	0	0	Ends at 2nd transfer
				0	—	1	—	Interrupt request to CPU
1	1	1	Not 0	—	—	—	—	Ends at 1st transfer
								Interrupt request to CPU

The DTC transfer mode can be normal mode, repeat mode, or block transfer mode.

The 24-bit SAR designates the DTC transfer source address and the 24-bit DAR designates the transfer destination address. After each transfer, SAR and DAR are independently incremented, decremented, or left fixed.

Table 7.3 outlines the functions of the DTC.

Table 7.3 DTC Functions

Transfer Mode	Activation Source	Address Registers	
		Transfer Source	Transfer Destination
• Normal mode — One transfer request transfers one byte or one word — Memory addresses are incremented or decremented by 1 or 2 — Up to 65,536 transfers possible • Repeat mode — One transfer request transfers one byte or one word — Memory addresses are incremented or decremented by 1 or 2 — After the specified number of transfers (1 to 256), the initial state resumes and operation continues • Block transfer mode — One transfer request transfers a block of the specified size — Block size is from 1 to 256 bytes or words — Up to 65,536 transfers possible — A block area can be designated at either the source or destination	• IRQ • TPU TGI • 8-bit timer CMI • SCI TXI or RXI • A/D converter ADI • Software	24 bits	24 bits

- Free-running count operation and periodic count operation

  Immediately after a reset, the TPU's TCNT counters are all designated as free-running counters. When the relevant bit in TSTR is set to 1 the corresponding TCNT counter starts up-count operation as a free-running counter. When TCNT overflows (from H'FFFF to H'0000), the TCFV bit in TSR is set to 1. If the value of the corresponding TCIEV bit in TIER is 1 at this point, the TPU requests an interrupt. After overflow, TCNT starts counting up again from H'0000.

  Figure 9.7 illustrates free-running counter operation.

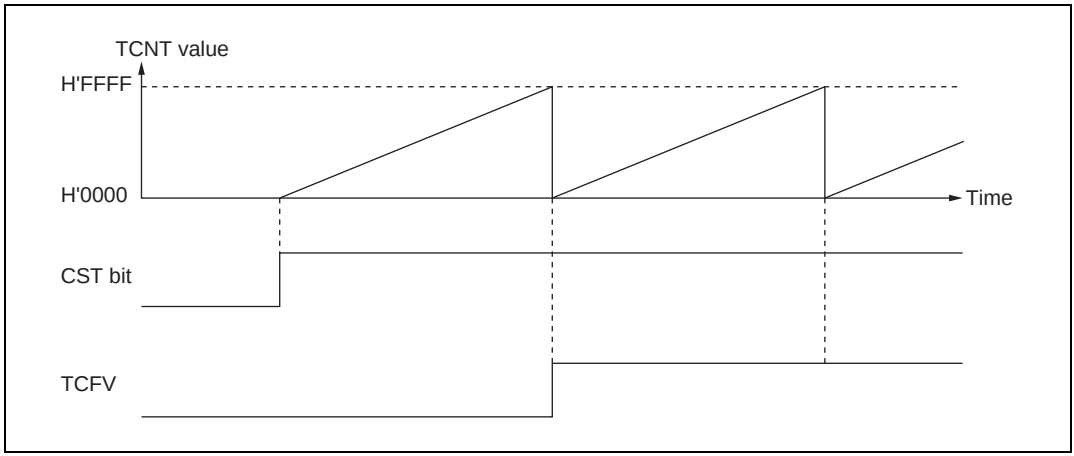


Figure 9.7 Free-Running Counter Operation

When compare match is selected as the TCNT clearing source, the TCNT counter for the relevant channel performs periodic count operation. The TGR register for setting the period is designated as an output compare register, and counter clearing by compare match is selected by means of bits CCLR2 to CCLR0 in TCR. After the settings have been made, TCNT starts up-count operation as a periodic counter when the corresponding bit in TSTR is set to 1. When the count value matches the value in TGR, the TGF bit in TSR is set to 1 and TCNT is cleared to H'0000.

If the value of the corresponding TGIE bit in TIER is 1 at this point, the TPU requests an interrupt. After a compare match, TCNT starts counting up again from H'0000.

Figure 9.8 illustrates periodic counter operation.

10.3 Operation

10.3.1 TCNT Incrementation Timing

TCNT is incremented by input clock pulses (either internal or external).

Internal Clock: Three different internal clock signals (ϕ/8, ϕ/64, or ϕ/8192) divided from the system clock (ϕ) can be selected, by setting bits CKS2 to CKS0 in TCR. Figure 10.2 shows the count timing.

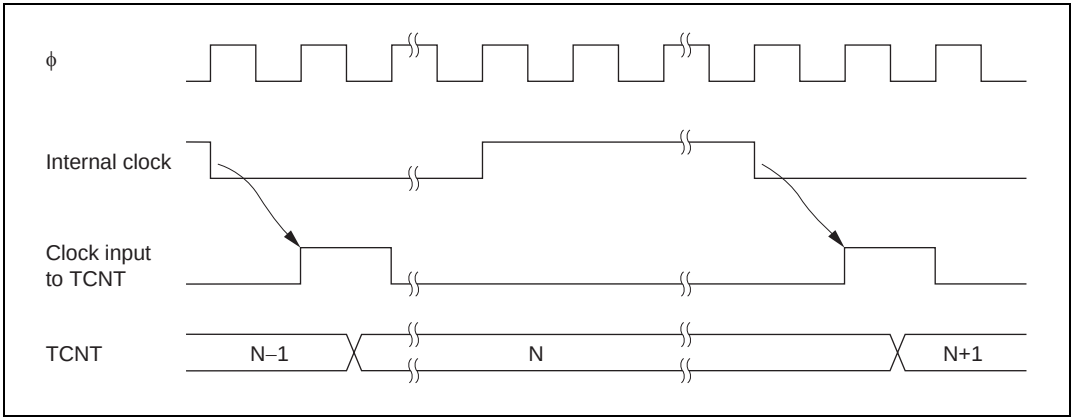


Figure 10.2 Count Timing for Internal Clock Input

External Clock: Three incrementation methods can be selected by setting bits CKS2 to CKS0 in TCR: at the rising edge, the falling edge, and both rising and falling edges.

Note that the external clock pulse width must be at least 1.5 states for incrementation at a single edge, and at least 2.5 states for incrementation at both edges. The counter will not increment correctly if the pulse width is less than these values.

Figure 10.3 shows the timing of incrementation at both edges of an external clock signal.

Section 11 Watchdog Timer

11.1 Overview

The chip has a single-channel on-chip watchdog timer (WDT) for monitoring system operation. The WDT outputs an overflow signal ($\overline{\text{WDTOVF}}$)* if a system crash prevents the CPU from writing to the timer counter, allowing it to overflow. At the same time, the WDT can also generate an internal reset signal for the chip.

When this watchdog function is not needed, the WDT can be used as an interval timer. In interval timer operation, an interval timer interrupt is generated each time the counter overflows.

Note: * The $\overline{\text{WDTOVF}}$ function is not available in the F-ZTAT versions.

11.1.1 Features

WDT features are listed below.

- Switchable between watchdog timer mode and interval timer mode
- $\overline{\text{WDTOVF}}$ output when in watchdog timer mode*
  If the counter overflows, the WDT outputs $\overline{\text{WDTOVF}}$. It is possible to select whether or not the entire chip is reset at the same time
- Interrupt generation when in interval timer mode
  If the counter overflows, the WDT generates an interval timer interrupt
- Choice of eight counter clock sources

Note: * The $\overline{\text{WDTOVF}}$ function is not available in the F-ZTAT versions.

Section 12 Serial Communication Interface (SCI)

12.1 Overview

The chip is equipped with a serial communication interface (SCI) that can handle both asynchronous and synchronous serial communication. A function is also provided for serial communication between processors (multiprocessor communication function).

12.1.1 Features

SCI features are listed below.

- Choice of asynchronous or synchronous serial communication mode

  Asynchronous mode
  - — Serial data communication executed using an asynchronous system in which synchronization is achieved character by character
  - — Serial data communication can be carried out with standard asynchronous communication chips such as a Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communication Interface Adapter (ACIA)
  - — A multiprocessor communication function is provided that enables serial data communication with a number of processors
  - — Choice of 12 serial data transfer formats

    Data length : 7 or 8 bits

    Stop bit length : 1 or 2 bits

    Parity : Even, odd, or none

    Multiprocessor bit : 1 or 0
  - — Receive error detection : Parity, overrun, and framing errors
  - — Break detection : Break can be detected by reading the RxD pin level directly in case of a framing error

  Synchronous mode
  - — Serial data communication synchronized with a clock
  - — Serial data communication can be carried out with other chips that have a synchronous communication function
  - — One serial data transfer format

    Data length : 8 bits
  - — Receive error detection : Overrun errors detected

Bit 3—Smart Card Data Transfer Direction (SDIR): Selects the serial/parallel conversion format.

This bit is valid when 8-bit data is used as the transmit/receive format.

Bit 3 SDIR	Description	
0	TDR contents are transmitted LSB-first	(Initial value)
	Receive data is stored in RDR LSB-first	
1	TDR contents are transmitted MSB-first	
	Receive data is stored in RDR MSB-first	

Bit 2—Smart Card Data Invert (SINV): Specifies inversion of the data logic level. The SINV bit does not affect the logic level of the parity bit(s): parity bit inversion requires inversion of the O/$\overline{E}$ bit in SMR.

Bit 2 SINV	Description	
0	TDR contents are transmitted without modification	(Initial value)
	Receive data is stored in RDR without modification	
1	TDR contents are inverted before being transmitted	
	Receive data is stored in RDR in inverted form	

Bit 1—Reserved: This bit cannot be modified and is always read as 1.

Bit 0—Smart Card Interface Mode Select (SMIF): When the smart card interface operates as a normal SCI, 0 should be written to this bit.

Bit 0 SMIF	Description	
0	Operates as normal SCI (smart card interface function disabled)	(Initial value)
1	Smart card interface function enabled	

Bit 3—Flash Memory Control Register Enable (FLSHE): Controls CPU access to the flash memory control registers (FLMCR1, FLMCR2, EBR1, and EBR2). Writing 1 to the FLSHE bit enables the flash memory control registers to be read and written to. Clearing FLSHE to 0 designates these registers as unselected (the register contents are retained).

Bit 3 FLSHE	Description
0	Flash control registers are not selected for addresses H'FFFFC8 to H'FFFFCB (Initial value)
1	Flash control registers are selected for addresses H'FFFFC8 to H'FFFFCB

Bits 2 to 0—Reserved: These bits cannot be modified and are always read as 0.

17.5.6 RAM Emulation Register (RAMER)

Bit	:	7	6	5	4	3	2	1	0
		—	—	—	—	RAMS	RAM2	RAM1	RAM0
Initial value	:	0	0	0	0	0	0	0	0
R/W	:	—	—	—	—	R/W	R/W	R/W	R/W

RAMER specifies the area of flash memory to be overlapped with part of RAM when emulating real-time flash memory programming. RAMER is initialized to H'00 by a reset and in hardware standby mode. It is not initialized in software standby mode. RAMER settings should be made in user mode or user program mode.

Flash memory area divisions are shown in table 17.8. To ensure correct operation of the emulation function, the ROM for which RAM emulation is performed should not be accessed immediately after this register has been modified. Normal execution of an access immediately after register modification is not guaranteed.

Note: RAM emulation function is not supported in the H8S/2314 F-ZTAT.

Bits 7 to 4—Reserved: These bits cannot be modified and are always read as 0.

17.14 Register Descriptions

17.14.1 Flash Memory Control Register 1 (FLMCR1)

Bit	:	7	6	5	4	3	2	1	0
		FWE1	SWE1	ESU1	PSU1	EV1	PV1	E1	P1
Initial value	:	1	0	0	0	0	0	0	0
R/W	:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

FLMCR1 is an 8-bit register used for flash memory operating mode control. Program-verify mode or erase-verify mode for addresses H'000000 to H'03FFFF is entered by setting SWE1 to 1 then setting the EV1 or PV1 bit. Program mode for addresses H'000000 to H'03FFFF is entered by setting SWE1 to 1 then setting the PSU1 bit, and finally setting the P1 bit. Erase mode for addresses H'000000 to H'03FFFF is entered by setting SWE1 to 1 then setting the ESU1 bit, and finally setting the E1 bit. FLMCR1 is initialized to H'80 by a reset, and in hardware standby mode and software standby mode. When on-chip flash memory is disabled, a read will return H'00, and writes are invalid.

Writes to bits ESU1, PSU1, EV1, and PV1 only when SWE1 = 1; writes to the E1 bit only when SWE1 = 1, and ESU1 = 1; and writes to the P1 bit only when SWE1 = 1, and PSU1 = 1.

Bit 7—Flash Write Enable Bit (FWE): Sets hardware protection against flash memory programming/erasing. This bit cannot be modified and is always read as 1 in this model.

Bit 6—Software Write Enable Bit 1 (SWE1): Enables or disables flash memory programming and erasing for addresses H'000000 to H'03FFFF. This bit should be set when setting FLMCR1 bits 5 to 0, EBR1 bits 7 to 0, and EBR2 bits 3 to 0.

When SWE1 = 1, the flash memory can only be read in program-verify or erase-verify mode.

Bit 6 SWE1	Description	
0	Writes disabled	(Initial value)
1	Writes enabled	

17.20 Flash Memory Programmer Mode

17.20.1 Programmer Mode Setting

Programs and data can be written and erased in programmer mode as well as in the on-board programming modes. In programmer mode, the on-chip ROM can be freely programmed using a PROM programmer that supports the Renesas Technology microcomputer device type with 512-kbyte on-chip flash memory (FZTAT512V3A). Flash memory read mode, auto-program mode, auto-erase mode, and status read mode are supported with this device type. In auto-program mode, auto-erase mode, and status read mode, a status polling procedure is used, and in status read mode, detailed internal signals are output after execution of an auto-program or auto-erase operation.

Table 17.34 shows programmer mode pin settings.

Table 17.34 Programmer Mode Pin Settings

Pin Names	Settings/External Circuit Connection
Mode pins: MD2, MD1, MD0	Low-level input
Mode setting pins: PF2, PF1, PF0	High-level input to PF2, low-level input to PF1 and PF0
$\overline{\text{STBY}}$ pin	High-level input (do not select hardware standby mode)
$\overline{\text{RES}}$ pin	Reset circuit
XTAL, EXTAL pins	Oscillator circuit
Other pins requiring setting: P23, P25	High-level input to P23, low-level input to P25

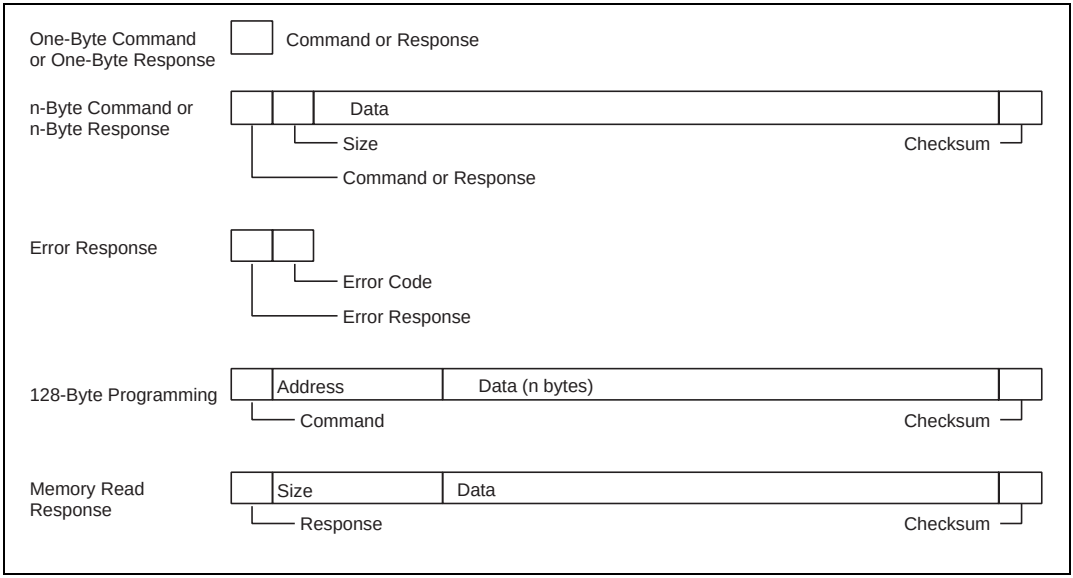


Figure 17.84 Communication Protocol Format

- Command (1 byte): Commands including inquiries, selection, programming, erasing, and checking
- Response (1 byte): Response to an inquiry
- Size (1 byte): The amount of data for transmission excluding the command, amount of data, and checksum
- Checksum (1 byte): The checksum is calculated so that the total of all values from the command byte to the SUM byte becomes H'00
- Data (n bytes): Detailed data of a command or response
- Error Response (1 byte): Error response to a command
- Error Code (1 byte): Type of the error
- Address (4 bytes): Address for programming
- Data (n bytes): Data to be programmed (the size is indicated in the response to the programming unit inquiry.)
- Size (4 bytes): Four-byte response to a memory read

19.5 Module Stop Mode

19.5.1 Module Stop Mode

Module stop mode can be set for individual on-chip supporting modules.

When the corresponding MSTP bit in MSTPCR is set to 1, module operation stops at the end of the bus cycle and a transition is made to module stop mode. The CPU continues operating independently.

Table 19.3 shows MSTP bits and the corresponding on-chip supporting modules.

When the corresponding MSTP bit is cleared to 0, module stop mode is cleared and the module starts operating at the end of the bus cycle. In module stop mode, the internal states of modules other than the SCI and A/D converter are retained.

After reset clearance, all modules other than DTC are in module stop mode.

When an on-chip supporting module is in module stop mode, read/write access to its registers is disabled.

Do not make a transition to sleep mode with MSTPCR set to H'FFFF or H'EFFF, as this will halt operation of the bus controller.

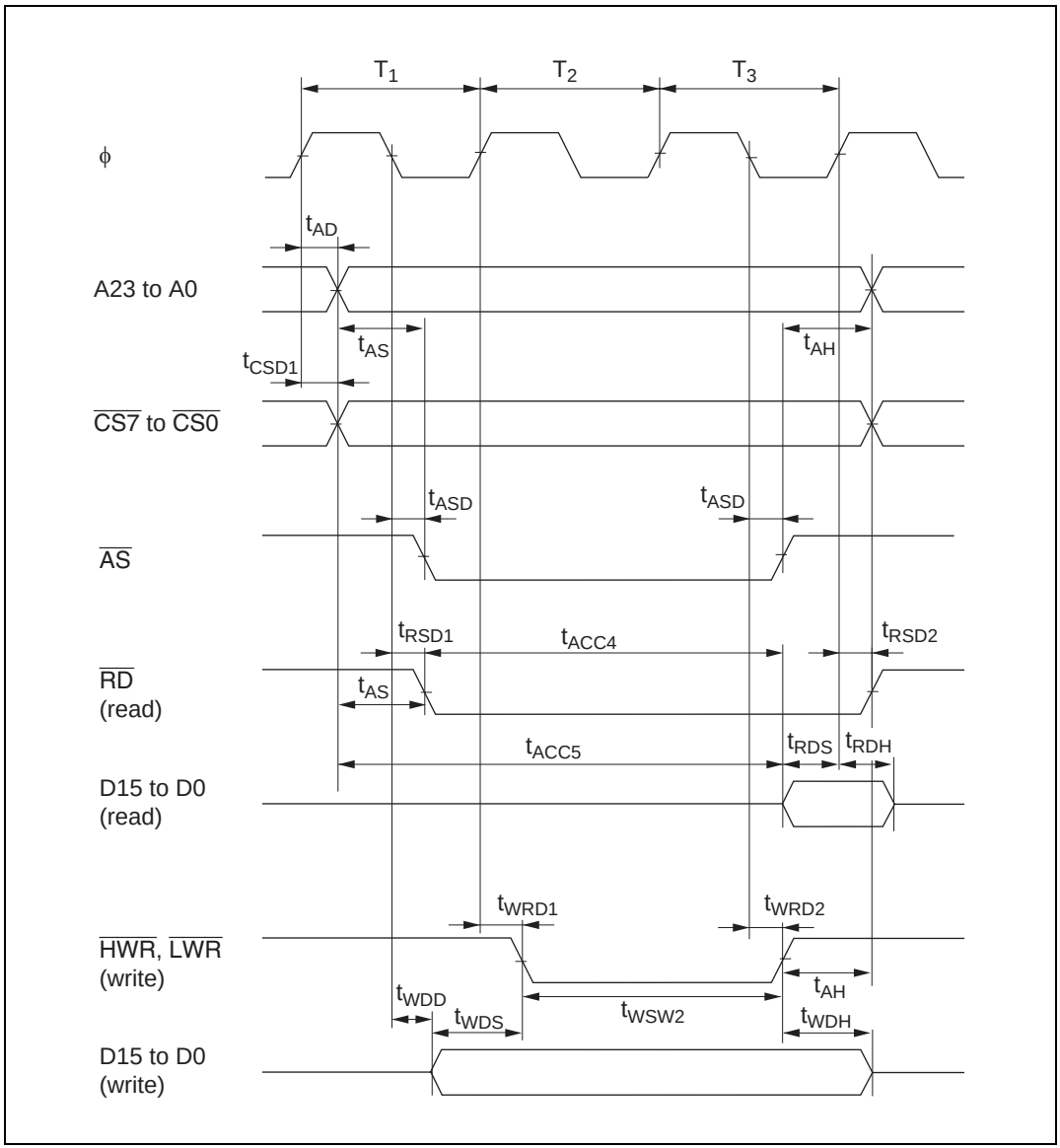


Figure 20.7 Basic Bus Timing (3-State Access)

(8) Block Transfer Instructions

Mnemonic		Operand Size	Addressing Mode/ Instruction Length (Bytes) #xx	Rn	@ERn	@(d,ERn)	@-ERn/@ERn+	@aa	@(d,PC)	@@aa	|	Operation	Condition Code I	H	N	Z	V	C	No. of States*1 Advanced
EEPMOV	EEPMOV.B	—									4	if R4L≠0 Repeat @ER5→@ER6 ER5+1→ER5 ER6+1→ER6 R4L-1→R4L Until R4L=0 else next;	—	—	—	—	—	—	4+2n*2
	EEPMOV.W	—									4	if R4≠0 Repeat @ER5→@ER6 ER5+1→ER5 ER6+1→ER6 R4-1→R4 Until R4=0 else next;	—	—	—	—	—	—	4+2n*2

Notes: 1. The number of states is the number of states required for execution when the instruction and its operands are located in on-chip memory.
2. n is the initial value of R4L or R4.
3. Only register ER0, ER1, ER4, or ER5 should be used when using the TAS instruction.
[1] Seven states for saving or restoring two registers, nine states for three registers, or eleven states for four registers.
[2] Cannot be used in the chip.
[3] Set to 1 when a carry or borrow occurs at bit 11; otherwise cleared to 0.
[4] Set to 1 when a carry or borrow occurs at bit 27; otherwise cleared to 0.
[5] Retains its previous value when the result is zero; otherwise cleared to 0.
[6] Set to 1 when the divisor is negative; otherwise cleared to 0.
[7] Set to 1 when the divisor is zero; otherwise cleared to 0.
[8] Set to 1 when the quotient is negative; otherwise cleared to 0.
[9] One additional state is required for execution when EXR is valid.

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FE90	TCR4	—	CCLR1	CCLR0	CKEG	CKEG0	TPSC2	TPSC1	TPSC0	TPU4	16 bits
H'FE91	TMDR4	—	—	—	—	MD3	MD2	MD1	MD0		
H'FE92	TIOR4	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FE94	TIER4	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA		
H'FE95	TSR4	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA		
H'FE96	TCNT4										
H'FE97											
H'FE98	TGR4A										
H'FE99											
H'FE9A	TGR4B										
H'FE9B											
H'FEA0	TCR5	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	TPU5	16 bits
H'FEA1	TMDR5	—	—	—	—	MD3	MD2	MD1	MD0		
H'FEA2	TIOR5	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0		
H'FEA4	TIER5	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA		
H'FEA5	TSR5	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA		
H'FEA6	TCNT5										
H'FEA7											
H'FEA8	TGR5A										
H'FEA9											
H'FEAA	TGR5B										
H'FEAB											
H'FEB0	P1DDR	P17DDR	P16DDR	P15DDR	P14DDR	P13DDR	P12DDR	P11DDR	P10DDR	Ports	8 bits
H'FEB1	P2DDR	P27DDR	P26DDR	P25DDR	P24DDR	P23DDR	P22DDR	P21DDR	P20DDR		
H'FEB2	P3DDR	—	—	P35DDR	P34DDR	P33DDR	P32DDR	P31DDR	P30DDR		
H'FEB9	PADDR	—	—	—	—	PA3DDR	PA2DDR	PA1DDR	PA0DDR		
H'FEBA	PBDDR	PB7DDR	PB6DDR	PB5DDR	PB4DDR	PB3DDR	PB2DDR	PB1DDR	PB0DDR		
H'FEBB	PCDDR	PC7DDR	PC6DDR	PC5DDR	PC4DDR	PC3DDR	PC2DDR	PC1DDR	PC0DDR		
H'FEBC	PDDDR	PD7DDR	PD6DDR	PD5DDR	PD4DDR	PD3DDR	PD2DDR	PD1DDR	PD0DDR		
H'FEBD	PEDDR	PE7DDR	PE6DDR	PE5DDR	PE4DDR	PE3DDR	PE2DDR	PE1DDR	PE0DDR		
H'FEBE	PFDDR	PF7DDR	PF6DDR	PF5DDR	PF4DDR	PF3DDR	PF2DDR	PF1DDR	PF0DDR		
H'FEBF	PGDDR	—	—	—	PG4DDR	PG3DDR	PG2DDR	PG1DDR	PG0DDR		

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name	Data Bus Width
H'FF78	SMR0	C/$\overline{A}$/ GM*3	CHR/ BLK*4	PE	O/$\overline{E}$	STOP/ BCP1*5	MP/ BCP0*6	CKS1	CKS0	SCI0, smart card interface 0	8 bits
H'FF79	BRR0										
H'FF7A	SCR0	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0		
H'FF7B	TDR0										
H'FF7C	SSR0	TDRE	RDRF	ORER	FER/ ERS*7	PER	TEND	MPB	MPBT		
H'FF7D	RDR0										
H'FF7E	SCMR0	—	—	—	—	SDIR	SINV	—	SMIF		
H'FF80	SMR1	C/$\overline{A}$/ GM*4	CHR/ BLK*5	PE	O/$\overline{E}$	STOP/ BCP1*6	MP/ BCP0*7	CKS1	CKS0	SCI1, smart card interface 1	8 bits
H'FF81	BRR1										
H'FF82	SCR1	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0		
H'FF83	TDR1										
H'FF84	SSR1	TDRE	RDRF	ORER	FER/ ERS*8	PER	TEND	MPB	MPBT		
H'FF85	RDR1										
H'FF86	SCMR1	—	—	—	—	SDIR	SINV	—	SMIF		
H'FE90	ADDRAH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	A/D converter	8 bits
H'FE91	ADDRAL	AD1	AD0	—	—	—	—	—	—		
H'FE92	ADDRBH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FE93	ADDRBL	AD1	AD0	—	—	—	—	—	—		
H'FE94	ADDRCH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FE95	ADDRCL	AD1	AD0	—	—	—	—	—	—		
H'FE96	ADDRDH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2		
H'FE97	ADDRDL	AD1	AD0	—	—	—	—	—	—		
H'FE98	ADCSR	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0		
H'FE99	ADCR	TRGS1	TRGS0	—	—	CKS1	—	—	—		

FTDAR—Flash Transfer Destination Address Register H'FFCA FLASH
(Valid only in the H8S/2319C F-ZTAT)

Bit	7	6	5	4	3	2	1	0
	TDER	TDA6	TDA5	TDA4	TDA3	TDA2	TDA1	TDA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Transfer Destination Address

TDA6 to TDA0	Description
H'00	Download start address is set to H'FFBC00
H'01	Download start address is set to H'FFCC00
H'02	Download start address is set to H'FFDC00
H'03	Download start address is set to H'FFEC00
H'04 to H'7F	Setting prohibited. If this value is set, the TDER bit (bit 7) is set to 1 to abort the download processing

Transfer Destination Address Setting Error

0	Setting of TDA6 to TDA0 is normal
1	Setting of TDER and TDA4 to TDA0 is H'04 to H'FF and download has been aborted