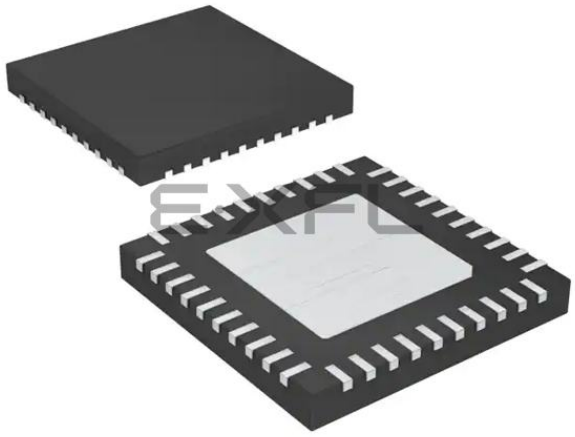

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	MAXQ20
Core Size	16-Bit
Speed	10MHz
Connectivity	3-Wire, I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	2.97V ~ 3.63V
Data Converters	A/D 18x13b; D/A 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-TQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds4830t-t

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND.....-0.3V to +3.63V
SCL, SDA, $\overline{RST}$.....-0.3V to +3.63V
All Other Pins to GND
except REG18 and REG285 .....-0.3V to (V_{DD} + 0.3V)*
Continuous Sink Current .....20mA per pin, 50mA total
Continuous Source Current.....20mA per pin, 50mA total
Operating Temperature Range.....-40°C to +85°C
Storage Temperature Range.....-55°C to +125°C
Lead Temperature (soldering, 10s) .....…+300°C
Soldering Temperature (reflow) .....…+260°C

**Subject to not exceeding +3.63V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Operating Voltage	V_{DD}	(Note 1)	3.0		3.6	V
Input Logic-High	V_{IH}		0.7 x V_{DD}		V_{DD} + 0.3	V
Input Logic-Low	V_{IL}		-0.3		0.3 x V_{DD}	V
Input Logic-High: SCL, SDA, MCL, MSDA	V_{I2C_IH}	(Note 1)	2.1		V_{DD} + 0.3	V
Input Logic-Low: SCL, SDA, MCL, MSDA	V_{I2C_IL}	(Note 1)	-0.5		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CPU}	CPU mode, all analog disabled (Notes 2, 3)		4.8		mA
	$I_{FASTCOMP}$			2		
	$I_{SAMPLEHOLDS}$	Both sample/hold		1.5		
	I_{ADC}			2.8		
	I_{DACS}	Per channel (Note 4)		0.6		
Brownout Voltage	V_{BO}	Monitors V_{DD} (Note 1)		2.7		V
Brownout Hysteresis	V_{BOH}	Monitors V_{DD} (Note 1)		0.07		V
1.8V Regulator Initial Voltage	V_{REG18}	(Note 1)	1.71	1.8	1.89	V
2.85V Regulator Initial Voltage	V_{REG285}	(Note 1)	2.8	2.85	2.9	V

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Frequencies	$f_{OSC-PERIPHERAL}$	T_A = +25°C (Note 5)		20		MHz
	$f_{MOSC-CORE}$	T_A = +25°C (Note 5)		10		
Clock Error	f_{ERR}	T_A = -40°C to +85°C			±5.5	%
External Clock Input	f_{XCLK}		20		133	MHz
Voltage Range: GP[15:0], SHEN, DACPW[7:0], REFINA, REFINB		(Note 1)	-0.3		V_{DD} + 0.3	V
Output Logic-Low: SCL, SDA, MDIO, MDI, MCL, MCS, REFINA, REFINB, All GPIO Pins	V_{OL1}	I_{OL} = 4mA (Note 1)			0.4	V
Output Logic-High: SDA, MDIO, MDI, MCL, MCS, REFINA, REFINB, All GPIO Pins Not Open Drain	V_{OH1}	I_{OH} = -4mA (Note 1)	V_{DD} - 0.5			V
Pullup Current: MDIO, MDI, MCL, MCS, All GPIO Pins	I_{PU1}	V_{PIN} = 0V	26	55	78	µA
GPIO Drive Strength, Extra Strong Outputs: GP0, GP1, MCS, PW8, PW9	R_{HISt}			9	27.6	Ω
	R_{LOSt}			8	25.2	
GPIO Drive Strength, Strong Outputs: MDI, DACPW3, DACPW6	R_{HIA}			17	32.4	Ω
	R_{LOA}			12	26.4	
GPIO Drive Strength, Excluding Strong GPIO Outputs	R_{HIB}			27	57	Ω
	R_{LOB}			31	63	

DAC DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC Resolution			12			Bits
DAC Internal Reference Accuracy		2.5V internal reference	-1.25		+1.25	%
DAC Internal Reference Power-Up Speed		99% settled		10		µs
Reference Input Full-Scale Range (REFINA, REFINB)			1		2.5	V
DAC Operating Current	I_{DACS}	Per channel	See the *DC Electrical Characteristics*			
DAC Integral Nonlinearity	DACINL	12-bit at 2.5V reference		12		LSB
DAC Differential Nonlinearity	DACDNL	12-bit at 2.5V reference			1	LSB
DAC Offset	$V_{OFFSET-DAC}$	At code “0”	0		18	mV
DAC Source Load Regulation	$I_{DAC-SOURCE}$	0 to full-scale output			8.6	mV/mA
DAC Sink Capability and Sink Load Regulation	$R_{DAC-SINK}$	0 to 0.5V output, limited by output buffer impedance		500		Ω
	$I_{DAC-SINK}$	0.5V to full-scale output			11.5	mV/mA
DAC Settling Time	t_{DAC}				10	µs

FAST COMPARATOR/QUICK TRIPS DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Fast Comparator Resolution			8			Bits
Fast Comparator Internal Reference Accuracy			-1		+1	%
Fast Comparator Operating Current	$I_{FASTCOMP}$		See the *DC Electrical Characteristics*			
Fast Comparator Full Scale	$V_{FS-COMP}$		2.36	2.42	2.48	V
Fast Comparator Integral Nonlinearity	INL	Differential mode, 2.2nF capacitor at input			2	LSB
Fast Comparator Differential Nonlinearity	DNL	Differential mode, 2.2nF capacitor at input			1	LSB
Fast Comparator Offset	$V_{OFFSET-COMP}$				2	LSB
Fast Comparator Input Resistance	$R_{IN-COMP}$	(Note 6)	15			MΩ
Fast Comparator Input Capacitance	$C_{IN-COMP}$			4		pF
Fast Comparator Sample Rate	f_{COMP}			625		ksps

ADC DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Resolution			13			Bits
ADC Internal Reference Accuracy			-0.85		+0.85	%
ADC Operating Current	I_{ADC}		See the *DC Electrical Characteristics*			
ADC Full-Scale 1	$V_{FS-ADC1}$			1.2		V
ADC Full-Scale 2	$V_{FS-ADC2}$			0.6		V
ADC Full-Scale 3	$V_{FS-ADC3}$			2.4		V
ADC Full-Scale 4	$V_{FS-ADC4}$			3.6		V
ADC Integral Nonlinearity	ADCINL	13-bit		10		LSB
ADC Differential Nonlinearity	ADCDNL		-8	+1	+8	LSB
ADC Sample-Sample Deviation		ADC full-scale set to $V_{FS-ADC3}$		5		LSB
ADC Offset	$V_{OFFSET-ADC}$	13-bit			2	LSB
GP[15:0] Input Resistance	R_{IN-ADC}		15			MΩ
ADC Sample Rate	f_{SAMPLE}	(Note 7)	8			ksps
ADC Temperature Conversion Time	t_{TEMP}			4.2		ms
Internal Temperature Measurement Error		(Note 8)	-3.2		+3.2	°C
Remote Temperature Measurement Error (DS4830 Error Only)		(Note 8)	-3.5		+3.5	°C

SAMPLE/HOLD DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Sample/Hold Input Range	V_{SHP}	ADC-SHN[1:0] = GND	0		1	V
Sample/Hold Capacitance	C_{SH}	ADC-SHP[1:0] to ADC-SHN[1:0]			5	pF
Sample Input Leakage	I_{SHLKG}	ADC-SHP[1:0] and ADC-SHN[1:0] connected to GND			1.2	µA
Sample Time	t_s	ADC-SHP[1:0] and ADC-SHN[1:0] connected to 50Ω voltage source	300			ns
Hold Time	t_h		250			µs
Sample Offset	V_{SH-OFF}	Measured at 10mV	-10	-1.6	+7	mV
Sample Error	ERR_{SH}	$V_{ADC-SHP\_}$ to $V_{ADC-SHN\_}$ = 5mV, t_s = 300ns, driven with 5kΩ voltage source	-3		+3	%
Sample Discharge Strength	R_{DIS}	ADC-SHP[1:0] or ADC-SHN[1:0] to GND		900	1500	Ω

FLASH MEMORY DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Flash Erase Time	t_{ME}	Mass erase	22	24	40	ms
	t_{PE}	Page erase	22	24	40	
Flash Programming Time per Word	t_{PROG}	(Note 9)	69	74	79	µs
Flash Programming Temperature			-40		+85	°C
Flash Endurance	n_{FLASH}	T_A = +50°C, guaranteed by design	20,000			Write Cycles
Data Retention		T_A = +50°C, guaranteed by design	100			Years

I²C-COMPATIBLE INTERFACE ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted.) (See Figure 1.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL/MSCL Clock Frequency	f_{SCL}	Timeout not enabled			400	kHz
SCL/MSCL Bootloader Clock Frequency	$f_{SCL:BOOT}$				100	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(Note 10)	0.6			µs
Low Period of SCL/MSCL Clock	t_{LOW}		1.3			µs
High Period of SCL/MSCL Clock	t_{HIGH}		0.6			µs
Setup Time for a (Repeated) START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	Receive	0			ns
		Transmit	300			
Data Setup Time	$t_{SU:DAT}$	(Notes 11, 12)	100			ns
SCL/MSCL, SDA/MSDA Capacitive Loading	C_B	(Note 13)			400	pF
Rise Time of Both SDA/MSDA and SCL/MSCL Signals	t_R	(Note 13)	20 + $0.1C_B$		300	ns
Fall Time of Both SDA/MSDA and SCL/MSCL Signals	t_F	(Note 13)	20 + $0.1C_B$		300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Width That Can Be Suppressed by Input Filter	t_{SP}	(Note 14)	0		50	ns
SCL/MSCL and SDA/MSDA Input Capacitance	C_{BIN}			5		pF
SMBusTimeout				30		ms

SPI DIGITAL INTERFACE SPECIFICATION (continued)

(V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted.) (See Figure 3 and Figure 4.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{SSPICS}$ Inactive	t_{SSH}		t_{SSPICK} + t_{SPI_RF}			ns
SSPICK Inactive to $\overline{SSPICS}$ Rising	t_{SD}		t_{SPI_RF}			ns
SSPIDO Output Disabled After $\overline{SSPICS}$ Edge Rise	t_{SLH}				$2t_{SSPICK}$ + $2t_{SPI\_RF}$	ns

ELECTRICAL CHARACTERISTICS: JTAG INTERFACE

(V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted.) (Figure 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
JTAG Logic Reference	V_{REF}			$V_{DD}/2$		V
TCK High Time	t_{TH}		0.5			µs
TCK Low Time	t_{TL}		0.5			µs
TCK Low to TDO Output	t_{TLQ}				0.125	µs
TMS, TDI Input Setup to TCK High	t_{DVTH}		0.25			µs
TMS, TDI Input Hold After TCK High	t_{THDX}		0.25			µs

Note 1: All voltages are referenced to GND. Currents entering the IC are specified as positive, and currents exiting the IC are specified as negative.
Note 2: Maximum current assuming 100% CPU duty cycle.
Note 3: This value does not include current in GPIO, SCL, SDA, MDIO, MDI, MCL, REFINA, and REFINB.
Note 4: Depends on voltage on REFINA/B using internal reference.
Note 5: There is one internal oscillator. The oscillator (peripheral clock) goes through a 2:1 divider to create the core clock.
Note 6: Guaranteed by design.
Note 7: ADC conversions are delayed up to 1.6µs if the fast comparator is sampling the selected ADC channel. This can cause a slight decrease in the ADC sampling rate.
Note 8: Temperature readings average 64 times.
Note 9: Programming time does not include overhead associated with the utility ROM interface.
Note 10: f_{SCL} must meet the minimum clock low time plus the rise/fall times.
Note 11: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.
Note 12: This device internally provides a hold time of at least 75ns for the SDA signal (referred to the $V_{IH:MIN}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 13: C_B—Total capacitance of one bus line in pF.
Note 14: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

Timing Diagrams (continued)

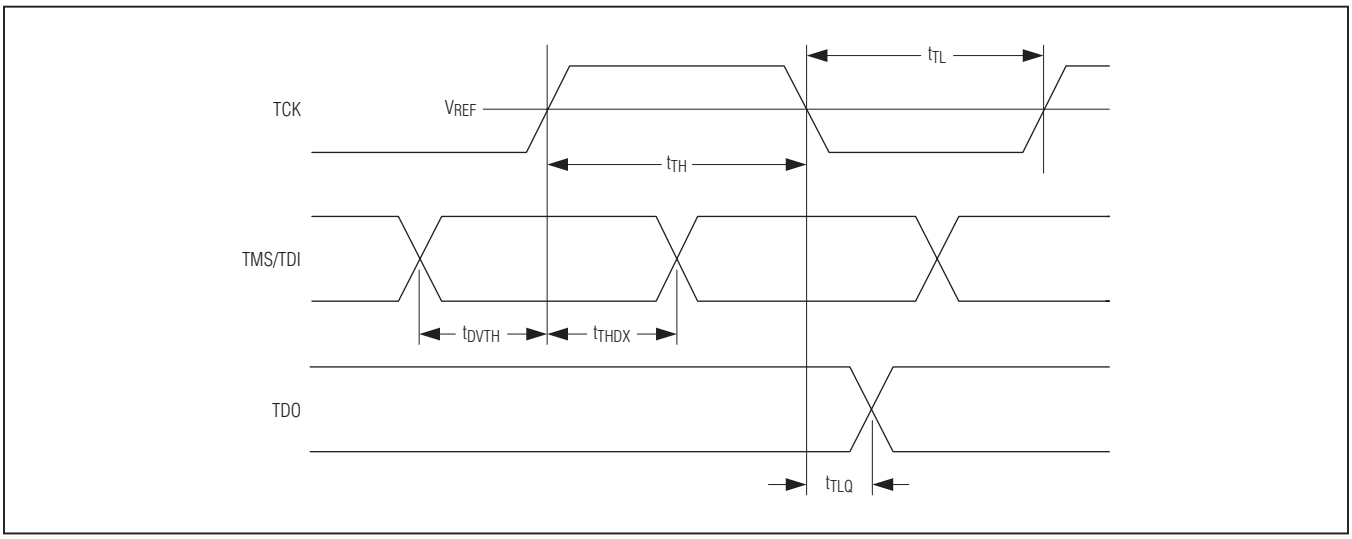
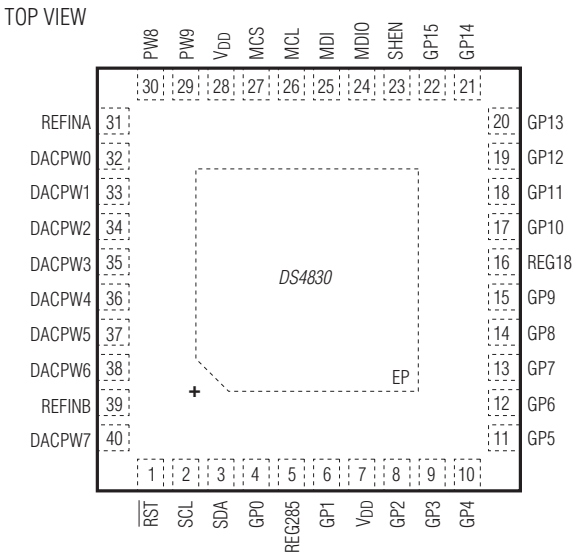


Figure 5. JTAG Timing Diagram

Pin Configuration



TQFN
(5mm x 5mm)

Pin Description

PIN	NAME	INPUT STRUCTURE(S)	OUTPUT STRUCTURE	POWER-ON STATE	SELECTABLE FUNCTIONS (FIRST COLUMN IS DEFAULT FUNCTION)				PORT
1	$\overline{RST}$	Digital	Open Drain	High Impedance	$\overline{RST}$	—	—	—	—
2	SCL	Digital	Open Drain	High Impedance	I^2C Slave Clock SCL	SPI SSPICK	—	—	—
3	SDA	Digital	Open Drain	High Impedance	I^2C Slave Data SDA	SPI SSPIDI	—	—	—
4	GP0	ADC/Digital Input	Push-Pull, Extra Strong	55µA Pullup	ADC-S0	ADC-D0P	PW0	—	P2.0
5	REG285	V_{REG}	None	2.85V	Only function is for bypass capacitor for 2.5V internal regulator				—
6	GP1	ADC/Digital Input	Push-Pull, Extra Strong	55µA Pullup	ADC-S1	ADC-D0N	PW1	—	P2.1
7	V_{DD}	Voltage Supply, ADC Input	None	V_{DD}	ADC-VDD	—	—	—	—
8	GP2	SH Input, ADC Input	None	High Impedance	ADC-S2	ADC-SHP0	ADC-D1P	—	—

Pin Description (continued)

PIN	NAME	INPUT STRUCTURE(S)	OUTPUT STRUCTURE	POWER-ON STATE	SELECTABLE FUNCTIONS (FIRST COLUMN IS DEFAULT FUNCTION)				PORT
9	GP3	SH input, ADC Input	None	High Impedance	ADC-S3	ADC-SHN0	ADC-D1N	—	—
10	GP4	ADC/Digital Input	Push-Pull	55µA Pullup	JTAG TCK	ADC-S4	ADC-D2P	—	P6.0
11	GP5	ADC/Digital Input	Push-Pull	55µA Pullup	JTAG TDI	ADC-S5	ADC-D2N	—	P6.1
12	GP6	ADC/Digital Input	Push-Pull	55µA Pullup	ADC-S6	ADC-D3P	PW2	SPI SSPIDO	P2.2
13	GP7	ADC/Digital Input	Push-Pull	55µA Pullup	ADC-S7	ADC-D3N	PW3	SPI $\overline{\text{SSPICS}}$	P2.3
14	GP8	ADC/Digital I/P, External Temp A+ I/P (ADC-TEXT_A)	Push-Pull	55µA Pullup	ADC-S8	ADC-D4P	—	—	P2.4
15	GP9	ADC/Digital I/P, External Temp A- I/P (ADC-TEXT_A)	Push-Pull	55µA Pullup	ADC-S9	ADC-D4N	—	—	P2.5
16	REG18	V_{REG}, ADC Input (ADC-1P8)	None	1.8V	Pin for 1.8V regulator bypass capacitor				—
17	GP10	ADC/Digital I/P, External Temp A+ I/P (ADC-TEXT_B)	Push-Pull	55µA Pullup	JTAG TMS	ADC-S10	ADC-D5P	—	P6.2
18	GP11	ADC/Digital I/P, External Temp A+ I/P (ADC-TEXT_B)	Push-Pull	55µA Pullup	JTAG TDO	ADC-S11	ADC-D5N	—	P6.3
19	GP12	SH Input, ADC/Digital Input	Push-Pull	55µA Pullup	ADC-S12	ADC-SHP1	ADC-D6P	—	P0.0
20	GP13	SH Input, ADC/Digital Input	Push-Pull	55µA Pullup	ADC-S13	ADC-SHN1	ADC-D6N	—	P0.1
21	GP14	ADC/Digital Input	Push-Pull	55µA Pullup	ADC-S14	ADC-D7P	SHEN1	—	P0.2
22	GP15	ADC/Digital Input	Push-Pull	55µA Pullup	ADC-S15	ADC-D7N	—	—	P0.3
23	SHEN	Digital	Push-Pull	55µA Pullup	SHEN0	—	—	—	P6.4
24	MDIO	Digital	Push-Pull	55µA Pullup	3-Wire Data MDIO	I^2C MSDA	SPI MSPIDO	PW4	P1.0
25	MDI	Digital	Push-Pull, Strong	55µA Pullup	—	—	SPI MSPIDI	PW5	P1.3
26	MCL	Digital	Push-Pull	55µA Pullup	3-Wire Clock MCL	I^2C MSCL	SPI MSPICK	PW6	P1.1

Pin Description (continued)

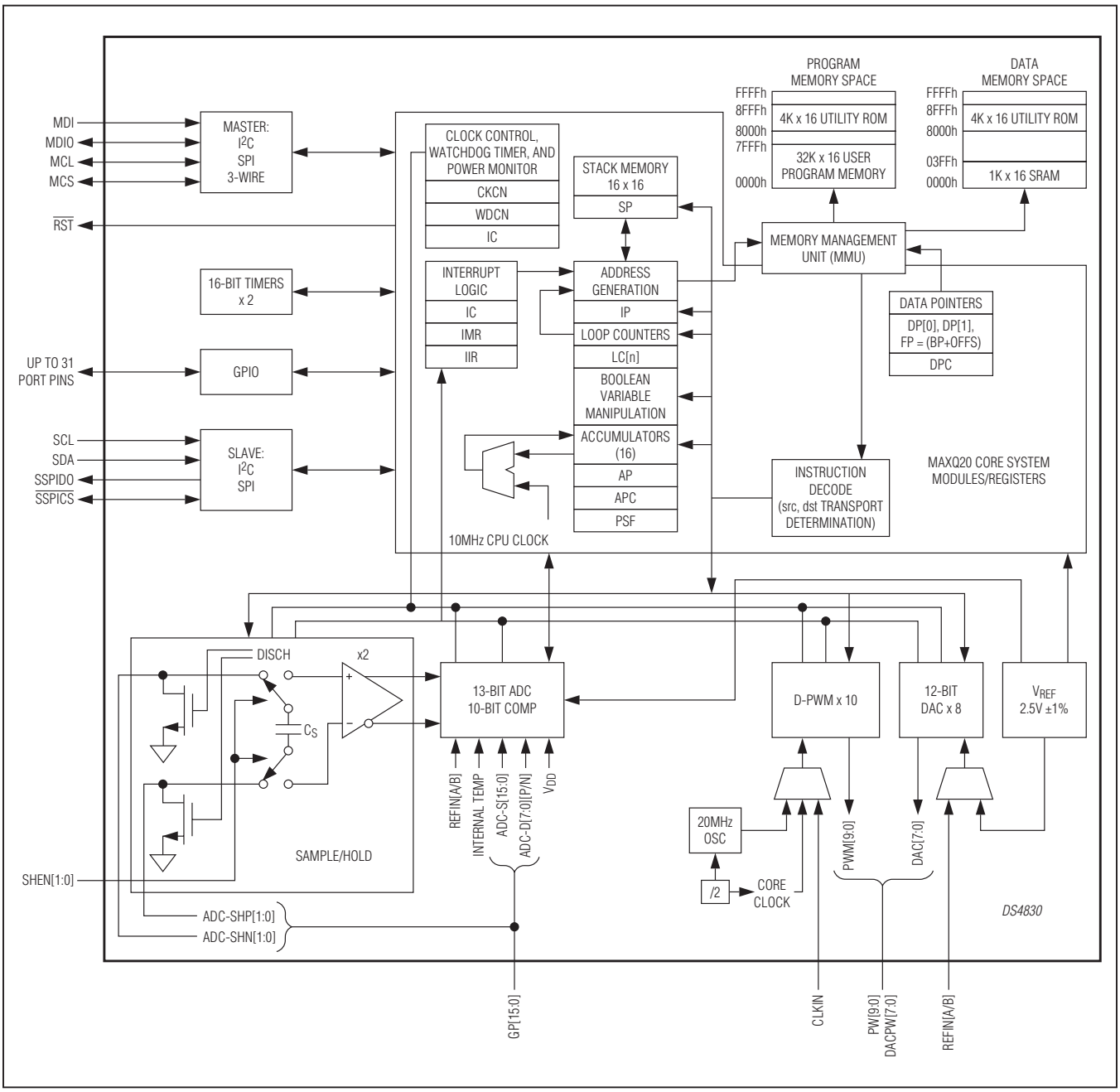
PIN	NAME	INPUT STRUCTURE(S)	OUTPUT STRUCTURE	POWER-ON STATE	SELECTABLE FUNCTIONS (FIRST COLUMN IS DEFAULT FUNCTION)				PORT
40	DACPW7	Digital	Push-Pull	55µA Pullup	DAC7, FS = REFINB or Internal Reference	PW7	—	—	P2.7
—	EP	Exposed Pad (Connect to GND)	—	GND	—	—	—	—	—

Note: *Bypass V_{DD}, REG285, and REG18 each with a 1µF X5R capacitor to ground. All input-only pins and open-drain outputs are high impedance after V_{DD} exceeds V_{BO} and prior to code execution. Pins configured as GPIO have a weak internal pullup. See the Selectable Functions table for more information.*

Selectable Functions

FUNCTION NAME	DESCRIPTION
ADC-1P8	1.8V Regulator Monitor Input to ADC
ADC-D[7:0][P/N]	Differential Inputs to ADC. Also used for external temperature sensors.
ADC-REFIN[A/B]	REFINA and REFINB Monitor Inputs to ADC
ADC-S[15:0]	Single-Ended Inputs to ADC
ADC-SH[P/N][1:0]	Sample/Hold Inputs 1 and 0
ADC-VDD	V_{DD} Monitor Input to ADC
DAC[7:0]	Voltage DAC Outputs
MCL, MCS, MDIO	Maxim Proprietary 3-Wire Interface, MCL (Clock), MCS (Chip Select), MDIO (Data). Used to control the MAX3798 family of high-speed laser drivers.
MSCL, MSDA	I²C Master Interface: MSCL (I²C Master Slave), MSDA (I²C Master Data)
MSPICK, $\overline{\text{MSPICS}}$, MSPIDI, MSPIDO	SPI Master Interface: MSPICK (Clock), $\overline{\text{MSPICS}}$ (Active-Low Chip Select), MSPIDI (Data In), MSPIDO (Data Out)
P0.n, P1.n, P2.n, P6.n	General-Purpose Inputs/Outputs. Can also function as interrupts.
PW[9:0]	PWM Outputs
$\overline{\text{RST}}$	Used by JTAG and as Active-Low Reset for Device
SCL, SDA	I²C Slave Interface: SCL (I²C Slave Clock), SDA (I²C Slave Data). These also function as a password-protected programming interface.
SHEN[1:0]	Sample/Hold Enable Inputs. Can also function as interrupts.
SSPICK, $\overline{\text{SSPICS}}$, SSPIDI, SSPIDO	SPI Slave Interface: SSPICK (Clock), $\overline{\text{SSPICS}}$ (Active-Low Chip Select), SSPIDI (Data In), SSPIDO (Data Out). In SPI slave mode, the I²C slave interface is disabled.
TCK, TDI, TDO, TMS	JTAG Interface Pins. Also includes $\overline{\text{RST}}$.

Block Diagram



Detailed Description

The following is an introduction to the primary features of the DS4830 system management microcontroller. More detailed descriptions of the device features can be found in the *DS4830 User's Guide*.

MAXQ20 Core Architecture

The device employs a MAXQ20 low-power, low-cost, high-performance, CMOS, fully static, 16-bit RISC microcontroller with flash memory. It is structured on a highly advanced, 16 accumulator-based, 16-bit RISC architecture. Fetch and execution operations are completed in one cycle without pipelining, since the instruction contains both the op code and data. The highly efficient core is supported by 16 accumulators and a 16-level hardware stack, enabling fast subroutine calling and task switching. Data can be quickly and efficiently manipulated with three internal data pointers. Multiple data pointers allow more than one function to access data memory without having to save and restore data pointers each time. The data pointers can automatically increment or decrement following an operation, eliminating the need for software intervention.

Module Information

The MAXQ20 architecture is designed to be modular and expandable. Top-level instruction decoding is extremely simple and based on transfers to and from registers. The registers are organized into functional modules, which are in turn divided into the system register and peripheral register groups.

Peripherals and other features are accessed through peripheral registers. These registers reside in modules 0 to 5. The following provides information about the specific module in which each peripheral resides:

- **Module 0:** Timer and Counter 1, GPIO Ports 0, 1, and 2
- **Module 1:** I²C Master, GPIO Port 6, SPI™ Slave, Flash Memory Controls
- **Module 2:** I²C Slave, Analog-to-Digital Converter (ADC), Sample/Hold, Temperature, 3-Wire Master
- **Module 3:** Timer and Counter 2, MAC-Related Registers
- **Module 4:** Digital-to-Analog Converter (DAC)
- **Module 5:** Quick Trips, SPI Master, PWM

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SPI is a trademark of Motorola, Inc.

Instruction Set

The instruction set is composed of fixed-length, 16-bit instructions that operate on registers and memory locations. The instruction set is highly orthogonal, allowing arithmetic and logical operations to use any register along with the accumulator. Special-function registers control the peripherals and are subdivided into register modules.

Memory Organization

The device incorporates several memory areas:

- 32KWords of flash memory for application program storage
- 1KWord of SRAM for storage of temporary variables
- 4KWords of utility ROM contain a debugger and program loader
- 16-level stack memory for storage of program return addresses and general-purpose use

The memory is implemented using the Harvard architecture, with separate address spaces for program memory, data memory, and register space. A pseudo-Von Neumann memory map is also used, placing ROM, application code, and data memory into a single contiguous memory map. The pseudo-Von Neumann memory map allows data memory to be mapped into program space, permitting code execution from data memory. In addition, program memory can be mapped into data space, permitting code constants to be accessed as data memory. Figure 6 shows the DS4830's memory map when executing from program memory space. Refer to the *DS4830 User's Guide* for memory map information when executing from data or ROM space.

The incorporation of flash memory allows field upgrade of the firmware. Flash memory can be password protected with a 16-word key, denying access to program memory by unauthorized individuals.

Utility ROM

The utility ROM is a 4KWord block of internal ROM memory that defaults to a starting address of 8000h. The utility ROM consists of subroutines that can be called from application software, which includes the following:

- In-system programming (bootstrap loader) over JTAG or I²C-compatible interfaces
- In-circuit debug routines

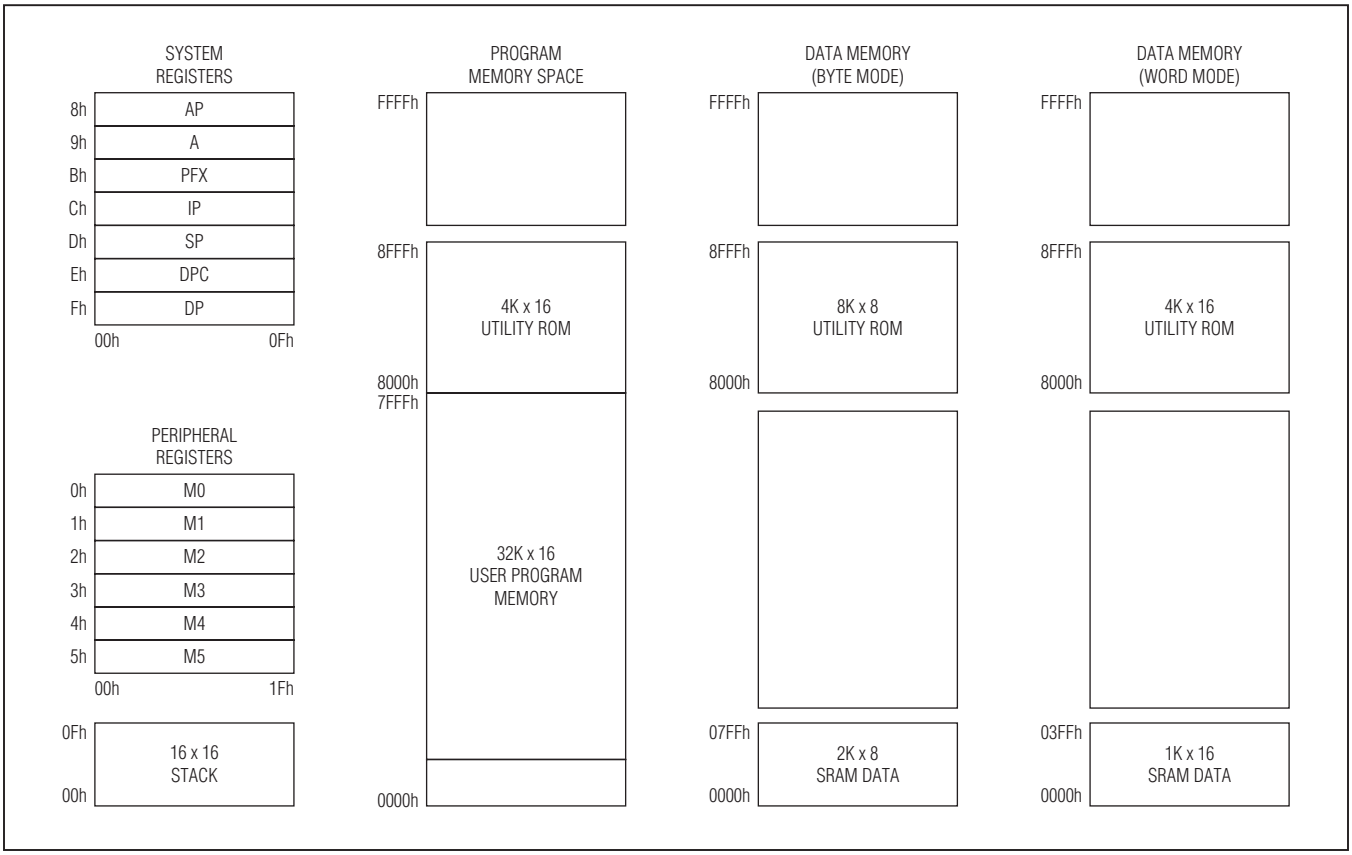

Figure 6. Memory Map

- Internal self-test routines
- Callable routines for in-application flash programming

Following any reset, execution begins in the utility ROM. The ROM software determines whether the program execution should immediately jump to location 0000h, the start of application code, or to one of the special routines mentioned. Routines within the utility ROM are firmware-accessible and can be called as subroutines by the application software. More information on the utility ROM contents is contained in the *DS4830 User's Guide*.

Password

Some applications require protection against unauthorized viewing of program code memory. For these applications, access to in-system programming, in-application programming, or in-circuit debugging functions is prohibited until a password has been supplied. The password is defined as the 16 words of physical program memory at addresses 0010h–001Fh.

A single password lock (PWL) bit is implemented in the device. When the PWL is set to 1 (power-on-reset default) and the contents of the memory at addresses 0010h–001Fh are any value other than all FFh or 00h, the password is required to access the utility ROM, including in-circuit debug and in-system programming routines that allow reading or writing of internal memory. When PWL is cleared to 0, these utilities are fully accessible without the password. The password is automatically set to all ones following a mass erase.

Detailed information regarding the password can be found in the *DS4830 User's Guide*.

Stack Memory

A 16-bit, 16-level internal stack provides storage for program return addresses and general-purpose use. The stack is used automatically by the processor when the CALL, RET, and RETI instructions are executed and interrupts serviced. The stack can also be used explicitly to store and retrieve data by using the PUSH, POP, and POPI instructions.

On reset, the stack pointer, SP, initializes to the top of the stack (0Fh). The CALL, PUSH, and interrupt-vectoring operations increment SP, then store a value at the location pointed to by SP. The RET, RETI, POP, and POPI operations retrieve the value at SP and then decrement SP.

Programming

The microcontroller's flash memory can be programmed by one of two methods: in-system programming or in-application programming. These provide great flexibility in system design as well as reduce the life-cycle cost of the embedded system. Programming can be password protected to prevent unauthorized access to code memory.

In-System Programming

An internal bootstrap loader allows the device to be programmed over the JTAG or I²C compatible interfaces. As a result, system software can be upgraded in-system, eliminating the need for a costly hardware retrofit when software updates are required.

The programming source select (PSS) bits in the ICDF register determine which interface is used for bootloading operation. The device supports JTAG and I²C as an interface corresponding to the 00 and 01 bits of PSS, respectively. See Figure 7.

In-Application Programming

The in-application programming feature allows the microcontroller to modify its own flash program memory. This allows on-the-fly software updates in mission-critical

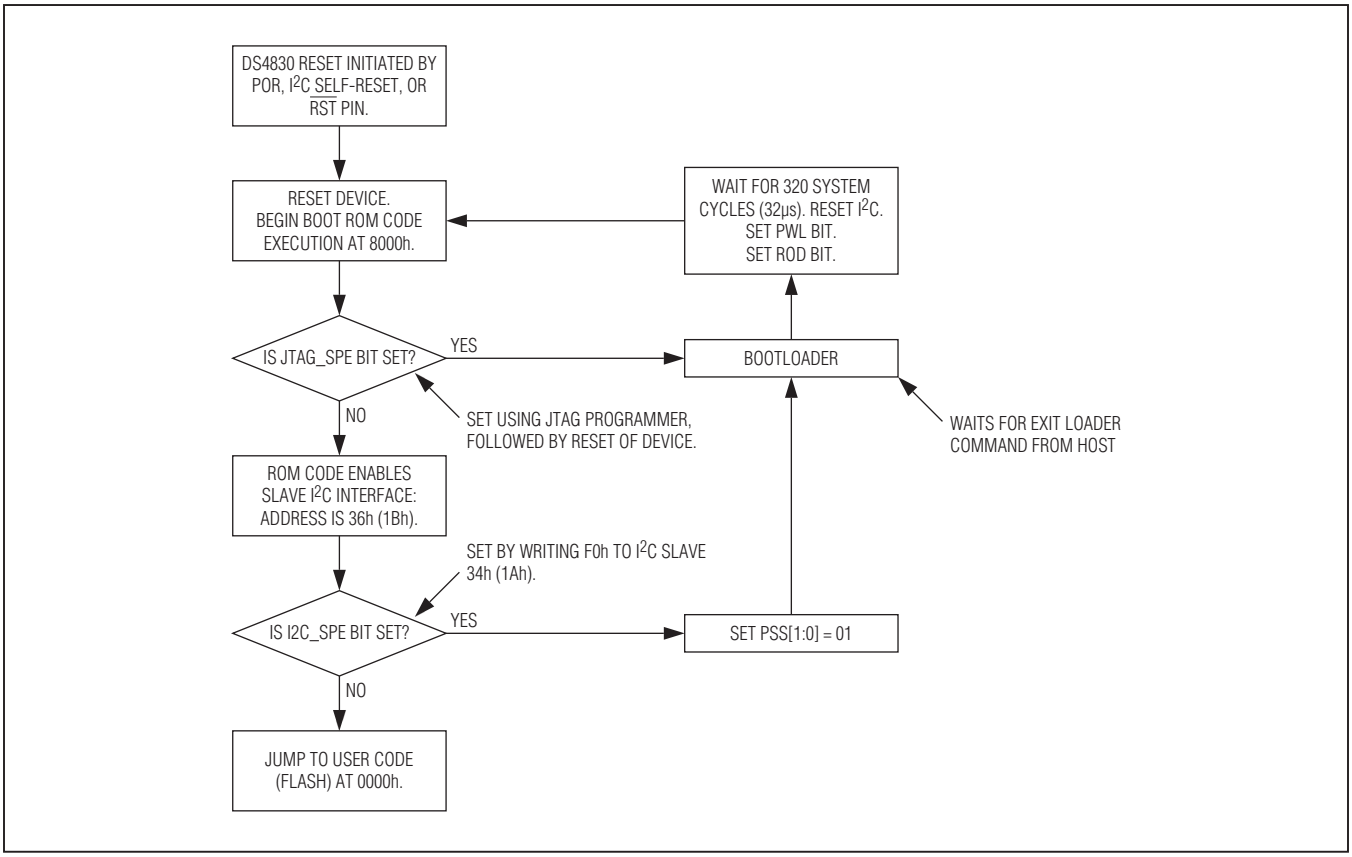

Figure 7. In-System Programming

applications that cannot afford downtime. Alternatively, it allows the application to develop custom loader software that can operate under the control of the application software. The utility ROM contains firmware-accessible flash programming functions that erase and program flash memory. These functions are described in detail in the *DS4830 User's Guide*.

Register Set

Sets of registers control most device functions. These registers provide a working space for memory operations as well as configuring and addressing peripheral registers on the device. Registers are divided into two major types: system registers (special-purpose registers, or SPRs) and peripheral registers (special-function registers, or SFRs). The common register set, also known as the system registers, includes the ALU, accumulator registers, data pointers, interrupt vectors and control, and stack pointer. The peripheral registers define additional functionality, and the functionality is broken up into discrete modules. Both the system registers and the peripheral registers are described in detail in the *DS4830 User's Guide*.

System Timing

The device generates its 10MHz instruction clock (MOSC) internally using a ring oscillator. On power-up, the oscillator's output (which cannot be accessed externally) is disabled until V_{DD} rises above V_{BO}. Once this threshold is reached, the output is enabled after approximately 1ms, clocking the device. See Figure 8.

System Reset

The device features several sources that can be used to reset the DS4830.

Power-On Reset

An internal power-on-reset (POR) circuit is used to enhance system reliability. This circuit forces the device to perform a POR whenever a rising voltage on V_{DD} climbs above V_{BO}. When this happens the following events occur:

- All registers and circuits enter their reset state.
- The POR flag (WDCN.7) is set to indicate the source of the reset.
- Code execution begins at location 8000h when the reset condition is released.

Brownout Detect/Reset

The device features a brownout detect/reset function. Whenever the power monitor detects a brownout condition (when $V_{DD} < V_{BO}$), it immediately issues a reset and stays in that state as long as V_{DD} remains below V_{BO}. Once V_{DD} voltage rises above V_{BO}, the device waits for $t_{SU:MOSC}$ before returning to normal operation, also referred to as CPU state. If a brownout occurs during $t_{SU:MOSC}$, the device again goes back to the brownout state. Otherwise, it enters into CPU state. In CPU state, the brownout detector is also enabled.

On power-up, the device always enters brownout state first and then follows the above sequence. The reset issued by brownout is the same as POR. Any action performed after POR also happens on brownout reset.

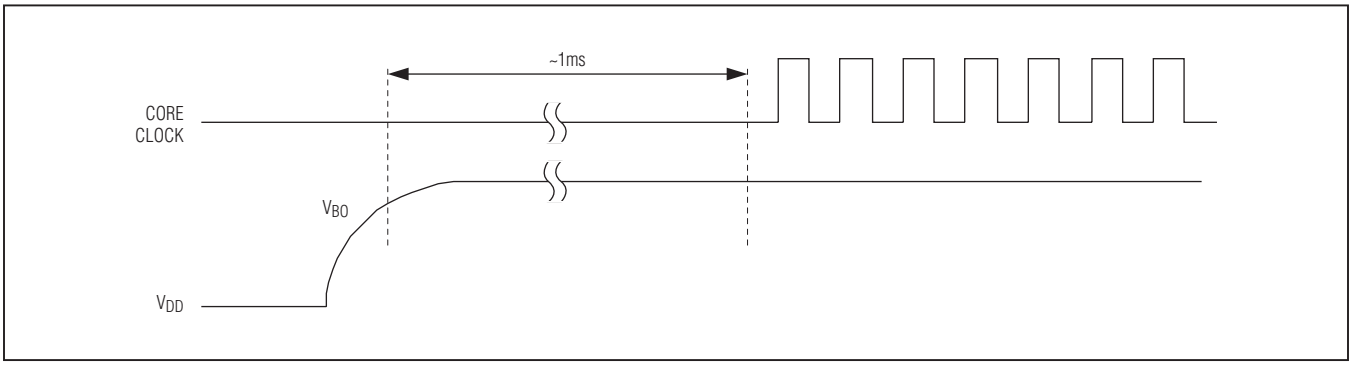

Figure 8. System Timing

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/11	Initial release	—
1	10/11	Corrected the lead temperature from +260°C to +300°C in the *Absolute Maximum Ratings* section; added explanation to the *DAC Outputs* section about the DAC operation in order to achieve desired INL levels	2, 22