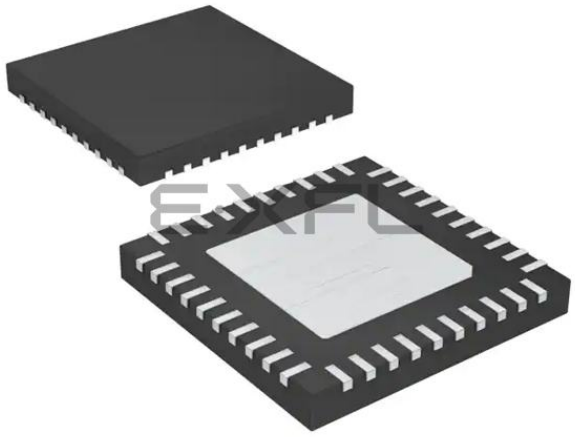

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	MAXQ20
Core Size	16-Bit
Speed	10MHz
Connectivity	3-Wire, I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	2.97V ~ 3.63V
Data Converters	A/D 18x13b; D/A 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-TQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds4830t

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND.....-0.3V to +3.63V
SCL, SDA, $\overline{RST}$.....-0.3V to +3.63V
All Other Pins to GND
except REG18 and REG285 .....-0.3V to (V_{DD} + 0.3V)*
Continuous Sink Current .....20mA per pin, 50mA total
Continuous Source Current.....20mA per pin, 50mA total
Operating Temperature Range.....-40°C to +85°C
Storage Temperature Range.....-55°C to +125°C
Lead Temperature (soldering, 10s) .....…+300°C
Soldering Temperature (reflow) .....…+260°C

**Subject to not exceeding +3.63V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Operating Voltage	V_{DD}	(Note 1)	3.0		3.6	V
Input Logic-High	V_{IH}		0.7 x V_{DD}		V_{DD} + 0.3	V
Input Logic-Low	V_{IL}		-0.3		0.3 x V_{DD}	V
Input Logic-High: SCL, SDA, MCL, MSDA	V_{I2C_IH}	(Note 1)	2.1		V_{DD} + 0.3	V
Input Logic-Low: SCL, SDA, MCL, MSDA	V_{I2C_IL}	(Note 1)	-0.5		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CPU}	CPU mode, all analog disabled (Notes 2, 3)		4.8		mA
	$I_{FASTCOMP}$			2		
	$I_{SAMPLEHOLDS}$	Both sample/hold		1.5		
	I_{ADC}			2.8		
	I_{DACS}	Per channel (Note 4)		0.6		
Brownout Voltage	V_{BO}	Monitors V_{DD} (Note 1)		2.7		V
Brownout Hysteresis	V_{BOH}	Monitors V_{DD} (Note 1)		0.07		V
1.8V Regulator Initial Voltage	V_{REG18}	(Note 1)	1.71	1.8	1.89	V
2.85V Regulator Initial Voltage	V_{REG285}	(Note 1)	2.8	2.85	2.9	V

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Frequencies	$f_{OSC-PERIPHERAL}$	T_A = +25°C (Note 5)		20		MHz
	$f_{MOSC-CORE}$	T_A = +25°C (Note 5)		10		
Clock Error	f_{ERR}	T_A = -40°C to +85°C			±5.5	%
External Clock Input	f_{XCLK}		20		133	MHz
Voltage Range: GP[15:0], SHEN, DACPW[7:0], REFINA, REFINB		(Note 1)	-0.3		V_{DD} + 0.3	V
Output Logic-Low: SCL, SDA, MDIO, MDI, MCL, MCS, REFINA, REFINB, All GPIO Pins	V_{OL1}	I_{OL} = 4mA (Note 1)			0.4	V
Output Logic-High: SDA, MDIO, MDI, MCL, MCS, REFINA, REFINB, All GPIO Pins Not Open Drain	V_{OH1}	I_{OH} = -4mA (Note 1)	V_{DD} - 0.5			V
Pullup Current: MDIO, MDI, MCL, MCS, All GPIO Pins	I_{PU1}	V_{PIN} = 0V	26	55	78	µA
GPIO Drive Strength, Extra Strong Outputs: GP0, GP1, MCS, PW8, PW9	R_{HISt}			9	27.6	Ω
	R_{LOSt}			8	25.2	
GPIO Drive Strength, Strong Outputs: MDI, DACPW3, DACPW6	R_{HIA}			17	32.4	Ω
	R_{LOA}			12	26.4	
GPIO Drive Strength, Excluding Strong GPIO Outputs	R_{HIB}			27	57	Ω
	R_{LOB}			31	63	

ADC DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Resolution			13			Bits
ADC Internal Reference Accuracy			-0.85		+0.85	%
ADC Operating Current	I_{ADC}		See the *DC Electrical Characteristics*			
ADC Full-Scale 1	$V_{FS-ADC1}$			1.2		V
ADC Full-Scale 2	$V_{FS-ADC2}$			0.6		V
ADC Full-Scale 3	$V_{FS-ADC3}$			2.4		V
ADC Full-Scale 4	$V_{FS-ADC4}$			3.6		V
ADC Integral Nonlinearity	ADCINL	13-bit		10		LSB
ADC Differential Nonlinearity	ADCDNL		-8	+1	+8	LSB
ADC Sample-Sample Deviation		ADC full-scale set to $V_{FS-ADC3}$		5		LSB
ADC Offset	$V_{OFFSET-ADC}$	13-bit			2	LSB
GP[15:0] Input Resistance	R_{IN-ADC}		15			MΩ
ADC Sample Rate	f_{SAMPLE}	(Note 7)	8			ksps
ADC Temperature Conversion Time	t_{TEMP}			4.2		ms
Internal Temperature Measurement Error		(Note 8)	-3.2		+3.2	°C
Remote Temperature Measurement Error (DS4830 Error Only)		(Note 8)	-3.5		+3.5	°C

SAMPLE/HOLD DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Sample/Hold Input Range	V_{SHP}	ADC-SHN[1:0] = GND	0		1	V
Sample/Hold Capacitance	C_{SH}	ADC-SHP[1:0] to ADC-SHN[1:0]			5	pF
Sample Input Leakage	I_{SHLKG}	ADC-SHP[1:0] and ADC-SHN[1:0] connected to GND			1.2	µA
Sample Time	t_s	ADC-SHP[1:0] and ADC-SHN[1:0] connected to 50Ω voltage source	300			ns
Hold Time	t_h		250			µs
Sample Offset	V_{SH-OFF}	Measured at 10mV	-10	-1.6	+7	mV
Sample Error	ERR_{SH}	$V_{ADC-SHP\_}$ to $V_{ADC-SHN\_}$ = 5mV, t_s = 300ns, driven with 5kΩ voltage source	-3		+3	%
Sample Discharge Strength	R_{DIS}	ADC-SHP[1:0] or ADC-SHN[1:0] to GND		900	1500	Ω

3-WIRE DIGITAL INTERFACE SPECIFICATION

(V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted.) (See Figure 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MCL Clock Frequency	f_{SCLOUT}			833		kHz
MCL Duty Cycle	t_{3WDC}			50		%
MDIO Setup Time	t_{DS}		100			ns
MDIO Hold Time	t_{DH}		100			ns
MCS Pulse-Width Low	t_{CSW}		500			ns
MCS Leading Time Before the First MCL Edge	t_L		500			ns
MCS Trailing Time After the Last MCL Edge	t_T		500			ns
MDIO, MCL Load	C_{B3W}	Total bus capacitance on one line			10	pF

SPI DIGITAL INTERFACE SPECIFICATION

(V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted.) (See Figure 3 and Figure 4.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI Master Operating Frequency	$1/t_{MSPICK}$				$f_{SYS}/2$	MHz
SPI Slave Operating Frequency	$1/t_{SSPICK}$				$f_{SYS}/4$	MHz
SPI I/O Rise/Fall Time	t_{SPI_RF}	C_L = 15pF, pullup = 560Ω			25	ns
MSPICK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$t_{MSPICK}/2$ - t_{SPI_RF}			ns
MSPIDO Output Hold After MSPICK Sample Edge	t_{MOH}		$t_{MSPICK}/2$ - t_{SPI_RF}			ns
MSPIDO Output Valid to MSPICK Sample Edge (MSPIDO Setup)	t_{MOV}		$t_{MSPICK}/2$ - t_{SPI_RF}			ns
MSPIDI Input Valid to MSPICK Sample Edge (MSPIDI Setup)	t_{MIS}		$2t_{SPI\_RF}$			ns
MSPIDI Input to MSPICK Sample Edge Rise/Fall Hold	t_{MIH}		0			ns
MSPICK Inactive to MSPIDO Inactive	t_{MLH}		$t_{MSPICK}/2$ - t_{SPI_RF}			ns
SSPICK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCL}/2$		ns
$\overline{SSPICS}$ Active to First Shift Edge	t_{SSE}		t_{SPI_RF}			ns
SSPIDI Input to SSPICK Sample Edge Rise/Fall Setup	t_{SIS}		t_{SPI_RF}			ns
SSPIDI Input from SSPICK Sample Edge Transition Hold	t_{SIH}		t_{SPI_RF}			ns
SSPIDO Output Valid After SSPICK Shift Edge Transition	t_{SOV}				$2t_{SPI\_RF}$	ns

SPI DIGITAL INTERFACE SPECIFICATION (continued)

(V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted.) (See Figure 3 and Figure 4.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{SSPICS}$ Inactive	t_{SSH}		t_{SSPICK} + t_{SPI_RF}			ns
SSPICK Inactive to $\overline{SSPICS}$ Rising	t_{SD}		t_{SPI_RF}			ns
SSPIDO Output Disabled After $\overline{SSPICS}$ Edge Rise	t_{SLH}				$2t_{SSPICK}$ + $2t_{SPI\_RF}$	ns

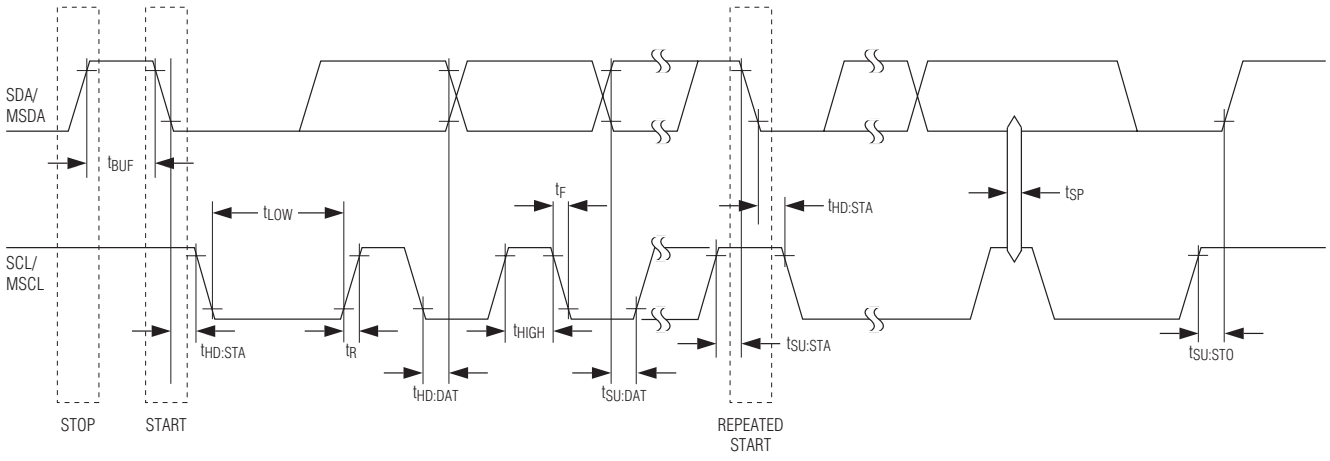
ELECTRICAL CHARACTERISTICS: JTAG INTERFACE

(V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted.) (Figure 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
JTAG Logic Reference	V_{REF}			$V_{DD}/2$		V
TCK High Time	t_{TH}		0.5			µs
TCK Low Time	t_{TL}		0.5			µs
TCK Low to TDO Output	t_{TLQ}				0.125	µs
TMS, TDI Input Setup to TCK High	t_{DVTH}		0.25			µs
TMS, TDI Input Hold After TCK High	t_{THDX}		0.25			µs

Note 1: All voltages are referenced to GND. Currents entering the IC are specified as positive, and currents exiting the IC are specified as negative.
Note 2: Maximum current assuming 100% CPU duty cycle.
Note 3: This value does not include current in GPIO, SCL, SDA, MDIO, MDI, MCL, REFINA, and REFINB.
Note 4: Depends on voltage on REFINA/B using internal reference.
Note 5: There is one internal oscillator. The oscillator (peripheral clock) goes through a 2:1 divider to create the core clock.
Note 6: Guaranteed by design.
Note 7: ADC conversions are delayed up to 1.6µs if the fast comparator is sampling the selected ADC channel. This can cause a slight decrease in the ADC sampling rate.
Note 8: Temperature readings average 64 times.
Note 9: Programming time does not include overhead associated with the utility ROM interface.
Note 10: f_{SCL} must meet the minimum clock low time plus the rise/fall times.
Note 11: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.
Note 12: This device internally provides a hold time of at least 75ns for the SDA signal (referred to the $V_{IH:MIN}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 13: C_B—Total capacitance of one bus line in pF.
Note 14: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

Timing Diagrams



NOTE: TIMING IS REFERENCED TO V_{ILMAX} AND V_{IHMIN}.

Figure 1. I²C Timing Diagram

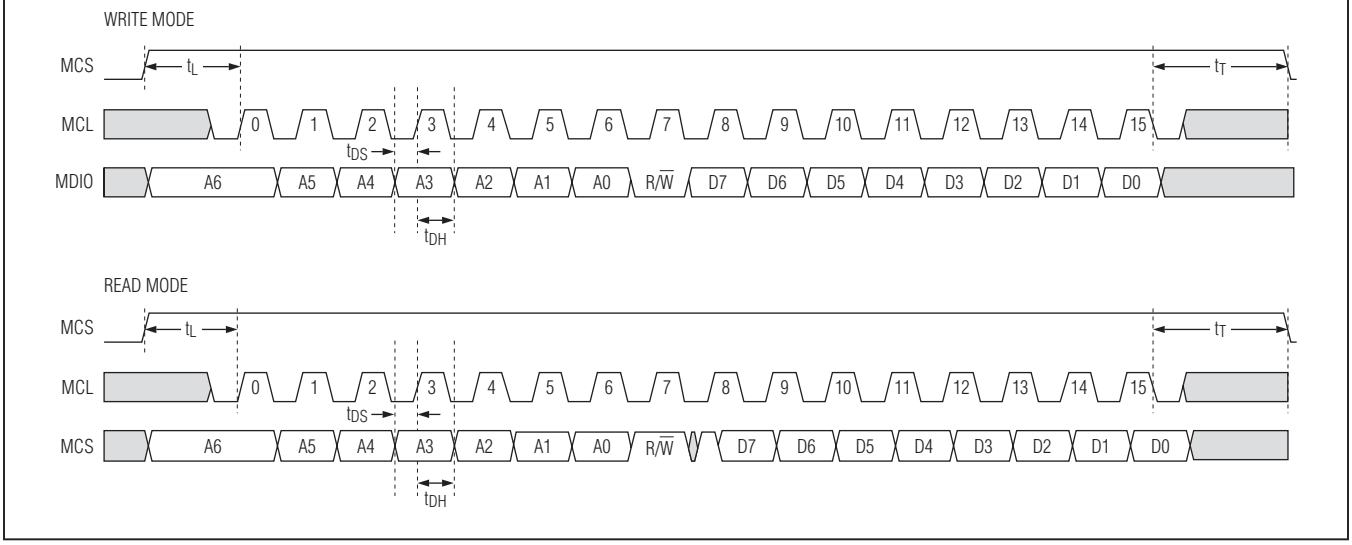


Figure 2. 3-Wire Timing Diagram

Timing Diagrams (continued)

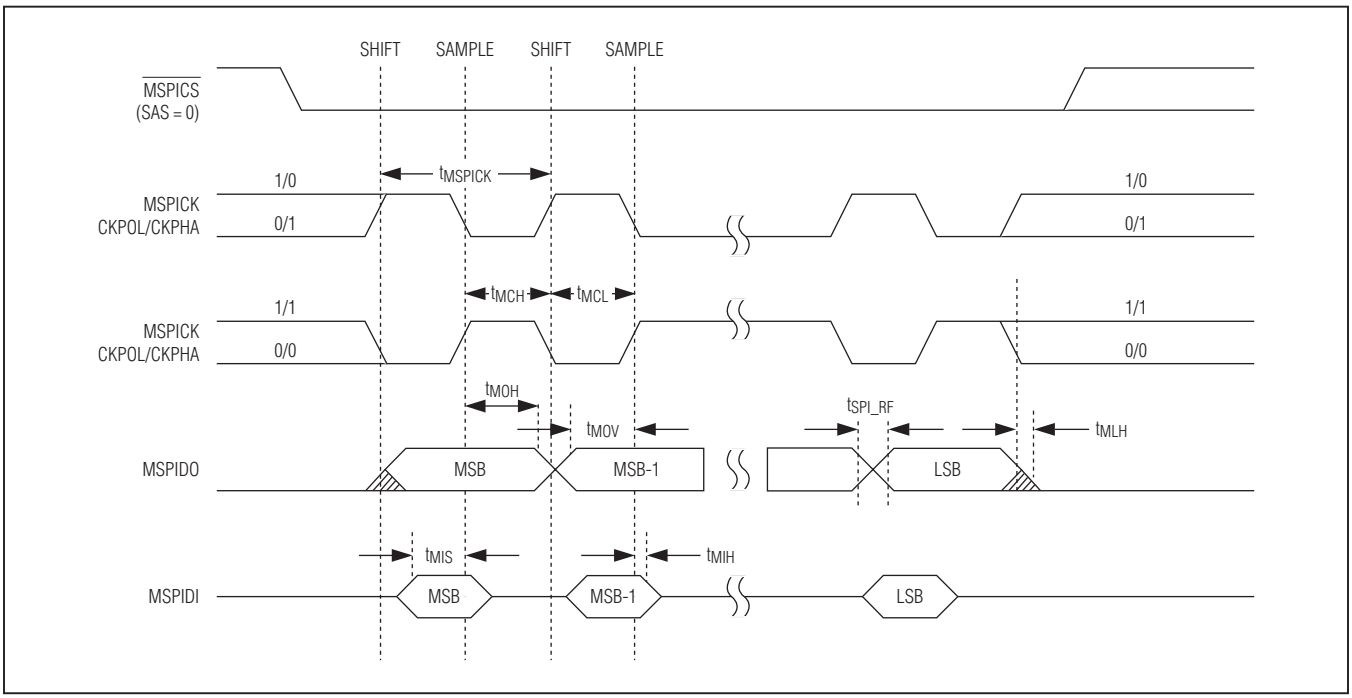


Figure 3. SPI Master Communications Timing Diagram

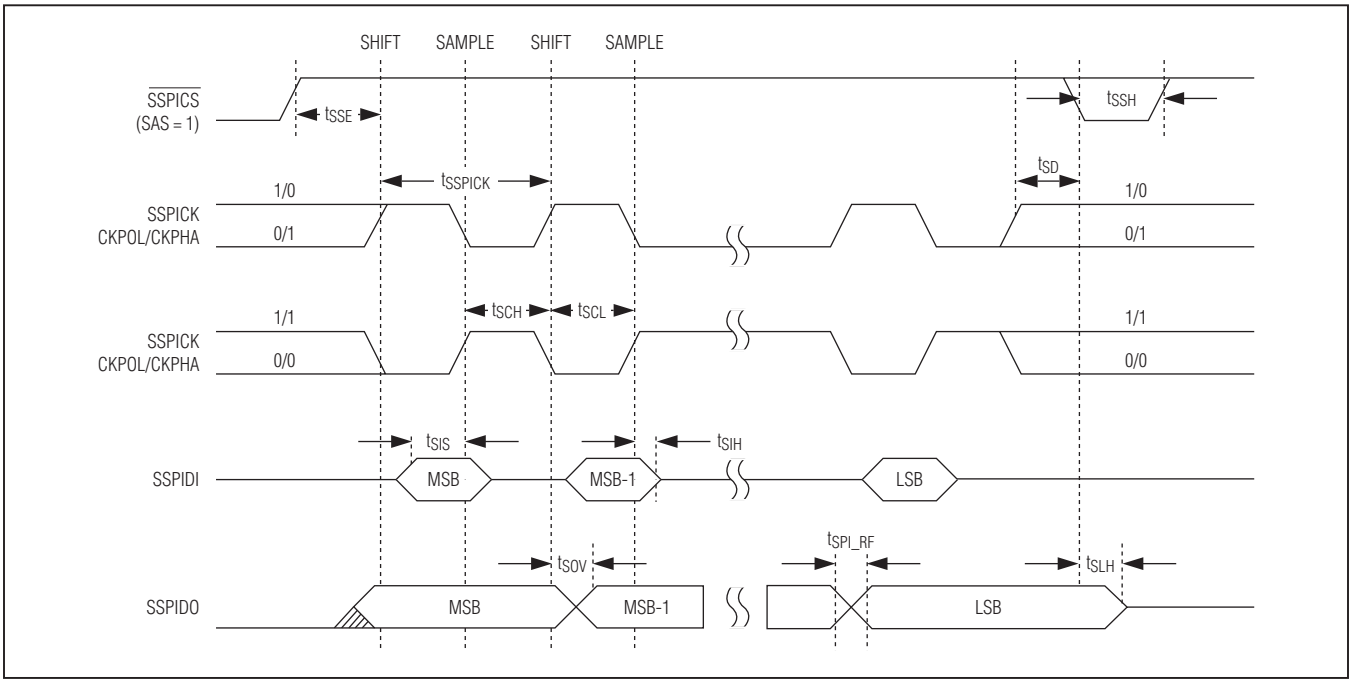


Figure 4. SPI Slave Communications Timing Diagram

Timing Diagrams (continued)

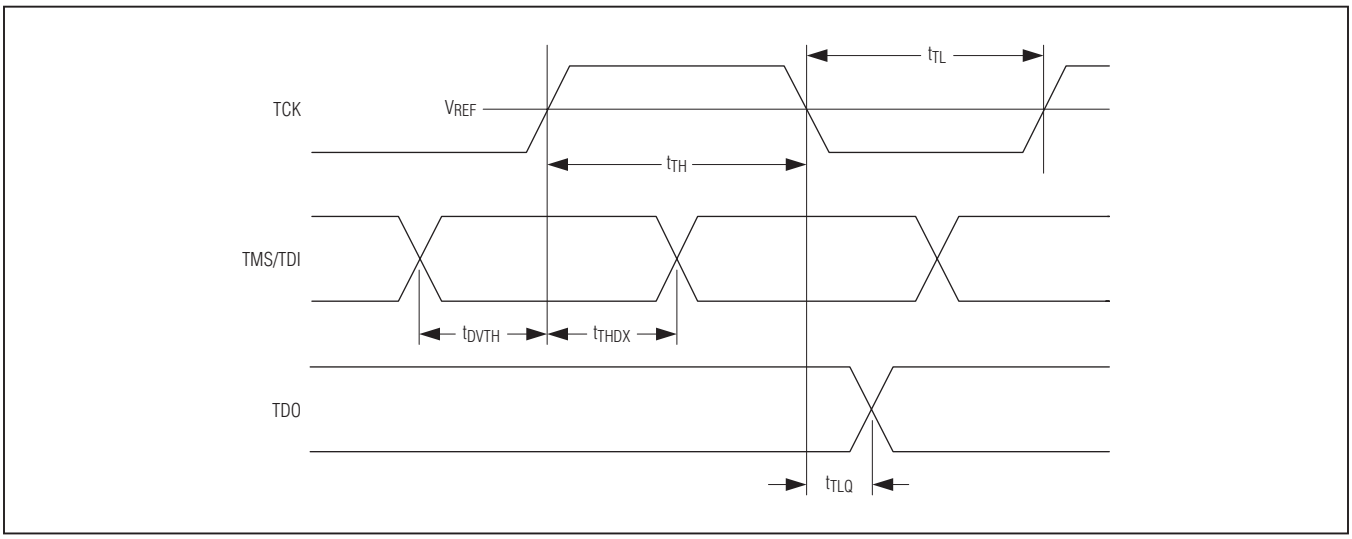


Figure 5. JTAG Timing Diagram

Pin Description (continued)

PIN	NAME	INPUT STRUCTURE(S)	OUTPUT STRUCTURE	POWER-ON STATE	SELECTABLE FUNCTIONS (FIRST COLUMN IS DEFAULT FUNCTION)				PORT
9	GP3	SH input, ADC Input	None	High Impedance	ADC-S3	ADC-SHN0	ADC-D1N	—	—
10	GP4	ADC/Digital Input	Push-Pull	55µA Pullup	JTAG TCK	ADC-S4	ADC-D2P	—	P6.0
11	GP5	ADC/Digital Input	Push-Pull	55µA Pullup	JTAG TDI	ADC-S5	ADC-D2N	—	P6.1
12	GP6	ADC/Digital Input	Push-Pull	55µA Pullup	ADC-S6	ADC-D3P	PW2	SPI SSPIDO	P2.2
13	GP7	ADC/Digital Input	Push-Pull	55µA Pullup	ADC-S7	ADC-D3N	PW3	SPI $\overline{\text{SSPICS}}$	P2.3
14	GP8	ADC/Digital I/P, External Temp A+ I/P (ADC-TEXT_A)	Push-Pull	55µA Pullup	ADC-S8	ADC-D4P	—	—	P2.4
15	GP9	ADC/Digital I/P, External Temp A- I/P (ADC-TEXT_A)	Push-Pull	55µA Pullup	ADC-S9	ADC-D4N	—	—	P2.5
16	REG18	V_{REG}, ADC Input (ADC-1P8)	None	1.8V	Pin for 1.8V regulator bypass capacitor				—
17	GP10	ADC/Digital I/P, External Temp A+ I/P (ADC-TEXT_B)	Push-Pull	55µA Pullup	JTAG TMS	ADC-S10	ADC-D5P	—	P6.2
18	GP11	ADC/Digital I/P, External Temp A+ I/P (ADC-TEXT_B)	Push-Pull	55µA Pullup	JTAG TDO	ADC-S11	ADC-D5N	—	P6.3
19	GP12	SH Input, ADC/Digital Input	Push-Pull	55µA Pullup	ADC-S12	ADC-SHP1	ADC-D6P	—	P0.0
20	GP13	SH Input, ADC/Digital Input	Push-Pull	55µA Pullup	ADC-S13	ADC-SHN1	ADC-D6N	—	P0.1
21	GP14	ADC/Digital Input	Push-Pull	55µA Pullup	ADC-S14	ADC-D7P	SHEN1	—	P0.2
22	GP15	ADC/Digital Input	Push-Pull	55µA Pullup	ADC-S15	ADC-D7N	—	—	P0.3
23	SHEN	Digital	Push-Pull	55µA Pullup	SHEN0	—	—	—	P6.4
24	MDIO	Digital	Push-Pull	55µA Pullup	3-Wire Data MDIO	I^2C MSDA	SPI MSPIDO	PW4	P1.0
25	MDI	Digital	Push-Pull, Strong	55µA Pullup	—	—	SPI MSPIDI	PW5	P1.3
26	MCL	Digital	Push-Pull	55µA Pullup	3-Wire Clock MCL	I^2C MSCL	SPI MSPICK	PW6	P1.1

Pin Description (continued)

PIN	NAME	INPUT STRUCTURE(S)	OUTPUT STRUCTURE	POWER-ON STATE	SELECTABLE FUNCTIONS (FIRST COLUMN IS DEFAULT FUNCTION)				PORT
27	MCS	Digital	Push-Pull, Extra Strong	55µA Pullup	3-Wire Chip Select MCS	—	SPI $\overline{\text{MSPICS}}$	PW7	P1.2
28	V_{DD}	Voltage Supply	None	V_{DD}	ADC-VDD	—	—	—	—
29	PW9	Digital	Push-Pull, Extra Strong	55µA Pullup	PW9	—	—	—	P0.7
30	PW8	Digital	Push-Pull, Extra Strong	55µA Pullup	PW8	—	—	—	P0.6
31	REFINA	Reference, ADC/Digital Input (ADC_REFA)	Push-Pull	55µA Pullup	ADC-REFINA	—	—	—	P2.6
32	DACPW0	Digital	Push-Pull	55µA Pullup	DAC0, FS = REFINA or Internal Reference	PW0	—	—	P0.4
33	DACPW1	Digital	Push-Pull	55µA Pullup	DAC1, FS = REFINA or Internal Reference	PW1	—	—	P0.5
34	DACPW2	Digital	Push-Pull	55µA Pullup	DAC2, FS = REFINA or Internal Reference	PW2	CLKIN	—	P6.5
35	DACPW3	Digital	Push-Pull, Strong	55µA Pullup	DAC3, FS = REFINA or Internal Reference	PW3	—	—	P1.5
36	DACPW4	Digital	Push-Pull	55µA Pullup	DAC4, FS = REFINB or Internal Reference	PW4	—	—	P1.6
37	DACPW5	Digital	Push-Pull	55µA Pullup	DAC5, FS = REFINB or Internal Reference	PW5	—	—	P1.7
38	DACPW6	Digital	Push-Pull, Strong	55µA Pullup	DAC6, FS = REFINB or Internal Reference	PW6	—	—	P6.6
39	REFINB	Reference, ADC/ Digital Input	Push-Pull	55µA Pullup	ADC-REFINB	—	—	—	P1.4

Pin Description (continued)

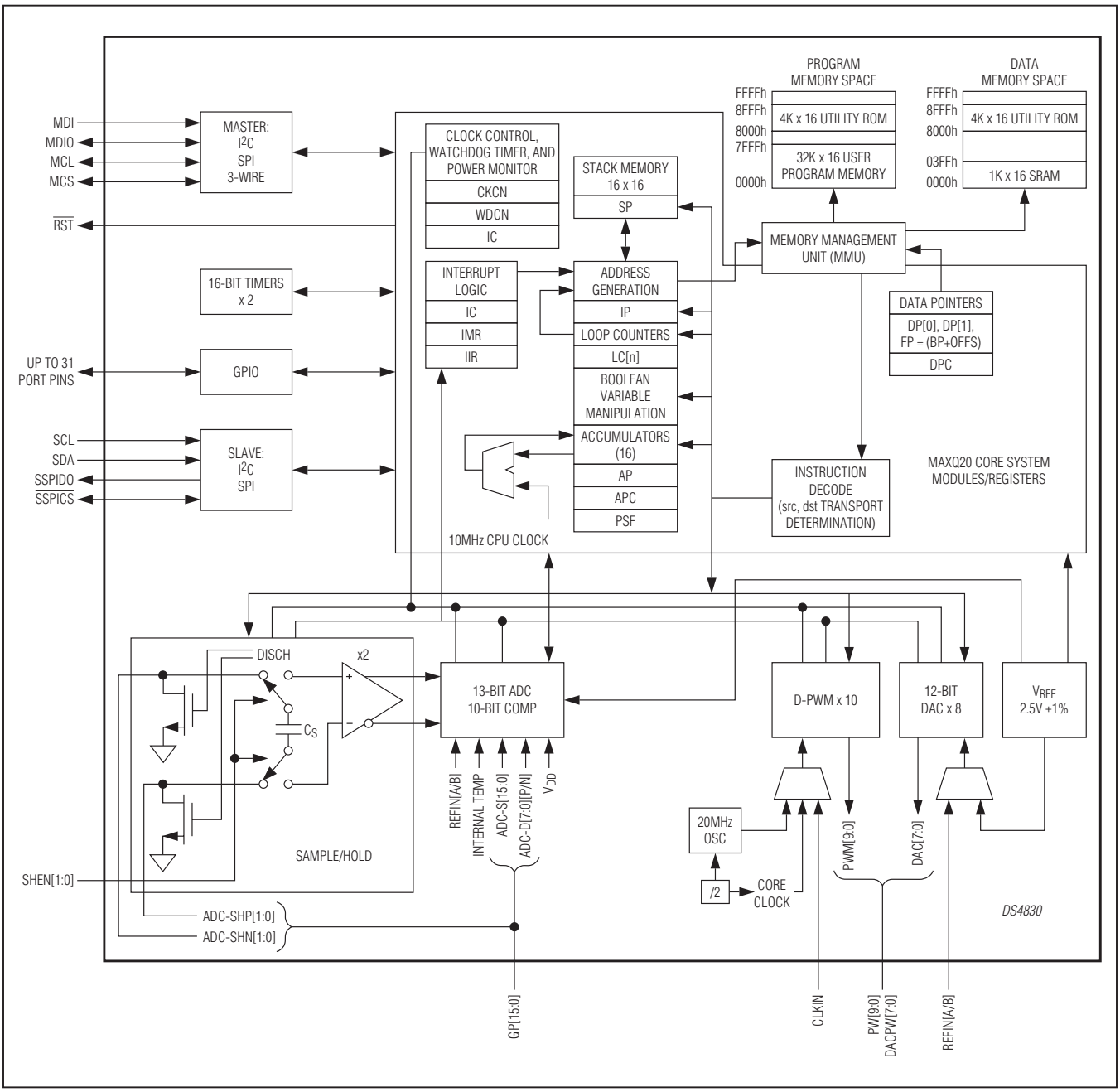
PIN	NAME	INPUT STRUCTURE(S)	OUTPUT STRUCTURE	POWER-ON STATE	SELECTABLE FUNCTIONS (FIRST COLUMN IS DEFAULT FUNCTION)				PORT
40	DACPW7	Digital	Push-Pull	55µA Pullup	DAC7, FS = REFINB or Internal Reference	PW7	—	—	P2.7
—	EP	Exposed Pad (Connect to GND)	—	GND	—	—	—	—	—

Note: *Bypass V_{DD}, REG285, and REG18 each with a 1µF X5R capacitor to ground. All input-only pins and open-drain outputs are high impedance after V_{DD} exceeds V_{BO} and prior to code execution. Pins configured as GPIO have a weak internal pullup. See the Selectable Functions table for more information.*

Selectable Functions

FUNCTION NAME	DESCRIPTION
ADC-1P8	1.8V Regulator Monitor Input to ADC
ADC-D[7:0][P/N]	Differential Inputs to ADC. Also used for external temperature sensors.
ADC-REFIN[A/B]	REFINA and REFINB Monitor Inputs to ADC
ADC-S[15:0]	Single-Ended Inputs to ADC
ADC-SH[P/N][1:0]	Sample/Hold Inputs 1 and 0
ADC-VDD	V_{DD} Monitor Input to ADC
DAC[7:0]	Voltage DAC Outputs
MCL, MCS, MDIO	Maxim Proprietary 3-Wire Interface, MCL (Clock), MCS (Chip Select), MDIO (Data). Used to control the MAX3798 family of high-speed laser drivers.
MSCL, MSDA	I²C Master Interface: MSCL (I²C Master Slave), MSDA (I²C Master Data)
MSPICK, $\overline{\text{MSPICS}}$, MSPIDI, MSPIDO	SPI Master Interface: MSPICK (Clock), $\overline{\text{MSPICS}}$ (Active-Low Chip Select), MSPIDI (Data In), MSPIDO (Data Out)
P0.n, P1.n, P2.n, P6.n	General-Purpose Inputs/Outputs. Can also function as interrupts.
PW[9:0]	PWM Outputs
$\overline{\text{RST}}$	Used by JTAG and as Active-Low Reset for Device
SCL, SDA	I²C Slave Interface: SCL (I²C Slave Clock), SDA (I²C Slave Data). These also function as a password-protected programming interface.
SHEN[1:0]	Sample/Hold Enable Inputs. Can also function as interrupts.
SSPICK, $\overline{\text{SSPICS}}$, SSPIDI, SSPIDO	SPI Slave Interface: SSPICK (Clock), $\overline{\text{SSPICS}}$ (Active-Low Chip Select), SSPIDI (Data In), SSPIDO (Data Out). In SPI slave mode, the I²C slave interface is disabled.
TCK, TDI, TDO, TMS	JTAG Interface Pins. Also includes $\overline{\text{RST}}$.

Block Diagram



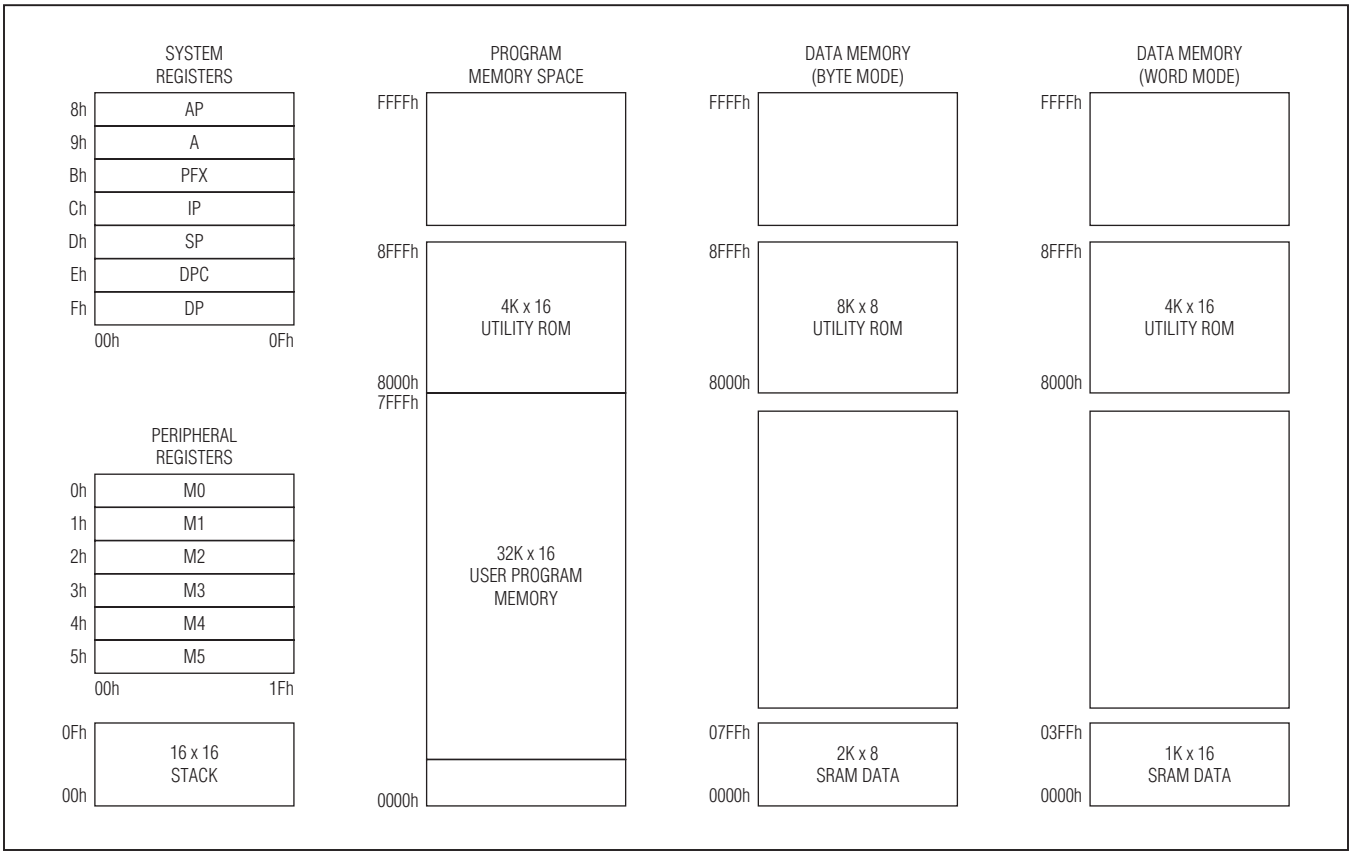


Figure 6. Memory Map

- Internal self-test routines
- Callable routines for in-application flash programming

Following any reset, execution begins in the utility ROM. The ROM software determines whether the program execution should immediately jump to location 0000h, the start of application code, or to one of the special routines mentioned. Routines within the utility ROM are firmware-accessible and can be called as subroutines by the application software. More information on the utility ROM contents is contained in the *DS4830 User's Guide*.

Password

Some applications require protection against unauthorized viewing of program code memory. For these applications, access to in-system programming, in-application programming, or in-circuit debugging functions is prohibited until a password has been supplied. The password is defined as the 16 words of physical program memory at addresses 0010h–001Fh.

A single password lock (PWL) bit is implemented in the device. When the PWL is set to 1 (power-on-reset default) and the contents of the memory at addresses 0010h–001Fh are any value other than all FFh or 00h, the password is required to access the utility ROM, including in-circuit debug and in-system programming routines that allow reading or writing of internal memory. When PWL is cleared to 0, these utilities are fully accessible without the password. The password is automatically set to all ones following a mass erase.

Detailed information regarding the password can be found in the *DS4830 User's Guide*.

applications that cannot afford downtime. Alternatively, it allows the application to develop custom loader software that can operate under the control of the application software. The utility ROM contains firmware-accessible flash programming functions that erase and program flash memory. These functions are described in detail in the *DS4830 User's Guide*.

Register Set

Sets of registers control most device functions. These registers provide a working space for memory operations as well as configuring and addressing peripheral registers on the device. Registers are divided into two major types: system registers (special-purpose registers, or SPRs) and peripheral registers (special-function registers, or SFRs). The common register set, also known as the system registers, includes the ALU, accumulator registers, data pointers, interrupt vectors and control, and stack pointer. The peripheral registers define additional functionality, and the functionality is broken up into discrete modules. Both the system registers and the peripheral registers are described in detail in the *DS4830 User's Guide*.

System Timing

The device generates its 10MHz instruction clock (MOSC) internally using a ring oscillator. On power-up, the oscillator's output (which cannot be accessed externally) is disabled until V_{DD} rises above V_{BO}. Once this threshold is reached, the output is enabled after approximately 1ms, clocking the device. See Figure 8.

System Reset

The device features several sources that can be used to reset the DS4830.

Power-On Reset

An internal power-on-reset (POR) circuit is used to enhance system reliability. This circuit forces the device to perform a POR whenever a rising voltage on V_{DD} climbs above V_{BO}. When this happens the following events occur:

- All registers and circuits enter their reset state.
- The POR flag (WDCN.7) is set to indicate the source of the reset.
- Code execution begins at location 8000h when the reset condition is released.

Brownout Detect/Reset

The device features a brownout detect/reset function. Whenever the power monitor detects a brownout condition (when $V_{DD} < V_{BO}$), it immediately issues a reset and stays in that state as long as V_{DD} remains below V_{BO}. Once V_{DD} voltage rises above V_{BO}, the device waits for $t_{SU:MOSC}$ before returning to normal operation, also referred to as CPU state. If a brownout occurs during $t_{SU:MOSC}$, the device again goes back to the brownout state. Otherwise, it enters into CPU state. In CPU state, the brownout detector is also enabled.

On power-up, the device always enters brownout state first and then follows the above sequence. The reset issued by brownout is the same as POR. Any action performed after POR also happens on brownout reset.

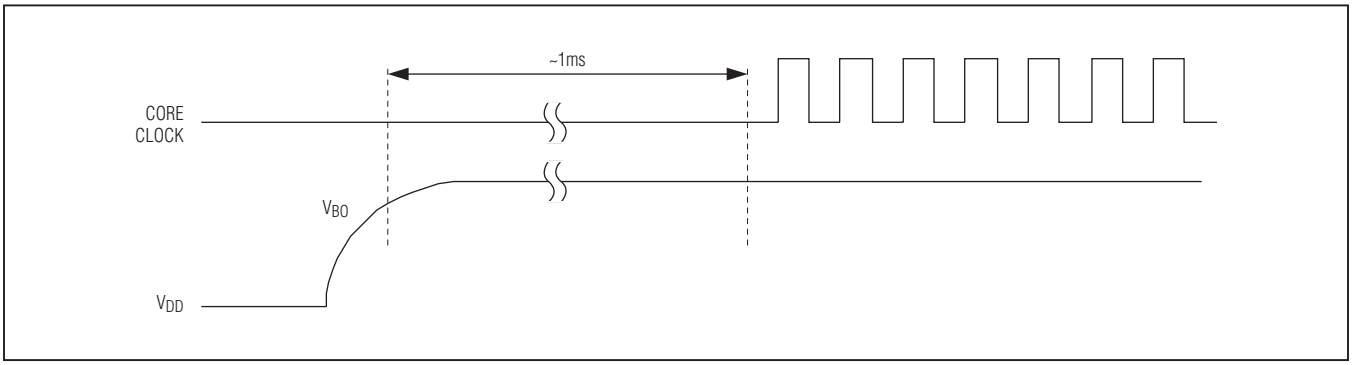


Figure 8. System Timing

All the registers that are cleared on POR are also cleared on brownout reset.

Watchdog Timer Reset

The watchdog timer provides a mechanism to reset the processor in the case of undesirable code execution. The watchdog timer is a hardware timer designed to be periodically reset by the application software. If the software operates correctly, the timer is reset before it reaches its maximum count. However, if undesirable code execution prevents a reset of the watchdog timer, the timer reaches its maximum count and resets the processor.

The watchdog timer is controlled through two bits in the WDCN register (WDCN[5:4]: WD[1:0]). Its timeout period can be set to one of the four programmable intervals ranging from 2^{12} to 2^{21} system clock (MOSC) periods (0.409ms to 0.210s). The watchdog interrupt occurs at the end of this timeout period, which is 512 MOSC clock periods, or approximately 50µs, before the reset. The reset generated by the watchdog timer lasts for four system clock cycles, which is 0.4µs. Software can determine if a reset is caused by a watchdog timeout by checking the watchdog timer reset flag (WTRF) in the WDCN register. Execution resumes at location 8000h following a watchdog timer reset.

External Reset

Asserting $\overline{RST}$ low causes the device to enter the reset state. The external reset function is described in the *DS4830 User's Guide*. Execution resumes at location 8000h after $\overline{RST}$ is released. The DAC and PWM outputs are unchanged during execution of external reset.

Internal System Reset

The host can issue an I²C command (BBh) to reset the communicating device. This reset has the same effect as the external reset as far as the reset values of all registers are concerned. Also, an internal system reset can occur when the in-system programming is done (ROD = 1).

Further details are available in the *DS4830 User's Guide*.

Programmable Timer/Counter

The device features two general-purpose programmable timer/counters. Various timing loops can be implemented using the timers. Each general-purpose timer/counter uses three SFRs. GTCN is the general control register, GTV is the timer value register, and GTC is the timer compare register.

The timer can be used in two modes: free-running mode and compare mode with interrupts. Both are described in detail in the *DS4830 User's Guide*.

The functionality of the timers can be accessed through three SFRs for each of the general-purpose timers. The timer and counter SFRs are accessed in module 0 and module 3. Detailed information regarding the timer/counter block can be found in theDS4830 *User's Guide*.

Hardware Multiplier

The hardware multiplier (multiply-accumulate, or MAC module) is a very powerful tool, especially for applications that require heavy calculations. This multiplier can execute the multiply or multiply-negate, or multiply-accumulate or multiply-subtract operation for signed or unsigned operands in a single machine cycle. The MAC module uses eight SFRs, mapped as register 0h–05h and 08h–09h in module M3.

System Interrupts

Multiple interrupt sources are available to respond to internal and external events. The MAXQ20 architecture uses a single interrupt vector (IV) and single interrupt-service routine (ISR) design. For maximum flexibility, interrupts can be enabled globally, individually, or by module. When an interrupt condition occurs, its individual flag is set, even if the interrupt source is disabled at the local, module, or global level. Interrupt flags must be cleared within the firmware-interrupt routine to avoid repeated interrupts from the same source. Application software must ensure a delay between the write to the flag and the RETI instruction to allow time for the interrupt hardware to remove the internal interrupt condition. Asynchronous interrupt flags require a one-instruction delay and synchronous interrupt flags require a two-instruction delay.

When an enabled interrupt is detected, execution jumps to a user-programmable interrupt vector location. The IV register defaults to 0000h on reset or power-up, so if it is not changed to a different address, application firmware must determine whether a jump to 0000h came from a $\overline{RST}$ or interrupt source.

Once control has been transferred to the ISR, the interrupt identification register (IIR) can be used to determine if a system register or peripheral register was the source of the interrupt. In addition to IIR, MIIR registers

are implemented to indicate which particular function under a peripheral module has caused the interrupt. The device contains six peripheral modules, M0 to M5. An MIIR register is implemented in modules M0, M1, and M2. The MIIRs are 16-bit read-only registers and all of them default to all zeros on system reset. Once the module that causes the interrupt is singled out, it can then be interrogated for the specific interrupt source and software can take appropriate action. Interrupts are evaluated by application code allowing the definition of a unique interrupt priority scheme for each application. Interrupt sources are available from the watchdog timer, the ADC (including sample/holds), fast comparators, the programmable timer/counter, the I^2C-compatible master and slave interface, 3-wire, master and slave SPI, and all GPIO pins.

I/O Port

The device allows for most inputs and outputs to function as general-purpose input and/or output pins. There are four ports: P0, P1, P2, and P6. Note that there is no port corresponding to P6.7. The 7th bit of port 6 is nonfunctional in all SFRs. Each pin is multiplexed with at least one special function, such as interrupts, timer/counter I/O pins, or JTAG pins, etc.

The GPIO pins have Schmitt trigger receivers and full CMOS output drivers and can support alternate functions. The ports can be accessed through SFRs (PO[0,1,2,6], PI[0,1,2,6], PD[0,1,2,6], EIE[0,1,2,6], EIF[0,1,2,6], and EIES[0,1,2,6]) in modules 0 and 1, and each pin can be individually configured. The pin is either high impedance or a weak pullup when defined as an input, dependent on the state of the corresponding bit in the output register. In addition, each pin can function as external interrupt with individual enable, flag and active edge selection, when programmed as input.

The I/O port SFRs are accessed in module 0 and 1. Detailed information regarding the GPIO block can be found in the *DS4830 User's Guide*.

DAC Outputs

The device provides eight 12-bit DAC outputs with multiple reference options. An internal 2.5V reference is provided. There are also two selectable external references. REFINA can be selected as the full-scale reference for DAC0 to DAC3. REFINB can be selected as the full-scale reference for DAC4 to DAC7. The DAC outputs are voltage buffered. Each DAC can be individually disabled and put into a low-power power-down mode using DACCFG. An external reset does not affect the DAC outputs.

If a DAC output is used during the lifetime of the DS4830, the DAC must always be enabled to guarantee meeting the INL and offset specifications. If a pin is used for a DAC, it should be used only for the DAC function. The pin's function should not be switched between DAC and PWM or switched between DAC and GPIO.

The DAC SFRs are accessed in module 4. Detailed information regarding the DAC block can be found in the *DS4830 User's Guide*.

PWM Outputs

The device provides 10 independently configurable PWM outputs. The PWM outputs are configured using three SFRs: PWMCN, PWMDATA, and PWNSYNC. Using PWMCN and PWMDATA, individual PWM channels can be programmed for unique duty cycles (DCYCn), configurations (PWMCFGn), and delays (PWMDLYn), where n represents the PWM channel number.

The PWM clock can be obtained from the core clock, peripheral clock, or an external clock, depending on CLK_SEL bits programmed in individual PWMCFGn registers. The PWMCFGn register also enables/disables the corresponding PWM output and selects the PWM polarity. The user can set the duty cycle and the frequency of each PWM output individually by configuring the corresponding DCYCn register and the PWMCFGn register.

The device allows 4-bit or 32-bit pulse spreading options for each PWM channel. The PWM outputs can be configured to be output on an alternate location using the configuration register. PWMDLY is a 12-bit register used for providing starting delay on different PWM channels, and can be used to create multiphase PWM operation.

Different channels can be synchronized using the PWMSYNC register. Doing so effectively brings the channels in phase by restarting the channels that are to be synchronized. An external reset does not affect the PWM outputs.

The PWM SFRs are accessed in module 5. Detailed information regarding the PWM block can be found in the *DS4830 User's Guide*.

Analog-to-Digital Converter and Sample/Hold

The analog-to-digital converter (ADC) controller is the digital interface block between the CPU and the ADC. It provides all the necessary controls to the ADC and the CPU interface. The ADC uses a set of SFRs for configuring the ADC in desired mode of operation.

The device contains a 13-bit ADC with an input mux (Figure 9). The mux selects the ADC input from 16 single-ended or eight differential inputs. Additionally, the channels can be configured to convert internal and external temperature, V_{DD}, internal reference, or REFINA/B. Two channels can be programmed to be sample/hold inputs. The internal channel is used exclusively to measure the die temperature. The SFR registers control the ADC.

ADC

When used in voltage input mode, the voltage applied on the corresponding channel (differential or single-ended) is converted to a digital readout. The ADC can be set up to continuously poll selected input channels (continuous-sequence mode) or run a short burst of conversions and enter a shutdown mode to conserve power (single-sequence mode).

In voltage mode there are four full-scale values that can be programmed. These values can be trimmed by modifying the associated gain registers (ADCG1, ADCG2, ADCG4, ADCG8). By default these are set to 1.2V, 0.6V, 2.4V, and 4.8V full scale.

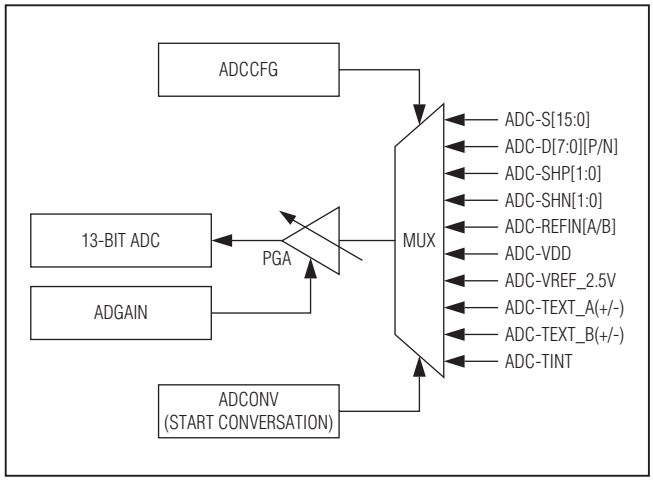


Figure 9. ADC Block Diagram

The ADCCLK is derived from the system clock with division ratio defined by the ADC control register. An A/D conversion takes 15 ADCCLK cycles to complete with additional four core clocks used for data processing. Internally every channel is converted twice and the average of two conversions is written to the data buffer. This gives each conversion result in (30 x ADC Clock Period + 800ns). ADC sampling rate is approximately 40ksps for the fastest ADC clock (core clock/8). In applications where extending the acquisition time is desired, the sample can be acquired over a prolonged period determined by the ADC control register.

Each ADC channel can have its own configuration, such as differential mode select, data alignment select, acquisition extension enable, ADC reference select and external temperature mode select, etc. The ADC also has 20 (0 to 19) 16-bit data buffers for conversion result storage. The ADC data available interrupt flag (ADDAI) can be configured to trigger an interrupt following a predetermined number of samples. Once set, ADDAI can be cleared by software or at the start of a conversion process.

Sample/Hold

Pin combinations A2-A3 and A12-A13 can be used for sample/hold conversions if enabled in the SHCN register. These two can be independently enabled or disabled by writing a 1 or 0 to their corresponding bit locations in SHCN register. A data buffer location is reserved for each channel. When a particular channel is enabled, a sample of the input voltage is taken when a signal is issued on the SHEN pin, converted and stored in the corresponding data buffer.

The two sample/hold channels can sample simultaneously on the same SHEN signal or different SHEN signals depending on the SH_DUAL bit in the SHCN SFR.

The sample/hold data available interrupt flag (SHnDAI) can be configured to trigger an interrupt following sample completion. Once set, SHnDAI can be cleared by software.

Each sample/hold circuit consists of a sampling capacitor, charge injection nulling switches, and a buffer. Also included is a discharge circuit used to discharge parasitic capacitance on the input node and the sample capacitor before sampling begins. The negative input pins can be used to reduce ground offsets and noise.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS4830T+	-40°C to +85°C	40 TQFN-EP*

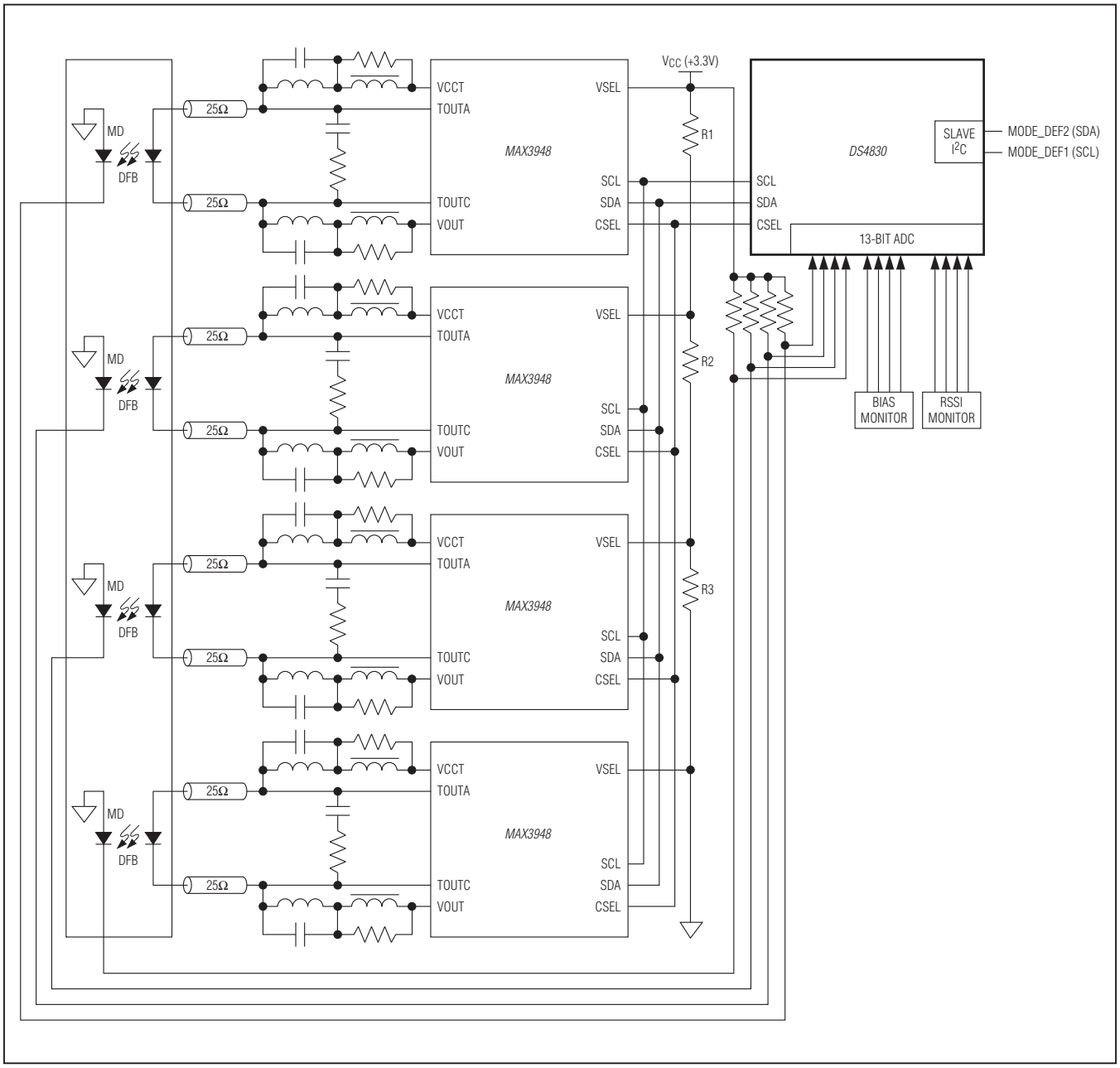
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
40 TQFN-EP	T4055+2	21-0140	90-0002

Typical Application Circuit



Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/11	Initial release	—
1	10/11	Corrected the lead temperature from +260°C to +300°C in the *Absolute Maximum Ratings* section; added explanation to the *DAC Outputs* section about the DAC operation in order to achieve desired INL levels	2, 22