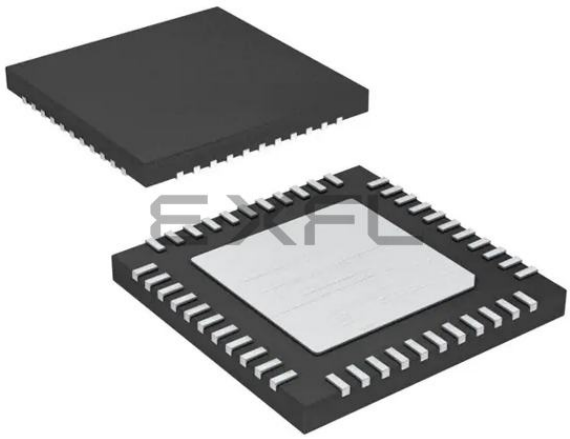

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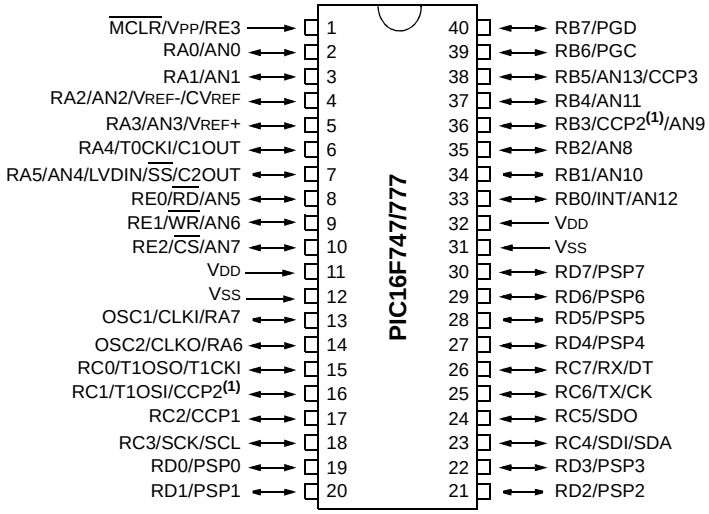
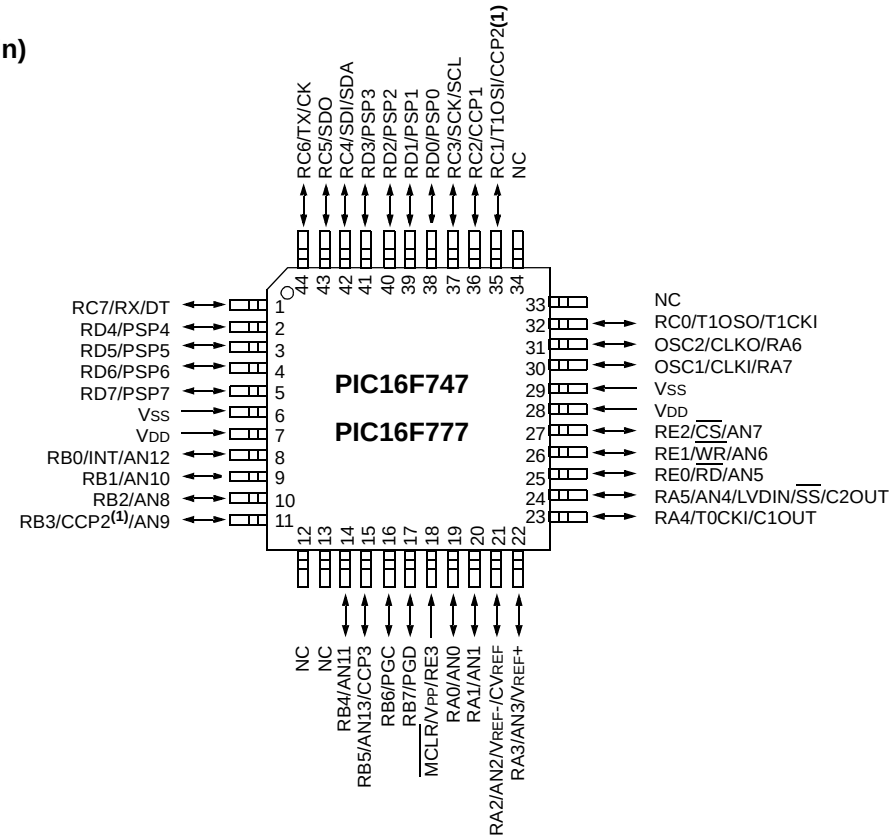
Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f747t-i-ml

Pin Diagrams (Continued)

PDIP (40-pin)



TQFP (44-pin)



Note 1: Pin location of CCP2 is determined by the CCPMX bit in Configuration Word Register 1.

TABLE 1-2: PIC16F737 AND PIC16F767 PINOUT DESCRIPTION

Pin Name	PDIP SOIC SSOP Pin #	QFN Pin #	I/O/P Type	Buffer Type	Description
OSC1/CLKI/RA7	9	6		ST/CMOS(3)	Oscillator crystal or external clock input.
OSC1			I		Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; otherwise CMOS.
CLKI			I		External clock source input. Always associated with pin function OSC1 (see OSC1/CLKI, OSC2/CLKO pins).
RA7			I/O	ST	Digital I/O.
OSC2/CLKO/RA6	10	7		—	Oscillator crystal or clock output.
OSC2			O		Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO			O		In RC mode, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6			I/O	ST	Digital I/O.
$\overline{MCLR}$/VPP/RE3	1	26		ST	Master Clear (input) or programming voltage (output).
$\overline{MCLR}$			I		Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP			P		Programming voltage input.
RE3			I	ST	Digital input only pin.
					PORTA is a bidirectional I/O port.
RA0/AN0	2	27		TTL	
RA0			I/O		Digital I/O.
AN0			I		Analog input 0.
RA1/AN1	3	28		TTL	
RA1			I/O		Digital I/O.
AN1			I		Analog input 1.
RA2/AN2/VREF-/CVREF	4	1		TTL	
RA2			I/O		Digital I/O.
AN2			I		Analog input 2.
VREF-			I		A/D reference voltage input (low).
CVREF			0		Comparator voltage reference output.
RA3/AN3/VREF+	5	2		TTL	
RA3			I/O		Digital I/O.
AN3			I		Analog input 3.
VREF+			I		A/D reference voltage input (high).
RA4/T0CKI/C1OUT	6	3		ST	
RA4			I/O		Digital I/O – Open-drain when configured as output.
T0CKI			I		Timer0 external clock input.
C1OUT			O		Comparator 1 output bit.
RA5/AN4/LVDIN/$\overline{SS}$/C2OUT	7	4		TTL	
RA5			I/O		Digital I/O.
AN4			I		Analog input 4.
LVDIN			I/O		Low-Voltage Detect input.
$\overline{SS}$			I		SPI slave select input.
C2OUT			O		Comparator 2 output bit.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.
4: Pin location of CCP2 is determined by the CCPMX bit in Configuration Word Register 1.

TABLE 1-3: PIC16F747 AND PIC16F777 PINOUT DESCRIPTION (CONTINUED)

Pin Name	PDIP Pin #	QFN Pin #	TQFP Pin #	I/O/P Type	Buffer Type	Description
						PORTD is a bidirectional I/O port or Parallel Slave Port when interfacing to a microprocessor bus.
RD0/PSP0	19	38	38		ST/TTL(3)	
RD0				I/O		Digital I/O.
PSP0				I/O		Parallel Slave Port data.
RD1/PSP1	20	39	39		ST/TTL(3)	
RD1				I/O		Digital I/O.
PSP1				I/O		Parallel Slave Port data.
RD2/PSP2	21	40	40		ST/TTL(3)	
RD2				I/O		Digital I/O.
PSP2				I/O		Parallel Slave Port data.
RD3/PSP3	22	41	41		ST/TTL(3)	
RD3				I/O		Digital I/O.
PSP3				I/O		Parallel Slave Port data.
RD4/PSP4	27	2	2		ST/TTL(3)	
RD4				I/O		Digital I/O.
PSP4				I/O		Parallel Slave Port data.
RD5/PSP5	28	3	3		ST/TTL(3)	
RD5				I/O		Digital I/O.
PSP5				I/O		Parallel Slave Port data.
RD6/PSP6	29	4	4		ST/TTL(3)	
RD6				I/O		Digital I/O.
PSP6				I/O		Parallel Slave Port data.
RD7/PSP7	30	5	5		ST/TTL(3)	
RD7				I/O		Digital I/O.
PSP7				I/O		Parallel Slave Port data.
						PORTE is a bidirectional I/O port.
RE0/$\overline{RD}$/AN5	8	25	25		ST/TTL(3)	
RE0				I/O		Digital I/O.
$\overline{RD}$				I		Read control for Parallel Slave Port.
AN5				I		Analog input 5.
RE1/$\overline{WR}$/AN6	9	26	26		ST/TTL(3)	
RE1				I/O		Digital I/O.
$\overline{WR}$				I		Write control for Parallel Slave Port.
AN6				I		Analog input 6.
RE2/$\overline{CS}$/AN7	10	27	27		ST/TTL(3)	
RE2				I/O		Digital I/O.
$\overline{CS}$				I		Chip select control for Parallel Slave Port.
AN7				I		Analog input 7.
VSS	—	31	—	P	—	Analog ground reference.
VSS	12, 31	6, 30	6, 29	P	—	Ground reference for logic and I/O pins.
VDD	—	8	—	P	—	Analog positive supply.
VDD	11, 32	7, 28	7, 28	P	—	Positive supply for logic and I/O pins.
NC	—	13, 29	12, 13, 33, 34	—	—	These pins are not internally connected. These pins should be left unconnected.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: This buffer is a Schmitt Trigger input when configured as a general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

4: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

5: Pin location of CCP2 is determined by the CCPMX bit in Configuration Word Register 1.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page
Bank 2											
100h(4)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	30, 180
101h	TMR0	Timer0 Module Register								xxxx xxxx	76, 180
102h(4)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	29, 180
103h(4)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	21, 180
104h(4)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	30, 180
105h	WDTCON	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	---0 1000	187
106h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	64, 180
107h	—	Unimplemented								—	—
108h	—	Unimplemented								—	—
109h	LVDCON	—	—	IRVST	LVDEN	LVDL3	LVDL2	LVDL1	LVDL0	--00 0101	176
10Ah(1,4)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	23, 180
10Bh(4)	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	25, 180
10Ch	PMDATA	EEPROM Data Register Low Byte								xxxx xxxx	32, 181
10Dh	PMADR	EEPROM Address Register Low Byte								xxxx xxxx	32, 181
10Eh	PMDATH	—	—	EEPROM Data Register High Byte						--xx xxxx	32, 181
10Fh	PMADRH	—	—	—	—	EEPROM Address Register High Byte				---- xxxx	32, 181
Bank 3											
180h(4)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	30, 180
181h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	22, 180
182h(4)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	29, 180
183h(4)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	21, 180
184h(4)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	30, 180
185h	—	Unimplemented								—	—
186h	TRISB	PORTB Data Direction Register								1111 1111	64, 181
187h	—	Unimplemented								—	—
188h	—	Unimplemented								—	—
189h	—	Unimplemented								—	—
18Ah(1,4)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	23, 180
18Bh(4)	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	25, 180
18Ch	PMCON1	r(6)	—	—	—	—	—	—	RD	1--- ---0	32, 181
18Dh	—	Reserved, maintain clear								—	—
18Eh	—	Reserved, maintain clear								—	—
18Fh	—	Reserved, maintain clear								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, — = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> bits, whose contents are transferred to the upper byte of the program counter during branches (CALL or GOTO).

2: Other (non Power-up) Resets include external Reset through $\overline{MCLR}$ and Watchdog Timer Reset.

3: Bits PSPIE and PSPIF are reserved on the 28-pin devices; always maintain these bits clear.

4: These registers can be addressed from any bank.

5: PORTD, PORTE, TRISD and TRISE are not physically implemented on the 28-pin devices (except for RE3), read as '0'.

6: This bit always reads as a '1'.

7: OSCCON<OSTS> bit resets to '0' with dual-speed start-up and LP, HS or HS-PLL selected as the oscillator.

8: RE3 is an input only. The state of the TRISE3 bit has no effect and will always read '1'.

4.7.3.2 Returning to Primary Oscillator with a Reset

A Reset will clear SCS<1:0> back to '00'. The sequence for starting the primary oscillator following a Reset is the same for all forms of Reset, including POR. There is no transition sequence from the alternate system clock to the primary system clock on a Reset condition. Instead, the device will reset the state of the OSCCON register and default to the primary system clock. The sequence of events that take place after this will depend upon the value of the FOSC bits in the Configuration register. If the external oscillator is configured as a crystal (HS, XT or LP), the CPU will be held in the Q1 state until 1024 clock cycles have transpired on the primary clock. This is necessary because the crystal oscillator had been powered down until the time of the transition.

During the oscillator start-up time, instruction execution and/or peripheral operation is suspended.

Note:	If Two-Speed Clock Start-up mode is enabled, the INTRC will act as the system clock until the Oscillator Start-up Timer has timed out.

If the primary system clock is either RC, EC or INTRC, the CPU will begin operating on the first Q1 cycle following the wake-up event. This means that there is no oscillator start-up time required because the primary clock is already stable; however, there is a delay between the wake-up event and the following Q2. An internal delay timer of 5-10 μs will suspend operation after the Reset to allow the CPU to become ready for code execution. The CPU and peripheral clock will be held in the first Q1.

The sequence of events is as follows:

1. A device Reset is asserted from one of many sources (WDT, BOR, MCLR, etc.).
2. The device resets and the CPU start-up timer is enabled if in Sleep mode. The device is held in Reset until the CPU start-up time-out is complete.
3. If the primary system clock is configured as an external oscillator (HS, XT, LP), then the OST will be active waiting for 1024 clocks of the primary system clock. While waiting for the OST, the device will be held in Reset. The OST and CPU start-up timers run in parallel.
4. After both the CPU start-up timer and the Oscillator Start-up Timer have timed out, the device will wait for one additional clock cycle and instruction execution will begin.

FIGURE 4-10: TIMING LP CLOCK TO PRIMARY SYSTEM CLOCK AFTER RESET (HS, XT, LP)

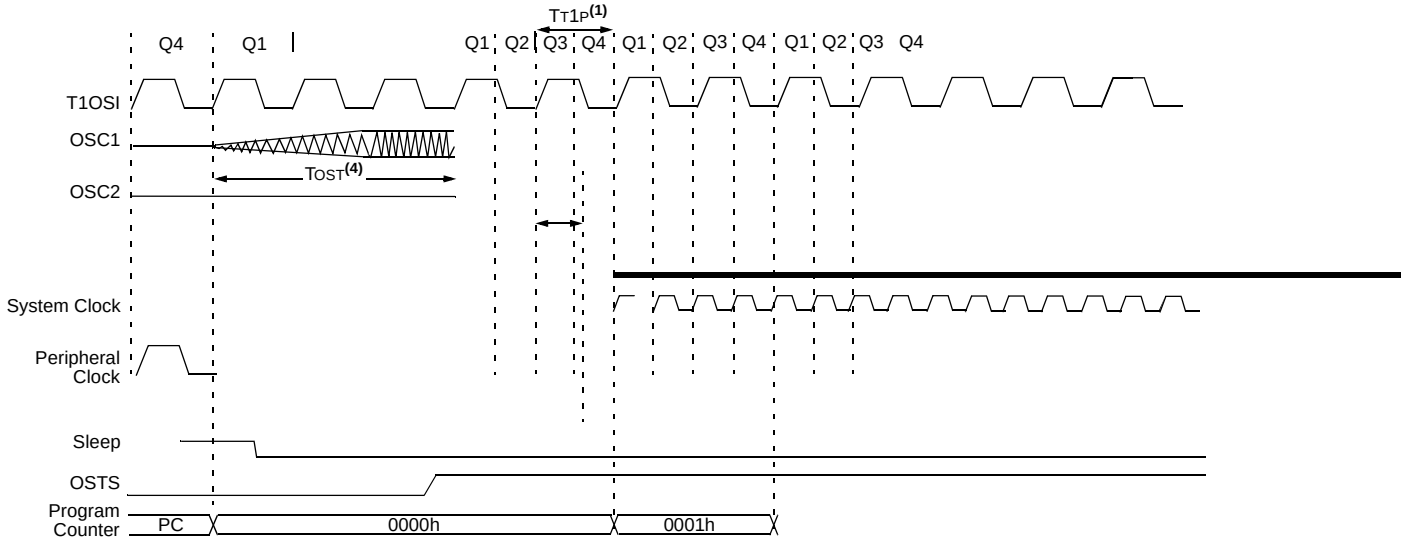
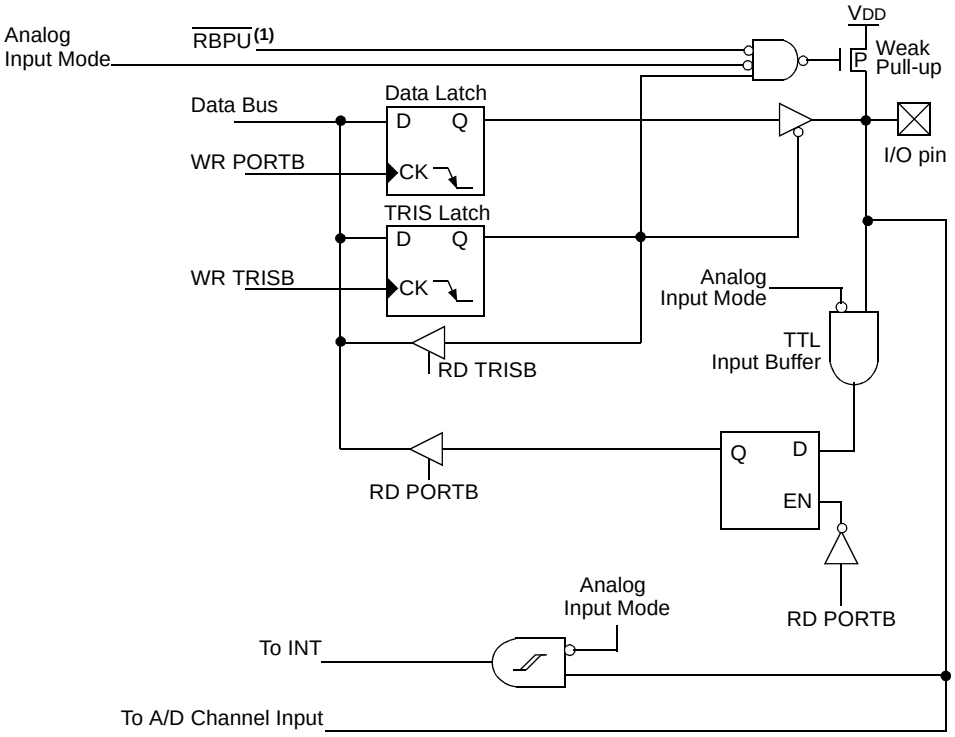
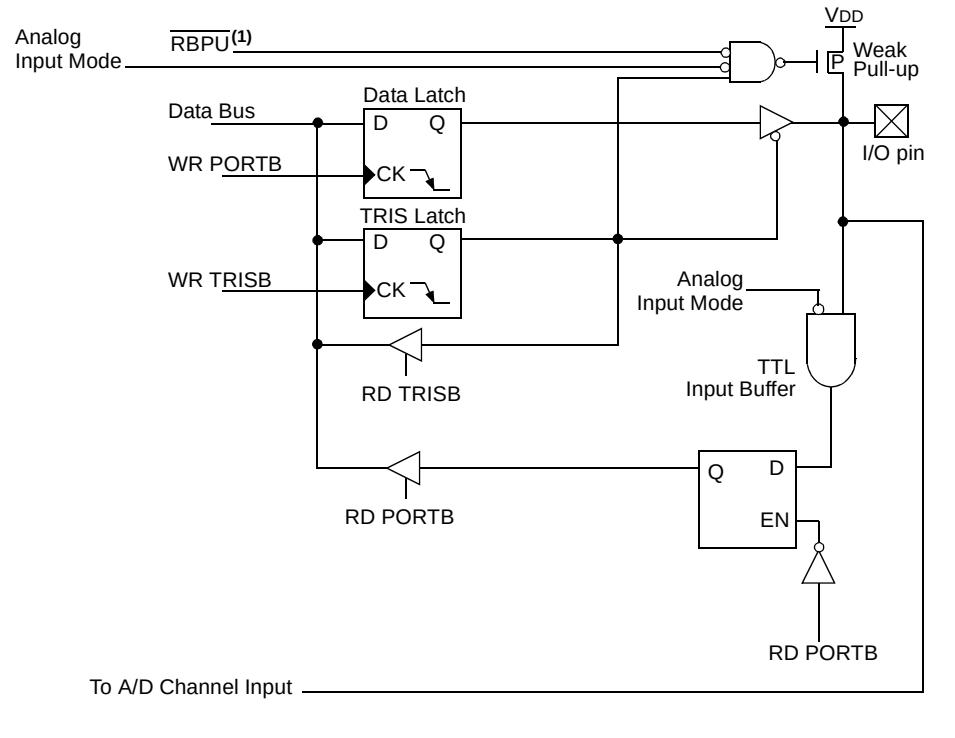


FIGURE 5-8: BLOCK DIAGRAM OF RB0/INT/AN12 PIN



Note 1: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the $\overline{\text{RBPU}}$ bit.

FIGURE 5-9: BLOCK DIAGRAM OF RB1/AN10 PIN



Note 1: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the $\overline{\text{RBPU}}$ bit.

10.4.9 I²C MASTER MODE REPEATED START CONDITION TIMING

A Repeated Start condition occurs when the RSEN bit (SSPCON2<1>) is programmed high and the I²C logic module is in the Idle state. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the Baud Rate Generator is loaded with the contents of SSPADD<5:0> and begins counting. The SDA pin is released (brought high) for one Baud Rate Generator count (TBRG). When the Baud Rate Generator times out, if SDA is sampled high, the SCL pin will be deasserted (brought high). When SCL is sampled high, the Baud Rate Generator is reloaded with the contents of SSPADD<6:0> and begins counting. SDA and SCL must be sampled high for one TBRG. This action is then followed by assertion of the SDA pin (SDA = 0) for one TBRG while SCL is high. Following this, the RSEN bit (SSPCON2<1>) will be automatically cleared and the Baud Rate Generator will not be reloaded, leaving the SDA pin held low. As soon as a Start condition is detected on the SDA and SCL pins, the S bit (SSPSTAT<3>) will be set. The SSPIF bit will not be set until the Baud Rate Generator has timed out.

Note 1: If RSEN is programmed while any other event is in progress, it will not take effect.

2: A bus collision during the Repeated Start condition occurs if:

- SDA is sampled low when SCL goes from low-to-high.
- SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data '1'.

Immediately following the SSPIF bit getting set, the user may write the SSPBUF with the 7-bit address in 7-bit mode or the default first address in 10-bit mode. After the first eight bits are transmitted and an ACK is received, the user may then transmit an additional eight bits of address (10-bit mode) or eight bits of data (7-bit mode).

10.4.9.1 WCOL Status Flag

If the user writes the SSPBUF when a Repeated Start sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

Note: Because queueing of events is not allowed, writing of the lower 5 bits of SSPCON2 is disabled until the Repeated Start condition is complete.

FIGURE 10-20: REPEATED START CONDITION WAVEFORM

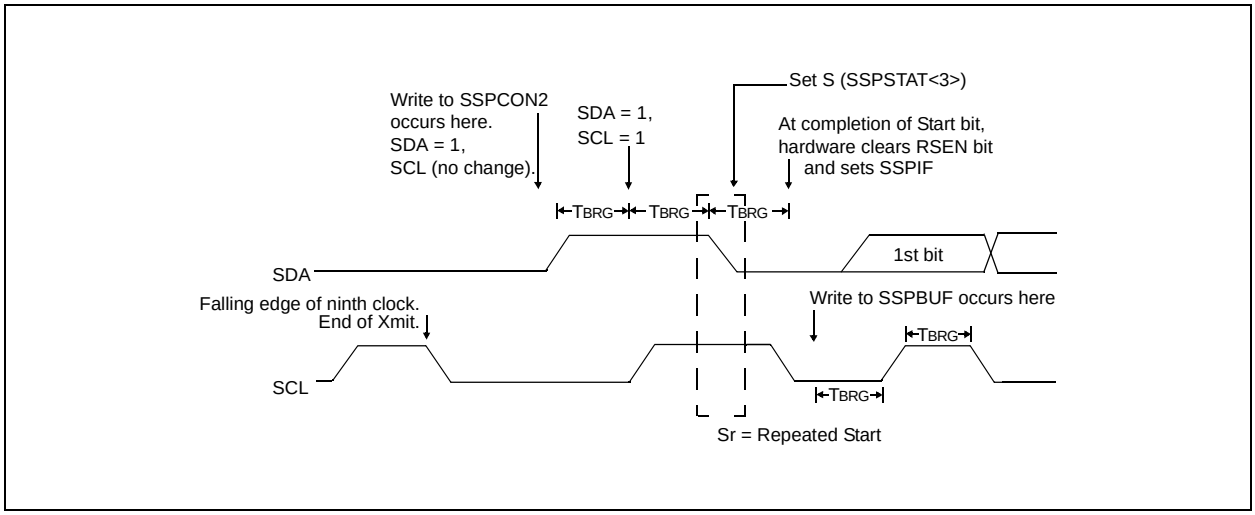


FIGURE 14-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

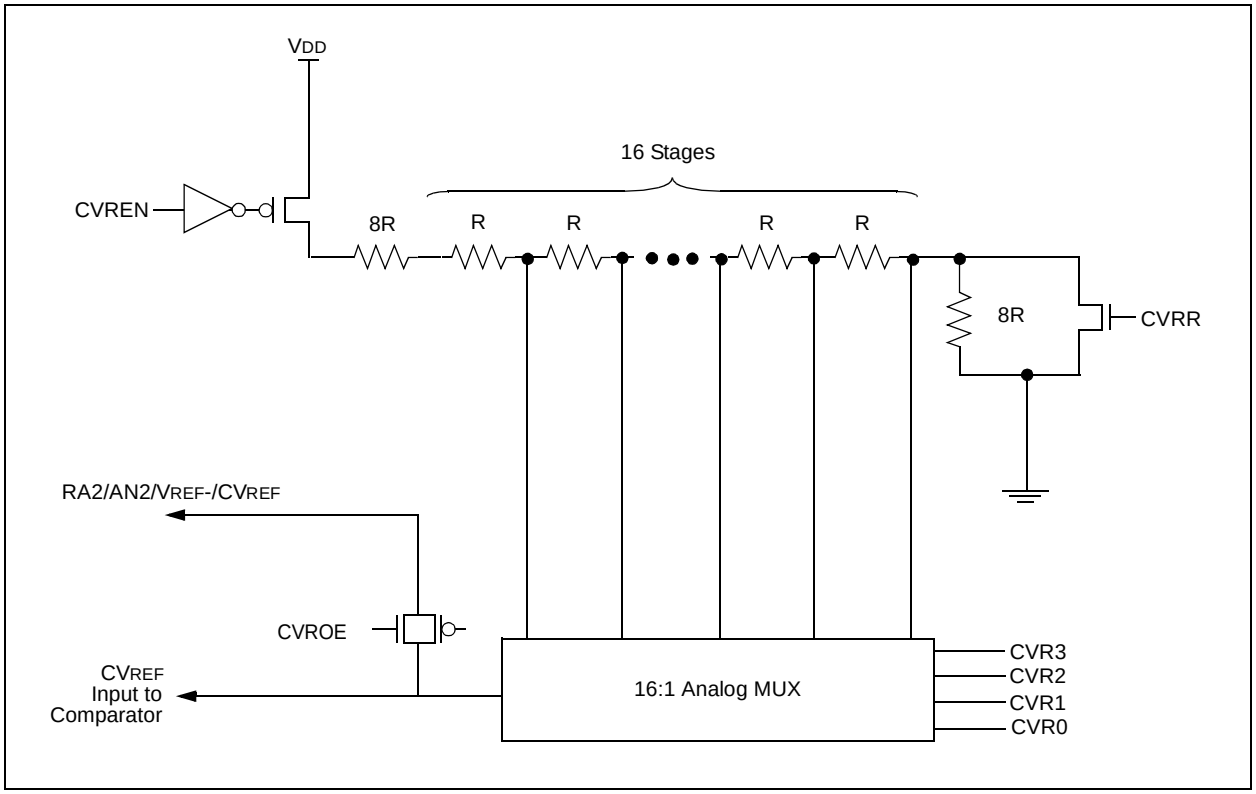


TABLE 14-1: REGISTERS ASSOCIATED WITH COMPARATOR VOLTAGE REFERENCE

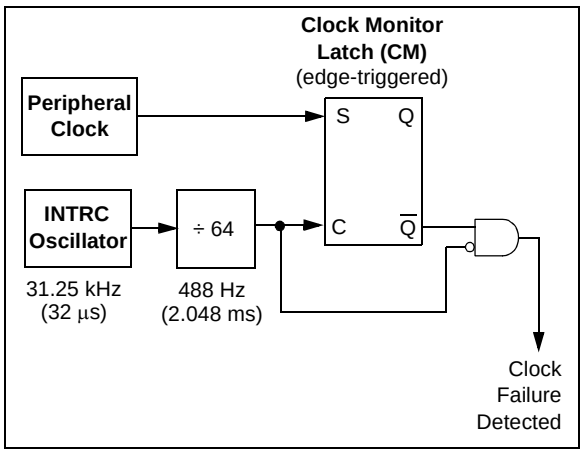
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on all other Resets
9Dh	CVRCON	CVREN	CVROE	CVRR	—	CVR3	CVR2	CVR1	CVR0	000- 0000	000- 0000
9Ch	CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0111	0000 0111

Legend: x = unknown, u = unchanged, — = unimplemented, read as '0'.
Shaded cells are not used with the comparator voltage reference.

15.17.4 FAIL-SAFE OPTION

The Fail-Safe Clock Monitor (FSCM) is designed to allow the device to continue to operate even in the event of an oscillator failure.

FIGURE 15-14: FSCM BLOCK DIAGRAM



The FSCM function is enabled by setting the FCMEN bit in Configuration Word Register 2.

In the event of an oscillator failure, the FSCM will generate an oscillator fail interrupt and will switch the system clock over to the internal oscillator. The system will continue to come from the internal oscillator until the Fail-Safe condition is exited. The Fail-Safe condition is exited with either a Reset, the execution of a SLEEP instruction or a write to the SCS bits of a different value.

The frequency of the internal oscillator will depend upon the value contained in the IRCF bits. Another clock source can be selected via the IRCF and the SCS bits of the OSCCON register.

The FSCM sample clock is generated by dividing the INTRC clock by 64. This will allow enough time between FSCM sample clocks for a system clock edge to occur.

On the rising edge of the postscaled clock, the monitoring latch (CM = 0) will be cleared. On a falling edge of the primary or secondary system clock, the monitoring latch will be set (CM = 1). In the event that a falling edge of the postscaled clock occurs and the monitoring latch is not set, a clock failure has been detected.

While in Fail-Safe mode, a Reset will exit the Fail-Safe condition. If the primary clock source is configured for a crystal, the OST timer will wait for the 1024 clock cycles for the OST time-out and the device will continue running from the internal oscillator until the OST is complete. A SLEEP instruction, or a write to the SCS bits (where SCS bits do not = 00), can be performed to put the device into a low-power mode.

If Reset occurs while in Fail-Safe mode and the primary clock source is EC or RC, then the device will immediately switch back to EC or RC mode.

Note:	Two-Speed Start-up is automatically enabled when the Fail-Safe option is enabled.

15.17.4.1 Fail-Safe in Low-Power Mode

A change of SCS<1:0> or the SLEEP instruction will end the Fail-Safe condition. The system clock will default to the source selected by the SCS bits, which is either T1OSC, INTRC or none (Sleep mode). However, the FSCM will continue to monitor the system clock. If the secondary clock fails, the device will immediately switch to the internal oscillator clock. If OSFIE is set, an interrupt will be generated.

FIGURE 15-15: FSCM TIMING DIAGRAM