



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f777-i-ml

2.2.2.5 PIR1 Register

The PIR1 register contains the individual flag bits for the peripheral interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the Global Interrupt Enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt bits are clear prior to enabling an interrupt.

REGISTER 2-5: PIR1: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 1 (ADDRESS 0Ch)

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit 7				bit 0			

- bit 7 **PSPIF:** Parallel Slave Port Read/Write Interrupt Flag bit⁽¹⁾
 1 = A read or a write operation has taken place (must be cleared in software)
 0 = No read or write has occurred
Note: PSPIF is reserved on 28-pin devices; always maintain this bit clear.
- bit 6 **ADIF:** A/D Converter Interrupt Flag bit
 1 = An A/D conversion is completed (must be cleared in software)
 0 = The A/D conversion is not complete
- bit 5 **RCIF:** AUSART Receive Interrupt Flag bit
 1 = The AUSART receive buffer is full
 0 = The AUSART receive buffer is empty
- bit 4 **TXIF:** AUSART Transmit Interrupt Flag bit
 1 = The AUSART transmit buffer is empty
 0 = The AUSART transmit buffer is full
- bit 3 **SSPIF:** Synchronous Serial Port (SSP) Interrupt Flag bit
 1 = The SSP interrupt condition has occurred and must be cleared in software before returning from the Interrupt Service Routine. The conditions that will set this bit are:
SPI:
 A transmission/reception has taken place.
I²C Slave:
 A transmission/reception has taken place.
I²C Master:
 A transmission/reception has taken place. The initiated Start condition was completed by the SSP module. The initiated Stop condition was completed by the SSP module. The initiated Restart condition was completed by the SSP module. The initiated Acknowledge condition was completed by the SSP module. A Start condition occurred while the SSP module was Idle (multi-master system). A Stop condition occurred while the SSP module was Idle (multi-master system).
 0 = No SSP interrupt condition has occurred
- bit 2 **CCP1IF:** CCP1 Interrupt Flag bit
Capture mode:
 1 = A TMR1 register capture occurred (must be cleared in software)
 0 = No TMR1 register capture occurred
Compare mode:
 1 = A TMR1 register compare match occurred (must be cleared in software)
 0 = No TMR1 register compare match occurred
PWM mode:
 Unused in this mode.
- bit 1 **TMR2IF:** TMR2 to PR2 Match Interrupt Flag bit
 1 = TMR2 to PR2 match occurred (must be cleared in software)
 0 = No TMR2 to PR2 match occurred
- bit 0 **TMR1IF:** TMR1 Overflow Interrupt Flag bit
 1 = TMR1 register overflowed (must be cleared in software)
 0 = TMR1 register did not overflow

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

PIC16F7X7

2.2.2.6 PIE2 Register

The PIE2 register contains the individual enable bits for the CCP2 and CCP3 peripheral interrupts.

REGISTER 2-6: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2 (ADDRESS 8Dh)

R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
OSFIE	CMIE	LVDIE	—	BCLIE	—	CCP3IE	CCP2IE
bit 7						bit 0	

- bit 7 **OSFIE:** Oscillator Fail Interrupt Enable bit
1 = Enabled
0 = Disabled
- bit 6 **CMIE:** Comparator Interrupt Enable bit
1 = Enabled
0 = Disabled
- bit 5 **LVDIE:** Low-Voltage Detect Interrupt Enable bit
1 = LVD interrupt is enabled
0 = LVD interrupt is disabled
- bit 4 **Unimplemented:** Read as '0'
- bit 3 **BCLIE:** Bus Collision Interrupt Enable bit
1 = Enable bus collision interrupt in the SSP when configured for I²C Master mode
0 = Disable bus collision interrupt in the SSP when configured for I²C Master mode
- bit 2 **Unimplemented:** Read as '0'
- bit 1 **CCP3IE:** CCP3 Interrupt Enable bit
1 = Enables the CCP3 interrupt
0 = Disables the CCP3 interrupt
- bit 0 **CCP2IE:** CCP2 Interrupt Enable bit
1 = Enables the CCP2 interrupt
0 = Disables the CCP2 interrupt

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

4.7.4 EXITING SLEEP WITH AN INTERRUPT

Any interrupt, such as WDT or INT0, will cause the part to leave the Sleep mode.

The SCS bits are unaffected by a `SLEEP` command and are the same before and after entering and leaving Sleep. The clock source used after an exit from Sleep is determined by the SCS bits.

4.7.4.1 Sequence of Events

If **SCS<1:0> = 00**:

1. The device is held in Sleep until the CPU start-up time-out is complete.
2. If the primary system clock is configured as an external oscillator (HS, XT, LP), then the OST will be active waiting for 1024 clocks of the primary system clock. While waiting for the OST, the device will be held in Sleep unless Two-Speed Start-up is enabled. The OST and CPU start-up timers run in parallel. Refer to **Section 15.17.3 “Two-Speed Clock Start-up Mode”** for details on Two-Speed Start-up.
3. After both the CPU start-up timer and the Oscillator Start-up Timer have timed out, the device will exit Sleep and begin instruction execution with the primary clock defined by the FOSC bits.

If **SCS<1:0> = 01 or 10**:

1. The device is held in Sleep until the CPU start-up time-out is complete.
2. After the CPU start-up timer has timed out, the device will exit Sleep and begin instruction execution with the selected oscillator mode.

Note: If a user changes SCS<1:0> just before entering Sleep mode, the system clock used when exiting Sleep mode could be different than the system clock used when entering Sleep mode.

As an example, if SCS<1:0> = 01, T1OSC is the system clock and the following instructions are executed:

```
BCF      OSCCON, SCS0
SLEEP
```

then a clock change event is executed. If the primary oscillator is XT, LP or HS, the core will continue to run off T1OSC and execute the `SLEEP` command.

When Sleep is exited, the part will resume operation with the primary oscillator after the OST has expired.

PIC16F7X7

TABLE 5-5: PORTC FUNCTIONS

Name	Bit#	Buffer Type	Function
RC0/T1OSO/T1CKI	bit 0	ST	Input/output port pin or Timer1 oscillator output/Timer1 clock input.
RC1/T1OSI/CCP2	bit 1	ST	Input/output port pin or Timer1 oscillator input or Capture 2 input/Compare 2 output/PWM 2 output.
RC2/CCP1	bit 2	ST	Input/output port pin or Capture 1 input/Compare 1 output/PWM 1 output.
RC3/SCK/SCL	bit 3	ST	RC3 can also be the synchronous serial clock for both SPI and I ² C™ modes.
RC4/SDI/SDA	bit 4	ST	RC4 can also be the SPI data in (SPI mode) or data I/O (I ² C mode).
RC5/SDO	bit 5	ST	Input/output port pin or Synchronous Serial Port data output.
RC6/TX/CK	bit 6	ST	Input/output port pin or AUSART asynchronous transmit or synchronous clock.
RC7/RX/DT	bit 7	ST	Input/output port pin or AUSART asynchronous receive or synchronous data.

Legend: ST = Schmitt Trigger input

TABLE 5-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged

PIC16F7X7

7.9 Resetting Timer1 Register Pair (TMR1H, TMR1L)

TMR1H and TMR1L registers are not reset to 00h on a POR, or any other Reset, except by the CCP1 special event triggers.

T1CON register is reset to 00h on a Power-on Reset or a Brown-out Reset, which shuts off the timer and leaves a 1:1 prescale. In all other Resets, the register is unaffected.

7.10 Timer1 Prescaler

The prescaler counter is cleared on writes to the TMR1H or TMR1L registers.

7.11 Using Timer1 as a Real-Time Clock

Adding an external LP oscillator to Timer1 (such as the one described in **Section 7.6 “Timer1 Oscillator”**) gives users the option to include RTC functionality in their applications. This is accomplished with an inexpensive watch crystal to provide an accurate time base and several lines of application code to calculate the time. When operating in Sleep mode and using a

battery or supercapacitor as a power source, it can completely eliminate the need for a separate RTC device and battery backup.

The application code routine, `RTCisr`, shown in Example 7-3, demonstrates a simple method to increment a counter at one-second intervals using an Interrupt Service Routine. Incrementing the TMR1 register pair to overflow, triggers the interrupt and calls the routine which increments the seconds counter by one; additional counters for minutes and hours are incremented as the previous counter overflows.

Since the register pair is 16 bits wide, counting up to overflow the register directly from a 32.768 kHz clock would take 2 seconds. To force the overflow at the required one-second intervals, it is necessary to preload it. The simplest method is to set the MSb of TMR1H with a `BSF` instruction. Note that the TMR1L register is never preloaded or altered; doing so may introduce cumulative error over many cycles.

For this method to be accurate, Timer1 must operate in Asynchronous mode and the Timer1 overflow interrupt must be enabled (`PIE1<0> = 1`) as shown in the routine, `RTCinit`. The Timer1 oscillator must also be enabled and running at all times.

EXAMPLE 7-3: IMPLEMENTING A REAL-TIME CLOCK USING A TIMER1 INTERRUPT SERVICE

RTCinit	BANKSEL	TMR1H	
	MOVLW	0x80	; Preload TMR1 register pair
	MOVWF	TMR1H	; for 1 second overflow
	CLRF	TMR1L	
	MOVLW	b'00001111'	; Configure for external clock,
	MOVWF	T1CON	; Asynchronous operation, external oscillator
	CLRF	secs	; Initialize timekeeping registers
	CLRF	mins	
	MOVLW	.12	
	MOVWF	hours	
	BANKSEL	PIE1	
	BSF	PIE1, TMR1IE	; Enable Timer1 interrupt
	RETURN		
RTCisr	BANKSEL	TMR1H	
	BSF	TMR1H, 7	; Preload for 1 sec overflow
	BCF	PIR1, TMR1IF	; Clear interrupt flag
	INCF	secs, F	; Increment seconds
	MOVF	secs, w	
	SUBLW	.60	
	BTFSS	STATUS, Z	; 60 seconds elapsed?
	RETURN		; No, done
	CLRF	seconds	; Clear seconds
	INCF	mins, f	; Increment minutes
	MOVF	mins, w	
	SUBLW	.60	
	BTFSS	STATUS, Z	; 60 seconds elapsed?
	RETURN		; No, done
	CLRF	mins	; Clear minutes
	INCF	hours, f	; Increment hours
	MOVF	hours, w	
	SUBLW	.24	
	BTFSS	STATUS, Z	; 24 hours elapsed?
	RETURN		; No, done
	CLRF	hours	; Clear hours
	RETURN		; Done

10.4.12 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable bit, ACKEN (SSPCON2<4>). When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit are presented on the SDA pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (TBRG) and the SCL pin is deasserted (pulled high). When the SCL pin is sampled high (clock arbitration), the Baud Rate Generator counts for TBRG. The SCL pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSP module then goes into Idle mode (Figure 10-23).

10.4.12.1 WCOL Status Flag

If the user writes the SSPBUF when an Acknowledge sequence is in progress, then WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

10.4.13 STOP CONDITION TIMING

A Stop bit is asserted on the SDA pin at the end of a receive/transmit by setting the Stop Sequence Enable bit, PEN (SSPCON2<2>). At the end of a receive/transmit, the SCL line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDA line low. When the SDA line is sampled low, the Baud Rate Generator is reloaded and counts down to '0'. When the Baud Rate Generator times out, the SCL pin will be brought high and one TBRG (Baud Rate Generator rollover count) later, the SDA pin will be deasserted. When the SDA pin is sampled high while SCL is high, the P bit (SSPSTAT<4>) is set. A TBRG later, the PEN bit is cleared and the SSPIF bit is set (Figure 10-24).

10.4.13.1 WCOL Status Flag

If the user writes the SSPBUF when a Stop sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write doesn't occur).

FIGURE 10-23: ACKNOWLEDGE SEQUENCE WAVEFORM

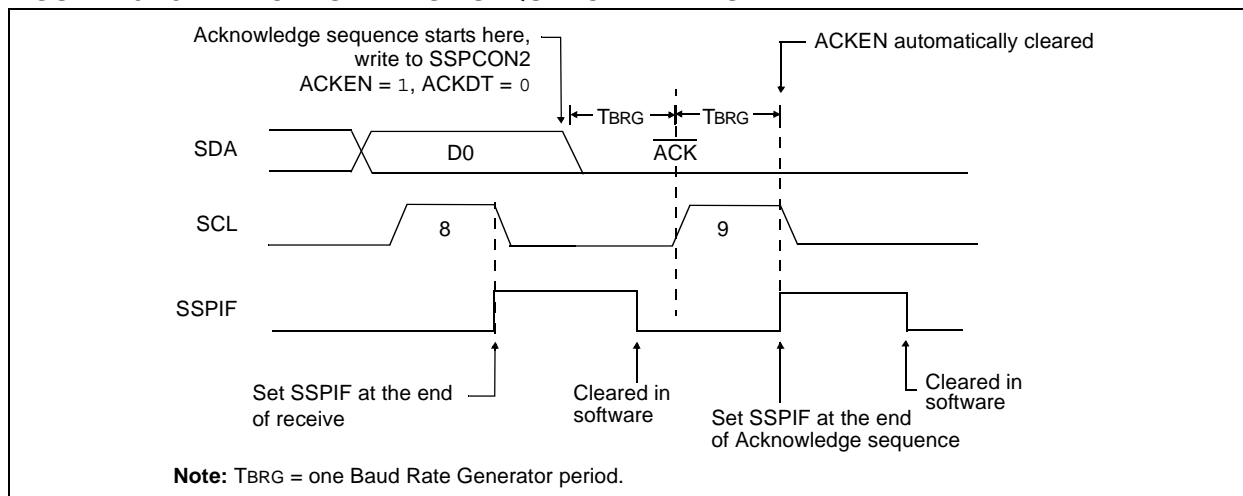
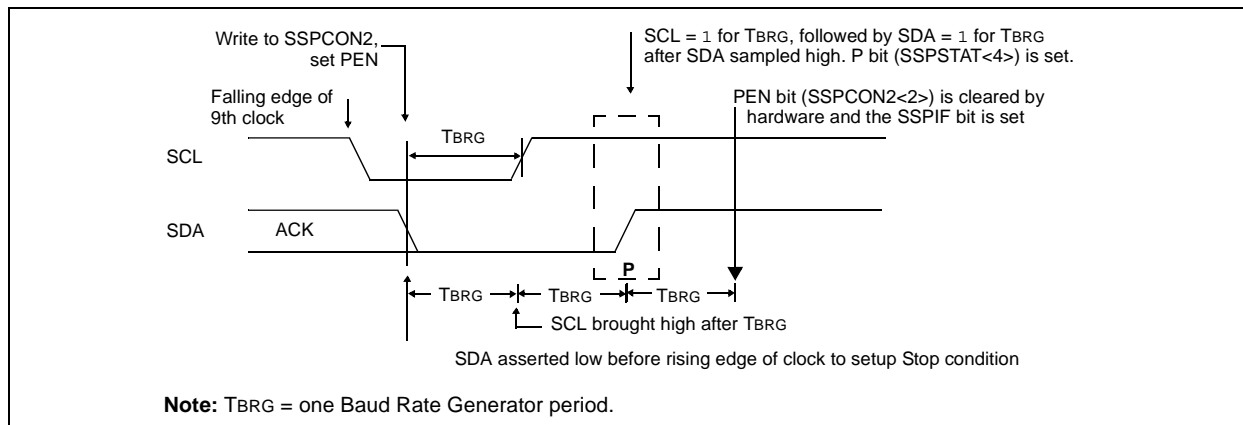


FIGURE 10-24: STOP CONDITION RECEIVE OR TRANSMIT MODE



PIC16F7X7

NOTES:

15.17.4.2 FSCM and the Watchdog Timer

When a clock failure is detected, SCS<1:0> will be forced to '10' which will reset the WDT (if enabled).

15.17.4.3 POR or Wake from Sleep

The FSCM is designed to detect oscillator failure at any point after the device has exited Power-on Reset (POR) or low-power Sleep mode. When the primary system clock is EC, RC or INTRC modes, monitoring can begin immediately following these events.

For oscillator modes involving a crystal or resonator (HS, LP or XT), the situation is somewhat different. Since the oscillator may require a start-up time considerably longer than the FSCM sample clock time, a false clock failure may be detected. To prevent this, the internal oscillator block is automatically configured as the system clock and functions until the primary clock is stable (the OST and PLL timers have timed out). This is identical to Two-Speed Start-up mode. Once the primary clock is stable, the INTRC returns to its role as the FSCM source.

Note: The same logic that prevents false oscillator failure interrupts on POR, or wake from Sleep, will also prevent the detection of the oscillator's failure to start at all following these events. This can be avoided by monitoring the OSTS bit and using a timing routine to determine if the oscillator is taking too long to start. Even so, no oscillator failure interrupt will be flagged.

15.18 Power-Down Mode (Sleep)

Power-Down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the PD bit (Status<3>) is cleared, the TO (Status<4>) bit is set and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, low or high-impedance).

For lowest current consumption in this mode, place all I/O pins at either VDD or VSS, ensure no external circuitry is drawing current from the I/O pin, power-down the A/D and disable external clocks. Pull all I/O pins that are high-impedance inputs, high or low externally, to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or VSS for lowest current consumption. The contribution from on-chip pull-ups on PORTB should also be considered.

The MCLR pin must be at a logic high level (VIHMC).

15.18.1 WAKE-UP FROM SLEEP

The device can wake-up from Sleep through one of the following events:

1. External Reset input on MCLR pin.
2. Watchdog Timer wake-up (if WDT was enabled).
3. Interrupt from INT pin, RB port change or a peripheral interrupt.

External MCLR Reset will cause a device Reset. All other events are considered a continuation of program execution and cause a "wake-up". The TO and PD bits in the Status register can be used to determine the cause of the device Reset. The PD bit, which is set on power-up, is cleared when Sleep is invoked. The TO bit is cleared if a WDT time-out occurred and caused wake-up.

The following peripheral interrupts can wake the device from Sleep:

1. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
2. CCP Capture mode interrupt.
3. Special event trigger (Timer1 in Asynchronous mode using an external clock).
4. SSP (Start/Stop) bit detect interrupt.
5. SSP transmit or receive in Slave mode (SPI/I²C).
6. A/D conversion (when A/D clock source is RC).
7. EEPROM write operation completion.
8. Comparator output changes state.
9. AUSART RX or TX (Synchronous Slave mode).

Other peripherals cannot generate interrupts, since during Sleep, no on-chip clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is prefetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up occurs regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

PIC16F7X7

TABLE 16-2: PIC16F7X7 INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode				Status Affected	Notes
				MSb		LSb			
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C, DC, Z	1, 2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1, 2
CLRF	f	Clear f	1	00	0001	1fff	ffff	Z	2
CLRWF	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1, 2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1, 2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1, 2, 3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1, 2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1, 2, 3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1, 2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1, 2
MOVWF	f	Move W to f	1	00	0000	1fff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	1, 2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C, DC, Z	1, 2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1, 2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1, 2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1, 2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1, 2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C, DC, Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{\text{TO}}$, $\overline{\text{PD}}$	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into Standby mode	1	00	0000	0110	0011	$\overline{\text{TO}}$, $\overline{\text{PD}}$	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C, DC, Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

- Note 1:** When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- 2:** If this instruction is executed on the TMR0 register (and where applicable, $d = 1$), the prescaler will be cleared if assigned to the Timer0 module.
- 3:** If Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

Note: Additional information on the mid-range instruction set is available in the “PIC® Mid-Range MCU Family Reference Manual” (DS33023).

17.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

17.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

17.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

18.2 DC Characteristics: Power-Down and Supply Current

PIC16F737/747/767/777 (Industrial, Extended)

PIC16LF737/747/767/777 (Industrial) (Continued)

PIC16LF737/747/767/777 (Industrial)		Standard Operating Conditions (unless otherwise stated)					
		Operating temperature		-40°C ≤ TA ≤ +85°C for industrial			
PIC16F737/747/767/777 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated)					
		Operating temperature		-40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended			
Param No.	Device	Typ	Max	Units	Conditions		
	Supply Current (IDD) ^(2,3)						
	PIC16LF7X7	9	20	μA	-40°C	VDD = 2.0V	Fosc = 32 kHz (LP Oscillator)
		7	15	μA	+25°C		
		7	15	μA	+85°C		
	PIC16LF7X7	16	30	μA	-40°C	VDD = 3.0V	
		14	25	μA	+25°C		
		14	25	μA	+85°C		
	All devices	32	40	μA	-40°C	VDD = 5.0V	
		26	35	μA	+25°C		
		26	35	μA	+85°C		
	Extended devices	35	53	μA	+125°C		
	PIC16LF7X7	72	95	μA	-40°C	VDD = 2.0V	Fosc = 1 MHz (RC Oscillator) ⁽³⁾
		76	90	μA	+25°C		
		76	90	μA	+85°C		
	PIC16LF7X7	138	175	μA	-40°C	VDD = 3.0V	
		136	170	μA	+25°C		
		136	170	μA	+85°C		
	All devices	310	380	μA	-40°C	VDD = 5.0V	
		290	360	μA	+25°C		
		280	360	μA	+85°C		
Extended devices	330	500	μA	+125°C			

Legend: Shading of rows is to assist in readability of the table.

- Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{DD} or V_{SS} and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).
- 2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all I_{DD} measurements in active operation mode are:
 OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD} ;
 $\text{MCLR} = V_{DD}$; WDT enabled/disabled as specified.
- 3:** For RC oscillator configurations, current through R_{EXT} is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in $k\Omega$.

PIC16F7X7

18.2 DC Characteristics: Power-Down and Supply Current

PIC16F737/747/767/777 (Industrial, Extended)

PIC16LF737/747/767/777 (Industrial) (Continued)

PIC16LF737/747/767/777 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial					
PIC16F737/747/767/777 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
Param No.	Device	Typ	Max	Units	Conditions		
D025 (ΔIOSCB)	Timer1 Oscillator	Module Differential Currents (ΔIWDt, ΔIBOR, ΔILVD, ΔIOSCB, ΔIAD)					
		1.7	2.3	μA	-40°C	$V_{DD} = 2.0\text{V}$	32 kHz on Timer1
		1.8	2.3	μA	$+25^{\circ}\text{C}$		
		2.0	2.3	μA	$+85^{\circ}\text{C}$		
		2.2	3.8	μA	-40°C	$V_{DD} = 3.0\text{V}$	
		2.6	3.8	μA	$+25^{\circ}\text{C}$		
		2.9	3.8	μA	$+85^{\circ}\text{C}$		
		3.0	6.0	μA	-40°C	$V_{DD} = 5.0\text{V}$	
		3.2	6.0	μA	$+25^{\circ}\text{C}$		
	3.4	7.0	μA	$+85^{\circ}\text{C}$			
D026 (ΔIAD)	A/D Converter	0.001	2.0	μA	-40°C to $+85^{\circ}\text{C}$	$V_{DD} = 2.0\text{V}$	A/D on, Sleep, not converting
		0.001	2.0	μA	-40°C to $+85^{\circ}\text{C}$	$V_{DD} = 3.0\text{V}$	
		0.003	2.0	μA	-40°C to $+85^{\circ}\text{C}$	$V_{DD} = 5.0\text{V}$	
	Extended devices	4	8	mA	-40°C to $+125^{\circ}\text{C}$	$V_{DD} = 5.0\text{V}$	

Legend: Shading of rows is to assist in readability of the table.

- Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{DD} or V_{SS} and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).
- 2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all I_{DD} measurements in active operation mode are:
 OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD} ;
 MCLR = V_{DD} ; WDT enabled/disabled as specified.
- 3:** For RC oscillator configurations, current through R_{EXT} is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in $k\Omega$.

PIC16F7X7

FIGURE 18-9: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

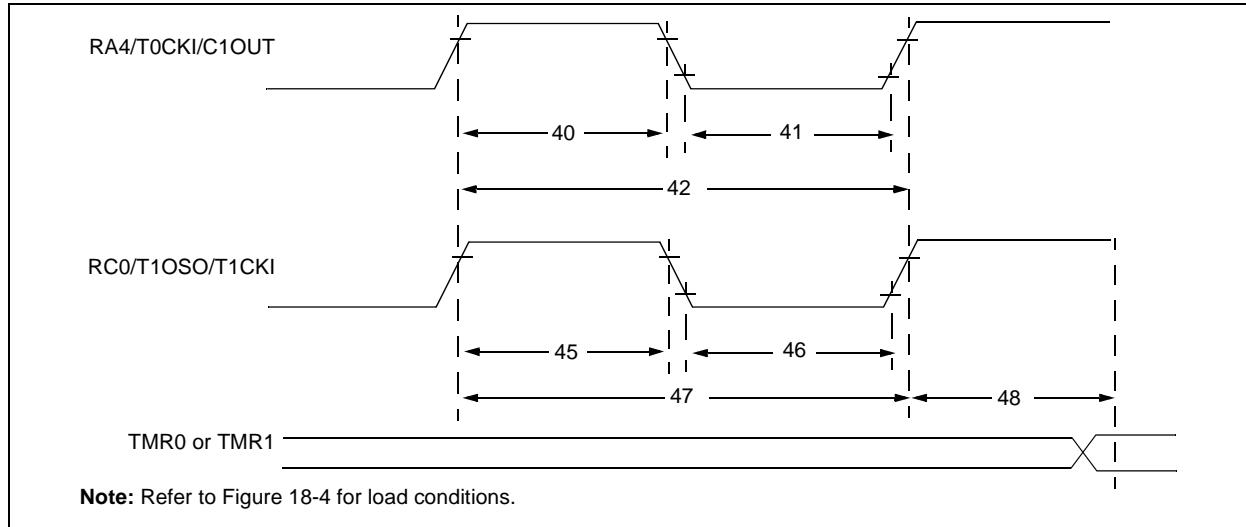


TABLE 18-7: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions	
40*	Tt0H	T0CKI High Pulse Width	No prescaler	0.5 Tcy + 20	—	—	ns	Must also meet parameter 42	
			With prescaler	10	—	—	ns		
41*	Tt0L	T0CKI Low Pulse Width	No prescaler	0.5 Tcy + 20	—	—	ns	Must also meet parameter 42	
			With prescaler	10	—	—	ns		
42*	Tt0P	T0CKI Period	No prescaler	Tcy + 40	—	—	ns	N = prescale value (2, 4, ..., 256)	
			With prescaler	Greater of: 20 or $\frac{Tcy + 40}{N}$	—	—	ns		
45*	Tt1H	T1CKI High Time	Synchronous, Prescaler = 1		0.5 Tcy + 20	—	—	Must also meet parameter 47	
			Synchronous, Prescaler = 2, 4, 8	PIC16F7X7	15	—	—		ns
				PIC16LF7X7	25	—	—		ns
			Asynchronous	PIC16F7X7	30	—	—		ns
				PIC16LF7X7	50	—	—		ns
46*	Tt1L	T1CKI Low Time	Synchronous, Prescaler = 1		0.5 Tcy + 20	—	—	Must also meet parameter 47	
			Synchronous, Prescaler = 2, 4, 8	PIC16F7X7	15	—	—		ns
				PIC16LF7X7	25	—	—		ns
			Asynchronous	PIC16F7X7	30	—	—		ns
				PIC16LF7X7	50	—	—		ns
47*	Tt1P	T1CKI Input Period	Synchronous	PIC16F7X7	Greater of: 30 or $\frac{Tcy + 40}{N}$	—	—	ns	N = prescale value (1, 2, 4, 8)
				PIC16LF7X7	Greater of: 50 or $\frac{Tcy + 40}{N}$	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	PIC16F7X7	60	—	—	ns	
				PIC16LF7X7	100	—	—	ns	
	Ft1	Timer1 Oscillator Input Frequency Range (oscillator enabled by setting bit T1OSCEN)			DC	—	200	kHz	
48	TCKEZTMR1	Delay from External Clock Edge to Timer Increment			2 Tosc	—	7 Tosc	—	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC16F7X7

FIGURE 18-18: AUSART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

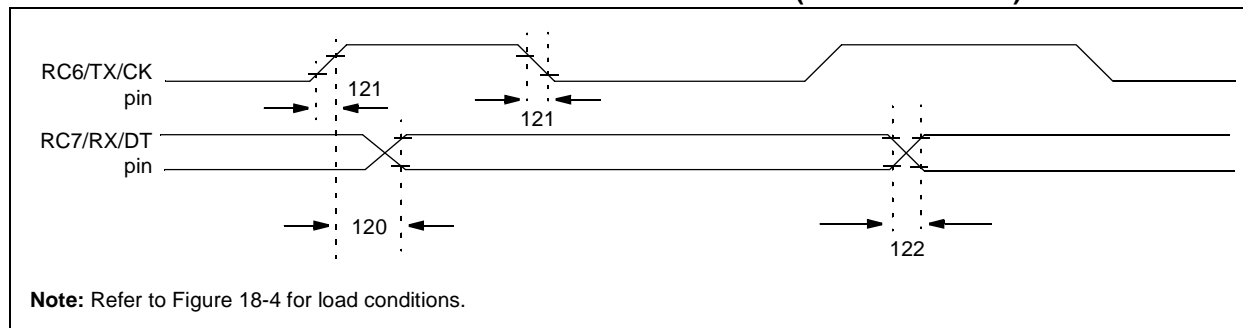


TABLE 18-13: AUSART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
120	T _{CKH2DTV}	<u>SYNC XMIT (MASTER & SLAVE)</u> Clock High to Data Out Valid					
			PIC16F7X7	—	—	80	ns
			PIC16LF7X7	—	—	100	ns
121	T _{CKRF}	Clock Out Rise Time and Fall Time (Master mode)	PIC16F7X7	—	—	45	ns
			PIC16LF7X7	—	—	50	ns
122	T _{DTRF}	Data Out Rise Time and Fall Time	PIC16F7X7	—	—	45	ns
			PIC16LF7X7	—	—	50	ns

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 18-19: AUSART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

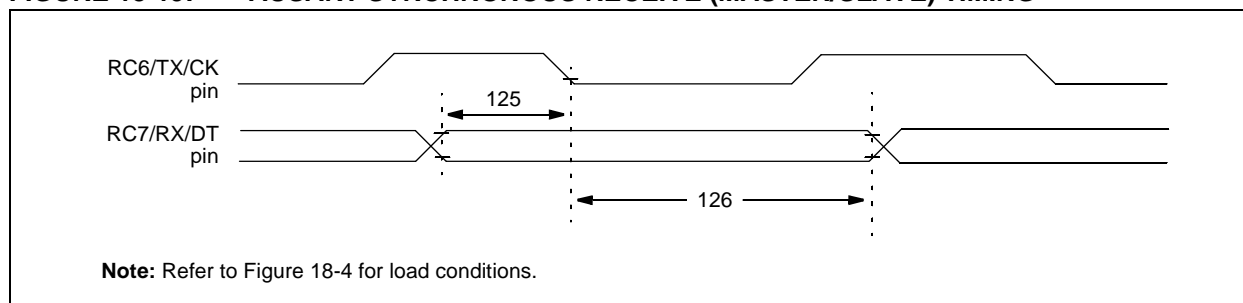


TABLE 18-14: AUSART SYNCHRONOUS RECEIVE REQUIREMENTS

Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
125	T _{DTV2CKL}	<u>SYNC RCV (MASTER & SLAVE)</u> Data Setup before CK ↓ (DT setup time)	15	—	—	ns	
126	T _{CKL2DTL}	Data Hold after CK ↓ (DT hold time)	15	—	—	ns	

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 19-5: TYPICAL I_{DD} vs. F_{osc} OVER V_{DD} (LP MODE)

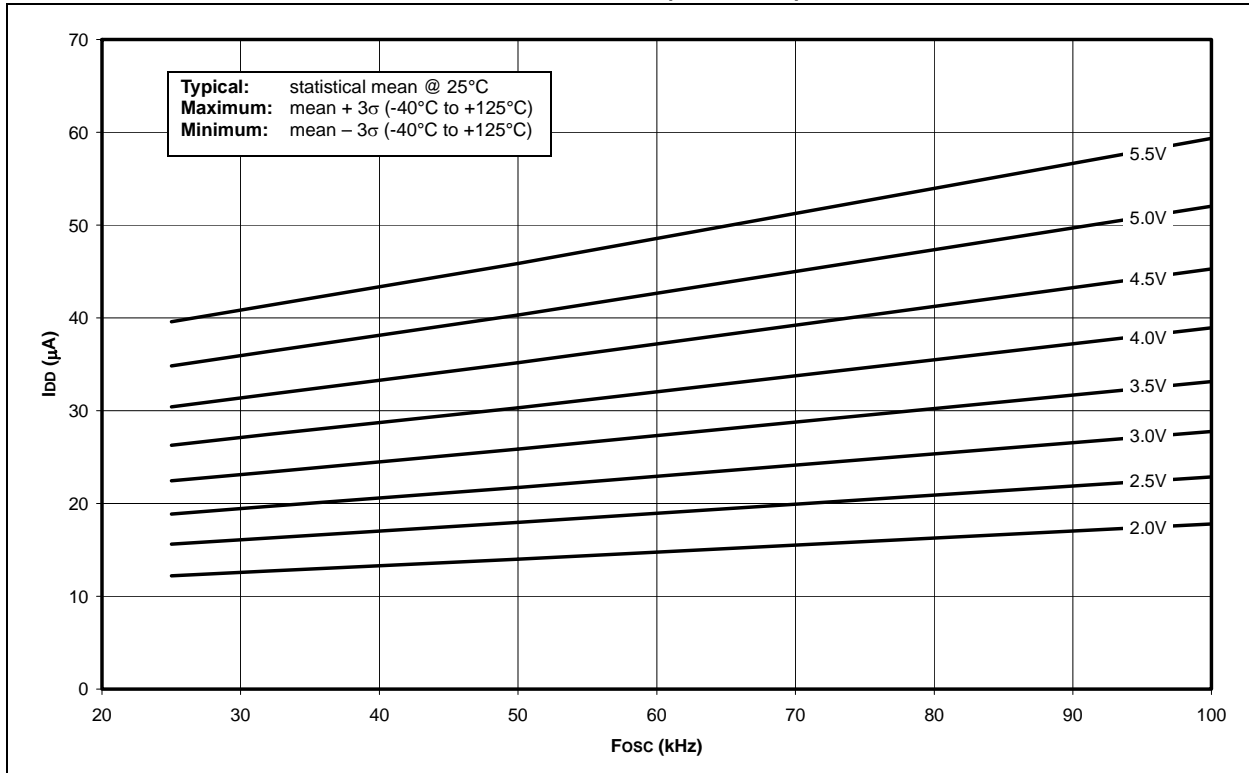
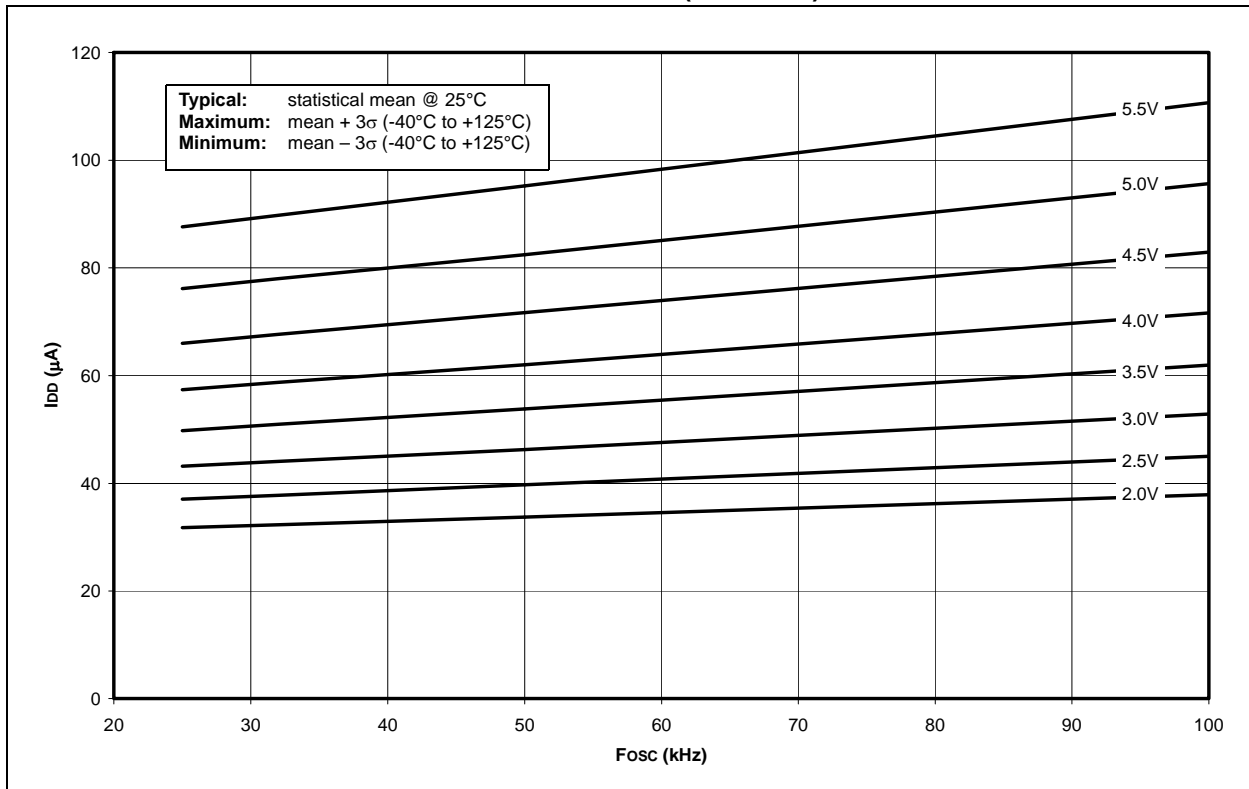


FIGURE 19-6: MAXIMUM I_{DD} vs. F_{osc} OVER V_{DD} (LP MODE)

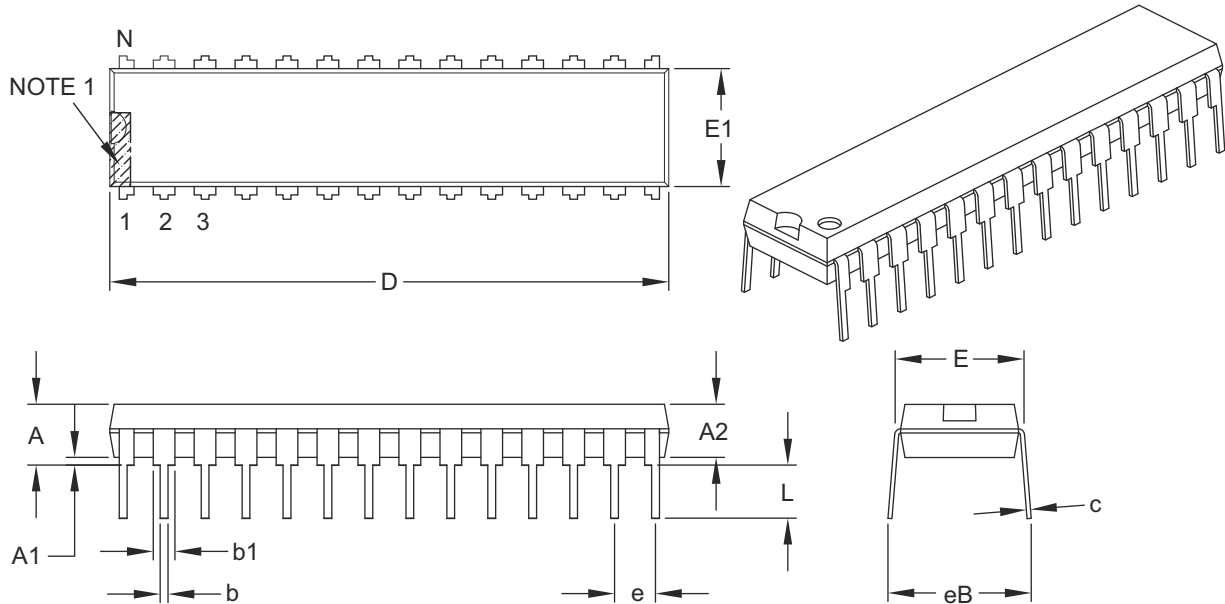


20.2 Package Details

The following sections give the technical details of the packages.

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

INDEX

A

A/D

A/D Converter Interrupt, Configuring	155
Acquisition Requirements	156
ADRESH Register.....	154
Analog Port Pins	68
Analog-to-Digital Converter.....	151
Associated Registers	160
Automatic Acquisition Time.....	157
Calculating Acquisition Time.....	156
Configuring Analog Port Pins.....	158
Configuring the Module.....	155
Conversion Clock.....	157
Conversion Requirements	234
Conversion Status (GO/DONE Bit)	154
Conversions	159
Delays	156
Effects of a Reset.....	160
Internal Sampling Switch (Rss) Impedance	156
Operation During Sleep	160
Operation in Power-Managed Modes	158
Source Impedance.....	156
Time Delays	156
Use of the CCP Trigger.....	160
Absolute Maximum Ratings	205
ACKSTAT	123
ACKSTAT Status Flag	123
ADCON0 Register	
GO/DONE Bit.....	154
Addressable Universal Synchronous Asynchronous Receiver Transmitter. <i>See</i> AUSART	
ADRESL Register	154
Application Notes	
AN546 (Using the Analog-to-Digital (A/D) Converter)	151
AN552 (Implementing Wake-up on Key Stroke)	56
AN556 (Implementing a Table Read)	29
AN607 (Power-up Trouble Shooting).....	173
Assembler	
MPASM Assembler.....	202
AUSART	
Address Detect Enable (ADDEN Bit)	134
Addressable Universal Synchronous Asynchronous Receiver Transmitter.....	133
Asynchronous Receiver	
(9-Bit Mode)	142
Asynchronous Mode	138
Receiver.....	140
Transmitter.....	138
Asynchronous Receive with Address Detect. <i>See</i> Asynchronous Receive (9-bit Mode).	
Asynchronous Reception	
Associated Registers	141, 143
Setup	141
Asynchronous Reception with Address Detect Setup	142
Asynchronous Transmission	
Associated Registers	139
Setup	139
Baud Rate Generator (BRG).....	135
Associated Registers	135
Baud Rate Formula.....	135

Baud Rates, Asynchronous Mode (BRGH = 0).....	136
Baud Rates, Asynchronous Mode (BRGH = 1).....	136
High Baud Rate Select (BRGH Bit)	133
INTRC Baud Rates, Asynchronous Mode (BRGH = 0).....	137
INTRC Baud Rates, Asynchronous Mode (BRGH = 1).....	137
Sampling	135
Clock Source Select (CSRC Bit)	133
Continuous Receive Enable (CREN Bit)	134
Framing Error (FERR Bit)	134
Overrun Error (OERR Bit).....	134
Receive Data, 9th Bit (RX9D Bit).....	134
Receive Enable, 9-Bit (RX9 Bit)	134
Serial Port Enable (SPEN Bit)	133, 134
Single Receive Enable (SREN Bit)	134
Synchronous Master Mode.....	144
Reception	146
Transmission	144
Synchronous Master Reception	
Associated Registers.....	146
Setup	146
Synchronous Master Transmission	
Associated Registers.....	145
Setup	144
Synchronous Slave Mode.....	148
Reception	149
Transmit.....	148
Synchronous Slave Reception	
Associated Registers.....	149
Setup	149
Synchronous Slave Transmission	
Associated Registers.....	148
Setup	148
Transmit Data, 9th Bit (TX9D)	133
Transmit Enable (TXEN Bit)	133
Transmit Enable, 9-Bit (TX9 Bit).....	133
Transmit Shift Register Status (TRMT Bit)	133

B

Banking, Data Memory	15
Baud Rate Generator	119
BF	123
BF Status Flag	123
Block Diagrams	
A/D.....	155
Analog Input Model.....	156, 165
AUSART Receive	140, 142
AUSART Transmit.....	138
Baud Rate Generator	119
Capture Mode Operation	89
Comparator I/O Operating Modes	162
Comparator Output.....	164
Comparator Voltage Reference	168
Compare	89
Fail-Safe Clock Monitor	189
In-Circuit Serial Programming Connections	192
Interrupt Logic.....	184
Low-Voltage Detect (LVD)	175
Low-Voltage Detect (LVD) with External Input	175
Low-Voltage Detect Characteristics	219
MSSP (I ² C Master Mode).....	117

PIC16F7X7

MSSP (I ² C Mode)	102	CCPR1L Register	87
MSSP (SPI Mode).....	93	CCPR2H Register.....	87
On-Chip Reset Circuit	172	CCPR2L Register.....	87
OSC1/CLKI/RA7 Pin	54	CCPR3H Register.....	87
OSC2/CLKO/RA6 Pin	53	CCPR3L Register	87
PIC16F737 and PIC16F767.....	6	CCPxM<3:0> Bits	88
PIC16F747 and PIC16F777	7	CCPxX and CCPxY Bits	88
PORTC (Peripheral Output Override)		Clock Sources.....	37
RC<2:0>, RC<7:5> Pins	65	Selection Using OSCCON Register.....	37
PORTC (Peripheral Output Override)		Clock Switching	37
RC<4:3> Pins.....	65	Modes (table).....	47
PORTD (In I/O Port Mode).....	67	Transition and the Watchdog Timer.....	38
PORTD and PORTE (Parallel Slave Port)	70	Code Examples	
PORTE (In I/O Port Mode).....	68	Call of a Subroutine in Page 1 from Page 0	29
PWM Mode	91	Changing Between Capture Prescalers.....	89
RA0/AN0:RA1/AN1 Pins	50	Changing Prescaler Assignment from WDT	
RA2/AN2/VREF-/CVREF Pin.....	51	to Timer0	76
RA3/AN3/VREF+ Pin.....	50	Flash Program Read.....	32
RA4/T0CKI/C1OUT Pin	51	Implementing a Real-Time Clock Using a	
RA5/AN4/LVDIN/SS-/C2OUT Pin	52	Timer1 Interrupt Service	82
RB0/INT/AN12 Pin	57	Indirect Addressing	30
RB1/AN10 Pin	57	Initializing PORTA.....	49
RB2/AN8 Pin	58	Loading the SSPBUF (SSPSR) Register.....	96
RB3/CCP2/AN9 Pin	59	Reading a 16-bit Free Running Timer	80
RB4/AN11 Pin	60	Saving Status and W Registers in RAM	185
RB5/AN13/CCP3 Pin	61	Writing a 16-bit Free Running Timer.....	80
RB6/PGC Pin	62	Code Protection	169, 192
RB7/PGD Pin	63	Comparator Module	161
Recommended MCLR Circuit	173	Analog Input Connection Considerations	165
System Clock	39	Associated Registers	165
Timer0/WDT Prescaler	73	Configuration	162
Timer1	79	Effects of a Reset	165
Timer2	85	Interrupts	164
Watchdog Timer (WDT)	186	Operation	163
BOR. See Brown-out Reset.		Operation During Sleep	165
BRG. See Baud Rate Generator.		Outputs	163
BRGH Bit.....	135	Reference	163
Brown-out Reset (BOR)	169, 172, 173, 179, 180	External Signal	163
		Internal Signal.....	163
C		Response Time.....	163
C Compilers		Comparator Specifications.....	218
MPLAB C18	202	Comparator Voltage Reference	167
Capture/Compare/PWM (CCP)	87	Associated Registers	168
Capture Mode	89	Computed GOTO.....	29
CCP Pin Configuration.....	89	Configuration Bits	169
Prescaler	89	Conversion Considerations.....	266
Compare Mode	89	Crystal and Ceramic Resonators	33
CCP Pin Configuration.....	90	Customer Change Notification Service	275
Software Interrupt Mode	90	Customer Notification Service	275
Special Event Trigger.....	90	Customer Support.....	275
Special Event Trigger Output.....	90		
Timer1 Mode Selection	90	D	
Interaction of Two CCP Modules	87	Data Memory	15
PWM Mode	91	Bank Select (RP1:RP0 Bits)	15
Duty Cycle.....	91	General Purpose Registers	15
Example Frequencies and Resolutions	92	Map for PIC16F737 and PIC16F767	16
Period.....	91	Map for PIC16F747 and PIC16F777	17
Setup for Operation.....	92	Special Function Registers	18
Registers Associated with Capture, Compare and		DC and AC Characteristics	
Timer1.....	90	Graphs and Tables	235
Registers Associated with PWM and Timer2.....	92	DC Characteristics.....	207, 216
Timer Resources.....	87	Internal RC Accuracy.....	215
CCP1 Module.....	87	Power-Down and Supply Current	208
CCP2 Module.....	87	Development Support	201
CCP3 Module.....	87		
CCPR1H Register	87		

PIC16F7X7

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC³² logo, rPIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MTP, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

Analog-for-the-Digital Age, Application Maestro, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniscent Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICTail, REAL ICE, rLAB, Select Mode, SQL, Serial Quad I/O, Total Endurance, TSHARC, UniWinDriver, WiperLock, ZENA and Z-Scale are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

GestIC and ULPP are registered trademarks of Microchip Technology Germany II GmbH & Co. & KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2003-2013, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.

ISBN: 9781620769386

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949 ==

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.