# Microchip Technology - PIC16LF767-I/SO Datasheet





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#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	10MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf767-i-so

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# **Pin Diagrams (Continued)**



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# PIC16F7X7

Pin Name	PDIP Pin #	QFN Pin #	TQFP Pin #	I/O/P Type	Buffer Type	Description
						PORTD is a bidirectional I/O port or Parallel Slave Port
						when interfacing to a microprocessor bus.
RD0/PSP0	19	38	38		ST/TTL <sup>(3)</sup>	
RD0				1/O		Digital I/O. Derellel Sleve Dert dete
PSP0				1/0	o <del>,</del> (3)	Parallel Slave Port data.
RD1/PSP1	20	39	39	1/0	SI/IIL®	Digital I/O
PSP1				1/O		Parallel Slave Port data.
RD2/PSP2	21	40	40		ST/TTL <sup>(3)</sup>	
RD2				I/O		Digital I/O.
PSP2				I/O		Parallel Slave Port data.
RD3/PSP3	22	41	41		ST/TTL <sup>(3)</sup>	
RD3				I/O		Digital I/O.
PSP3				I/O	(2)	Parallel Slave Port data.
RD4/PSP4	27	2	2	1/0	ST/TTL <sup>(3)</sup>	District VO
RD4 PSP4				1/0		Digital I/O. Parallel Slave Port data
	20	2	2	1/0	ст/тті (3)	
RD5/FSF5	20	3	3	I/O	31/11LY	Digital I/O.
PSP5				I/O		Parallel Slave Port data.
RD6/PSP6	29	4	4		ST/TTL <sup>(3)</sup>	
RD6				I/O		Digital I/O.
PSP6				I/O		Parallel Slave Port data.
RD7/PSP7	30	5	5		ST/TTL <sup>(3)</sup>	
RD7				1/0		Digital I/O. Derellel Sleve Dert dete
P3P7				1/0		
		05	05		o <del></del>	POR I E is a bidirectional I/O port.
REU/RD/AN5	8	25	25	1/0	SI/IIL®	Digital I/O
RD				1/0		Read control for Parallel Slave Port.
AN5				I.		Analog input 5.
RE1/WR/AN6	9	26	26		ST/TTL <sup>(3)</sup>	
RE1				I/O		Digital I/O.
WR				1		Write control for Parallel Slave Port.
AN6				I	(2)	Analog input 6.
RE2/CS/AN7	10	27	27	1/0	ST/TTL(3)	Digital 1/0
$\frac{RE2}{CS}$				1/0		Chip select control for Parallel Slave Port
AN7				i		Analog input 7.
Vss	—	31	_	Р	_	Analog ground reference.
Vss	12, 31	6, 30	6, 29	Р	_	Ground reference for logic and I/O pins.
Vdd	_	8	_	Р		Analog positive supply.
Vdd	11, 32	7, 28	7, 28	Р		Positive supply for logic and I/O pins.
NC	_	13, 29	12, 13, 33, 34	_	_	These pins are not internally connected. These pins should be left unconnected.
Legend: I = input			Itput	+	I/O = inpu ST = Sch	nt/output P = power

# TABLE 1-3: PIC16F747 AND PIC16F777 PINOUT DESCRIPTION (CONTINUED)

**Note 1:** This buffer is a Schmitt Trigger input when configured as an external interrupt.

This buffer is a Schmitt Trigger input when used in Serial Programming mode.
 This buffer is a Schmitt Trigger input when configured as a general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

4: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

5: Pin location of CCP2 is determined by the CCPMX bit in Configuration Word Register 1.

FIGU	RE	2-2:
------	----	------

# DATA MEMORY MAP FOR PIC16F737 AND THE PIC16F767

A	File Address		File Address		File Address	A	File ddre
ndirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180
TMR0	01h	OPTION REG	81h	TMR0	101h	OPTION_REG	181
PCL	02h	PCL	82h	PCL	102h	PCL	182
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183
FSR	04h	FSR	84h	FSR	104h	FSR	184
PORTA	05h	TRISA	85h	WDTCON	105h		185
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186
PORTC	07h	TRISC	87h		107h		187
101110	08h		88h		108h		188
PORTE	09h	TRISE	89h	LVDCON	109h		189
	0Ah	PCLATH	84h	PCLATH	10Ah	PCLATH	184
	0Bh	INTCON	88h	INTCON	10Bh	INTCON	18P
PIR1	0Ch		9Ch	PMDATA	10Ch	PMCON1	180
PIR?	0Dh		804	PMADR	10Dh		180
	0Eh		8Eh		10Fh		190
					10Eh		
	106		001	FINADALI	110h		100
	116		90n		11011		190
	106	SSPCON2	91n				
	1211		92n				
SSPBUF	1.011	SSPADD	93h				
SSPCON	14n	SSPSIAI	94h				
	15N	CCPR3L	95h				
CCPR1H	16h	CCPR3H	96h	General		General	
CCP1CON	1/h	CCP3CON	97h	Purpose		Purpose	
RCSTA	18h	TXSTA	98h	Register		Register	
TXREG	19h	SPBRG	99h	16 Bytes		To Bytes	
RCREG	1Ah		9Ah				
CCPR2L	1Bh	ADCON2	9Bh				
CCPR2H	1Ch	CMCON	9Ch				
CCP2CON	1Dh	CVRCON	9Dh				
ADRESH	1Eh	ADRESL	9Eh				
ADCON0	1Fh	ADCON1	9Fh		11Fh		19F
General Purpose Register	20h	General Purpose Register 80 Bytes	A0h EFh	General Purpose Register 80 Bytes	120h 16Fh	General Purpose Register 80 Bytes	1A0
96 Bytes	756	Accesses 70h-7Fh	FOh	Accesses 70h-7Fh	170h	Accesses 70h-7Fh	1F0
Bank 0	] / ["[]	Bank 1	, F <b>F</b> N	Bank 2	/	Bank 3	
Unimplement	nted data i cal registe	memory locations r.	read as 'o	o'.			

#### 2.2.2.5 PIR1 Register

bit 5

The PIR1 register contains the individual flag bits for the peripheral interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the Global Interrupt Enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt bits are clear prior to enabling an interrupt.

### REGISTER 2-5: PIR1: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 1 (ADDRESS 0Ch)

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit 7		•	•	•	•	•	bit 0

- bit 7 **PSPIF:** Parallel Slave Port Read/Write Interrupt Flag bit<sup>(1)</sup>
  - 1 = A read or a write operation has taken place (must be cleared in software)
  - 0 = No read or write has occurred

Note: PSPIF is reserved on 28-pin devices; always maintain this bit clear.

- bit 6 ADIF: A/D Converter Interrupt Flag bit
  - 1 = An A/D conversion is completed (must be cleared in software)
  - 0 = The A/D conversion is not complete
  - RCIF: AUSART Receive Interrupt Flag bit
    - 1 = The AUSART receive buffer is full
    - 0 = The AUSART receive buffer is empty
- bit 4 **TXIF**: AUSART Transmit Interrupt Flag bit
  - 1 = The AUSART transmit buffer is empty
  - 0 = The AUSART transmit buffer is full
- bit 3 **SSPIF**: Synchronous Serial Port (SSP) Interrupt Flag bit
  - 1 = The SSP interrupt condition has occurred and must be cleared in software before returning from the Interrupt Service Routine. The conditions that will set this bit are: SPI:
    - A transmission/reception has taken place.
    - I<sup>2</sup>C Slave:
    - A transmission/reception has taken place.
    - I<sup>2</sup>C Master:

A transmission/reception has taken place. The initiated Start condition was completed by the SSP module. The initiated Stop condition was completed by the SSP module. The initiated Restart condition was completed by the SSP module. The initiated Acknowledge condition was completed by the SSP module. A Start condition occurred while the SSP module was Idle (multi-master system). A Stop condition occurred while the SSP module was Idle (multi-master system).

- 0 = No SSP interrupt condition has occurred
- bit 2 **CCP1IF**: CCP1 Interrupt Flag bit
  - Capture mode:
    - 1 = A TMR1 register capture occurred (must be cleared in software)
    - 0 = No TMR1 register capture occurred
    - Compare mode:
    - 1 = A TMR1 register compare match occurred (must be cleared in software)
    - 0 = No TMR1 register compare match occurred
    - PWM mode:
    - Unused in this mode.
- bit 1 **TMR2IF**: TMR2 to PR2 Match Interrupt Flag bit
  - 1 = TMR2 to PR2 match occurred (must be cleared in software)
  - 0 = No TMR2 to PR2 match occurred
- bit 0 TMR1IF: TMR1 Overflow Interrupt Flag bit
  - 1 = TMR1 register overflowed (must be cleared in software)
  - 0 = TMR1 register did not overflow

# Legend:R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

# 2.3 PCL and PCLATH

The Program Counter (PC) is 13 bits wide. The low byte comes from the PCL register which is a readable and writable register. The upper bits (PC<12:8>) are not readable but are indirectly writable through the PCLATH register. On any Reset, the upper bits of the PC will be cleared. Figure 2-4 shows the two situations for the loading of the PC. The upper example in the figure shows how the PC is loaded on a write to PCL (PCLATH<4:0>  $\rightarrow$  PCH). The lower example in the figure shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3>  $\rightarrow$  PCH).

#### FIGURE 2-4: LOADING OF PC IN DIFFERENT SITUATIONS



# 2.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to the Application Note, *AN556 "Implementing a Table Read"* (DS00556).

# 2.3.2 STACK

The PIC16F7X7 family has an 8-level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1: There are no Status bits to indicate stack overflow or stack underflow conditions.2: There are no instructions/mnemonics

2: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

# 2.4 Program Memory Paging

PIC16F7X7 devices are capable of addressing a continuous 8K word block of program memory. The CALL and GOTO instructions provide only 11 bits of address to allow branching within any 2K program memory page. When doing a CALL or GOTO instruction, the upper 2 bits of the address are provided by PCLATH<4:3>. When doing a CALL or GOTO instruction, the user must ensure that the page select bits are programmed so that the desired program memory page is addressed. If a return from a CALL instruction (or interrupt) is executed, the entire 13-bit PC is POPed off the stack. Therefore, manipulation of the PCLATH<4:3> bits is not required for the RETURN instructions (which POPs the address from the stack).

Note:	The	contents	of	the	PCLA	ΤН	are				
	uncha	anged afte	r a	RETU	RN or	RET	FIE				
	instruction is executed. The user must set										
	up the PCLATH for any subsequent CALLS										
	or GO	TO <b>S</b> .									

Example 2-1 shows the calling of a subroutine in page 1 of the program memory. This example assumes that PCLATH is saved and restored by the Interrupt Service Routine (if interrupts are used).

### EXAMPLE 2-1: CALL OF A SUBROUTINE IN PAGE 1 FROM PAGE 0

	ORG BCF	0x500 PCLATH, 4	4
	BSF	PCLATH,	3 ;Select page 1 ;(800h-FFFh)
	CALL :	SUB1_P1	;Call subroutine in ;page 1 (800h-FFFh)
SUB1_P1	ORG	0x900	;page 1 (800h-FFFh)
	:		;called subroutine
	:		;page 1 (800h-FFFh)
RETURN	:		;return to Call ;subroutine in page 0 ;(000h-7FFh)

Name	Bit#	Buffer	Function
RA0/AN0	bit 0	TTL	Input/output or analog input.
RA1/AN1	bit 1	TTL	Input/output or analog input.
RA2/AN2/VREF-/CVREF	bit 2	TTL	Input/output or analog input or VREF
RA3/AN3/VREF+	bit 3	TTL	Input/output or analog input or VREF+.
RA4/T0CKI/C1OUT	bit 4	ST	Input/output or external clock input for Timer0. Output is open-drain type.
RA5/AN4/LVDIN/SS/C2OUT	bit 5	TTL	Input/output or slave select input for synchronous serial port or analog input.
OSC2/CLKO/RA6	bit 6	ST	Input/output, connects to crystal or resonator, oscillator output or 1/4 the frequency of OSC1 and denotes the instruction cycle in RC mode.
OSC1/CLKI/RA7	bit 7	ST/CMOS <sup>(1)</sup>	Input/output, connects to crystal or resonator or oscillator input.

### TABLE 5-1: PORTA FUNCTIONS

**Legend:** TTL = TTL input, ST = Schmitt Trigger input

**Note 1:** This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

#### TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
05h	PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xx0x 0000	uu0u 0000
85h	TRISA	PORTA D	PORTA Data Direction Register								1111 1111
9Fh	ADCON1	ADFM	ADCS2	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	0000 0000	0000 0000
9Ch	CMCON	C2OUT	C10UT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0111	0000 0111
9Dh	CVRCON	CVREN	CVROE	CVRR	—	CVR3	CVR2	CVR1	CVR0	000- 0000	000- 0000

Legend: x = unknown, u = unchanged, -- = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

**Note:** When using the SSP module in SPI Slave mode and  $\overline{SS}$  enabled, the A/D converter must be set to one of the following modes, where PCFG2:PCFG0 = 100, 101, 11x.

# PIC16F7X7



FIGURE 5-11: BLOCK DIAGRAM OF RB3/CCP2<sup>(1)</sup>/AN9 PIN

# 6.3 Using Timer0 With an External Clock

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least 2 Tosc (and a small RC delay of 20 ns) and low for at least 2 Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

### 6.4 Prescaler

There is only one prescaler available, which is mutually exclusively shared between the Timer0 module and the Watchdog Timer. A prescaler assignment for the Timer0 module means that the prescaler cannot be used by the Watchdog Timer and vice versa. This prescaler is not readable or writable (see Figure 6-1). Note: Although the prescaler can be assigned to either the WDT or Timer0, but not both, a new divide counter is implemented in the WDT circuit to give multiple WDT time-out selections. This allows TMR0 and WDT to each have their own scaler. Refer to Section 15.17 "Watchdog Timer (WDT)" for further details.

The PSA and PS2:PS0 bits (OPTION\_REG<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, x....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

Note:	Writing to TMR0 when the prescaler is
	assigned to Timer0 will clear the prescaler
	count but will not change the prescaler
	assignment.

The CCPR1H register and a 2-bit internal latch are used to double-buffer the PWM duty cycle. This double-buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2, concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

The maximum PWM resolution (bits) for a given PWM frequency is given by the formula:

### **EQUATION 9-3:**



**Note:** If the PWM duty cycle value is longer than the PWM period, the CCP1 pin will not be cleared.

# 9.6.3 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

- 1. Set the PWM period by writing to the PR2 register.
- 2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
- Make the CCP1 pin an output by clearing the TRISC<2> bit.
- 4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
- 5. Configure the CCP1 module for PWM operation.

### TABLE 9-4:EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 20 MHz)

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

#### TABLE 9-5: REGISTERS ASSOCIATED WITH PWM AND TIMER2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTOIE	RBIE	TMR0IF	INTOIF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	OSFIF	CMIF	LVDIF	_	BCLIF		CCP3IF	CCP2IF	000- 0-00	000- 0-00
8Ch	PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh	PIE2	OSFIE	CMIE	LVDIE	—	BCLIE		CCP3IE	CCP2IE	000- 0-00	000- 0-00
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
11h	TMR2	Timer2 Module Register								0000 0000	0000 0000
92h	PR2	Timer2 Period Register								1111 1111	1111 1111
12h	T2CON		TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/C	Capture/Compare/PWM Register 1 (LSB)								
16h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)									
17h	CCP1CON		—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
1Bh	CCPR2L	Capture/Compare/PWM Register 2 (LSB)									
1Ch	CCPR2H	Capture/Compare/PWM Register 2 (MSB)									
1Dh	CCP2CON		—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	00 0000
95h	CCPR3L	Capture/Compare/PWM Register 3 (LSB)						xxxx xxxx	uuuu uuuu		
96h	CCPR3H	Capture/Compare/PWM Register 3 (MSB)						xxxx xxxx	uuuu uuuu		
97h	CCP3CON	—	—	CCP3X	CCP3Y	CCP3M3	CCP3M2	CCP3M1	CCP3M0	00 0000	00 0000
Legend:	x = unknown $u = unknown = unknown = unknown = unknown = 0$ , Shaded cells are not used by PWM and Timer2										

**Note 1:** Bits PSPIE and PSPIF are reserved on the PIC16F737/767 devices; always maintain these bits clear.

# 10.3.6 SLAVE MODE

In Slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched, the SSPIF interrupt flag bit is set.

While in Slave mode, the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times, as specified in the electrical specifications.

While in Sleep mode, the slave can transmit/receive data. When a byte is received, the device will wake-up from Sleep.

Before enabling the module in SPI Slave mode, the clock line must match the proper Idle state. The clock line can be observed by reading the SCK pin. The Idle state is determined by the CKP bit (SSPCON1<4>).

# 10.3.7 SLAVE SELECT SYNCHRONIZATION

The  $\overline{SS}$  pin allows a Synchronous Slave mode. The SPI must be in Slave mode with  $\overline{SS}$  pin control enabled (SSPCON<3:0> = 4h). The pin must not be driven low for the  $\overline{SS}$  pin to function as an input. The data latch

must be high. When the  $\overline{SS}$  pin is low, transmission and reception are enabled and the SDO pin is driven. When the  $\overline{SS}$  pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte and becomes a floating output. External pull-up/pull-down resistors may be desirable, depending on the application.

- Note 1: When the SPI is in Slave mode with  $\overline{SS}$  pin control enabled (SSPCON<3:0> = 0100), the SPI module will reset if the  $\overline{SS}$  pin is set to VDD.
  - 2: If the SPI is used in Slave mode with CKE set, then the SS pin control must be enabled.

When the SPI module resets, the bit counter is forced to '0'. This can be done by either forcing the SS pin to a high level or clearing the SSPEN bit.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver, the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function) since it cannot create a bus conflict.

### FIGURE 10-4: SLAVE SYNCHRONIZATION WAVEFORM



In 10-bit Address mode, two address bytes need to be received by the slave. The five Most Significant bits (MSbs) of the first address byte specify if this is a 10-bit address. Bit R/W (SSPSTAT<2>) must specify a write so the slave device will receive the second address byte. For a 10-bit address, the first byte would equal '11110 A9 A8 0', where 'A9' and 'A8' are the two MSbs of the address. The sequence of events for 10-bit address is as follows, with steps 7 through 9 for the slave-transmitter:

- 1. Receive first (high) byte of address (bits SSPIF, BF and UA (SSPSTAT<1>) are set).
- Update the SSPADD register with second (low) byte of address (clears bit UA and releases the SCL line).
- 3. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
- 4. Receive second (low) byte of address (bits SSPIF, BF and UA are set).
- 5. Update the SSPADD register with the first (high) byte of address. If match releases SCL line, this will clear bit UA.
- 6. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
- 7. Receive Repeated Start condition.
- 8. Receive first (high) byte of address (bits SSPIF and BF are set).
- 9. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.

# 10.4.3.2 Reception

When the  $R/\overline{W}$  bit of the address byte is clear and an address match occurs, the  $R/\overline{W}$  bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register and the SDA line is held low (ACK).

When the address byte overflow condition exists, then the no Acknowledge (ACK) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) is set or bit SSPOV (SSPCON<6>) is set. An MSSP interrupt is generated for each data transfer byte. Flag bit, SSPIF (PIR1<3>), must be cleared in software. The SSPSTAT register is used to determine the status of the byte.

If SEN is enabled (SSPCON<0> = 1), RC3/SCK/SCL will be held low (clock stretch) following each data transfer. The clock must be released by setting bit, CKP (SSPCON<4>). See **Section 10.4.4** "Clock Stretching" for more detail.

# 10.4.3.3 Transmission

When the R/W bit of the incoming address byte is set and an address match occurs, the R/W bit of the SSPSTAT register is set. The received address is loaded into the SSPBUF register. The ACK pulse will be sent on the ninth bit and pin RC3/SCK/SCL is held low regardless of SEN (see **Section 10.4.4 "Clock Stretching"** for more detail). By stretching the clock, the master will be unable to assert another clock pulse until the slave is done preparing the transmit data. The transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then pin RC3/SCK/SCL should be enabled by setting bit CKP (SSPCON<4>). The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time (Figure 10-9).

The ACK pulse from the master-receiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line is high (not ACK), then the data transfer is complete. In this case, when the ACK is latched by the slave, the slave logic is reset (resets SSPSTAT register) and the slave monitors for another occurrence of the Start bit. If the SDA line was low (ACK), the next transmit data must be loaded into the SSPBUF register. Again, pin RC3/SCK/SCL must be enabled by setting bit CKP.

An MSSP interrupt is generated for each data transfer byte. The SSPIF bit must be cleared in software and the SSPSTAT register is used to determine the status of the byte. The SSPIF bit is set on the falling edge of the ninth clock pulse.

# 10.4.9 I<sup>2</sup>C MASTER MODE REPEATED START CONDITION TIMING

A Repeated Start condition occurs when the RSEN bit (SSPCON2<1>) is programmed high and the I<sup>2</sup>C logic module is in the Idle state. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the Baud Rate Generator is loaded with the contents of SSPADD<5:0> and begins counting. The SDA pin is released (brought high) for one Baud Rate Generator count (TBRG). When the Baud Rate Generator times out, if SDA is sampled high, the SCL pin will be deasserted (brought high). When SCL is sampled high, the Baud Rate Generator is reloaded with the contents of SSPADD<6:0> and begins counting. SDA and SCL must be sampled high for one TBRG. This action is then followed by assertion of the SDA pin (SDA = 0) for one TBRG while SCL is high. Following this, the RSEN bit (SSPCON2<1>) will be automatically cleared and the Baud Rate Generator will not be reloaded, leaving the SDA pin held low. As soon as a Start condition is detected on the SDA and SCL pins, the S bit (SSPSTAT<3>) will be set. The SSPIF bit will not be set until the Baud Rate Generator has timed out.

- Note 1: If RSEN is programmed while any other event is in progress, it will not take effect.
  - A bus collision during the Repeated Start condition occurs if:
    - SDA is sampled low when SCL goes from low-to-high.
    - SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data '1'.

Immediately following the SSPIF bit getting set, the user may write the SSPBUF with the 7-bit address in 7-bit mode or the default first address in 10-bit mode. After the first eight bits are transmitted and an ACK is received, the user may then transmit an additional eight bits of address (10-bit mode) or eight bits of data (7-bit mode).

### 10.4.9.1 WCOL Status Flag

If the user writes the SSPBUF when a Repeated Start sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

Note: Because queueing of events is not allowed, writing of the lower 5 bits of SSPCON2 is disabled until the Repeated Start condition is complete.

# FIGURE 10-20: REPEATED START CONDITION WAVEFORM



# 15.15 Interrupts

The PIC16F7X7 has up to 17 sources of interrupt. The Interrupt Control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

Note:	Individual interrupt flag bits are set regard-
	less of the status of their corresponding
	mask bit or the GIE bit.

A Global Interrupt Enable bit, GIE (INTCON<7>), enables (if set) all unmasked interrupts or disables (if cleared) all interrupts. When bit GIE is enabled and an interrupt's flag bit and mask bit are set, the interrupt will vector immediately. Individual interrupts can be disabled through their corresponding enable bits in various registers. Individual interrupt bits are set regardless of the status of the GIE bit. The GIE bit is cleared on Reset.

The "return from interrupt" instruction, RETFIE, exits the interrupt routine as well as sets the GIE bit which re-enables interrupts.

The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register. The peripheral interrupt flags are contained in the Special Function Register, PIR1. The corresponding interrupt enable bits are contained in Special Function Register, PIE1 and the peripheral interrupt enable bit is contained in Special Function Register, INTCON.

When an interrupt is serviced, the GIE bit is cleared to disable any further interrupt, the return address is pushed onto the stack and the PC is loaded with 0004h. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

For external interrupt events, such as the INT pin or PORTB change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends on when the interrupt event occurs relative to the current Q cycle. The latency is the same for one or two-cycle instructions. Individual interrupt flag bits are set regardless of the status of their corresponding mask bit, PEIE bit or the GIE bit.



#### FIGURE 15-11: INTERRUPT LOGIC

# 17.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC<sup>®</sup> DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

# 17.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC<sup>®</sup> Flash MCUs and dsPIC<sup>®</sup> Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with incircuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

# 17.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC<sup>®</sup> Flash microcontrollers and dsPIC<sup>®</sup> DSCs with the powerful, yet easyto-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

# 17.10 PICkit 3 In-Circuit Debugger/ Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC<sup>®</sup> and dsPIC<sup>®</sup> Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming<sup>™</sup>.

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

# PIC16F7X7







# 18.2 DC Characteristics: Power-Down and Supply Current PIC16F737/747/767/777 (Industrial, Extended) PIC16LF737/747/767/777 (Industrial) (Continued)

PIC16LF (Indu	Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial							
PIC16F7 (Indu	$\begin{array}{llllllllllllllllllllllllllllllllllll$							
Param No.	Device	Тур	Max	Units	Conditions			
	Supply Current (IDD) <sup>(2,3)</sup>							
	PIC16LF7X7	.950	1.3	mA	-40°C			
			1.2	mA	+25°C	VDD = 3.0V		
		.930	1.2	mA	+85°C		Fosc = 8 MHz	
	All devices	1.8	3.0	mA	-40°C		(RC_RUN mode,	
		1.7	2.8	mA	+25°C	V5_0V	Internal RC Oscillator)	
		1.7	2.8	mA	+85°C	VDD = 3.0V		
	Extended devices	2.0	4.0	mA	+125°C			
	PIC16LF7X7	9	13	μΑ	-10°C			
		9	14	μΑ	+25°C	VDD = 2.0V		
		11	16	μA	+70°C			
	PIC16LF7X7	12	34	μΑ	-10°C		Fosc = 32 kHz	
		12	31	μΑ	+25°C	VDD = 3.0V	(SEC_RUN mode,	
		14	28	μΑ	+70°C		Timer1 as Clock)	
	All devices	20	72	μΑ	-10°C			
			65	μΑ	+25°C	VDD = 5.0V		
		25	59	μA	+70°C			

Legend: Shading of rows is to assist in readability of the table.

**Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;

- MCLR = VDD; WDT enabled/disabled as specified.
- **3:** For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

# TABLE 18-15: A/D CONVERTER CHARACTERISTICS: PIC16F7X7 (INDUSTRIAL, EXTENDED) PIC16LF7X7 (INDUSTRIAL)

No.	Sym	Characteristic		Min	Тур†	Мах	Units	Conditions	
A01	NR	Resolution		_	—	10 bits	bit	$\label{eq:VREF} \begin{array}{l} VREF = VDD = 5.12V,\\ VSS \leq VAIN \leq VREF \end{array}$	
A03	EIL	Integral Linearity Error		_	—	<±1	LSb	$\begin{array}{l} VREF=VDD=5.12V,\\ VSS\leqVAIN\leqVREF \end{array}$	
A04	Edl	Differential Linearity Error		-	—	<±1	LSb	$\begin{array}{l} VREF=VDD=5.12V,\\ VSS\leqVAIN\leqVREF \end{array}$	
A06	EOFF	Offset Error		-	—	<±2	LSb	$\begin{array}{l} VREF=VDD=5.12V,\\ VSS\leqVAIN\leqVREF \end{array}$	
A07	Egn	Gain Error		_	—	<±1	LSb	$\begin{array}{l} VREF=VDD=5.12V,\\ VSS\leqVAIN\leqVREF \end{array}$	
A10		Monotonicity		—	guaranteed <sup>(3)</sup>	_		$VSS \leq VAIN \leq VREF$	
A20	Vref	Reference Voltage (VREF+ – VREF-)		2.0	—	VDD + 0.3	V		
A21	Vref+	Reference Voltage High		AVDD – 2.5V	—	AVDD + 0.3V	V		
A22	Vref-	Reference Voltage Low		AVss - 0.3V	—	VREF+ - 2.0V	V		
A25	VAIN	Analog Input Voltage		Vss – 0.3V	—	VREF + 0.3V	V		
A30	ZAIN	Recommended Impedance of Analog Voltage Source		_	—	2.5	kΩ	(Note 4)	
A40	IAD	A/D Conversion	PIC16F7X7	—	220	_	μΑ	Average current	
		Current (VDD)	PIC16LF7X7	_	90		μΑ	consumption when A/D is on (Note 1)	
A50	IREF	VREF Input Current (Note 2)		_	_	5	μΑ	During VAIN acquisition. Based on differential of VHOLD to VAIN to charge CHOLD, see Section 12.1 "A/D Acquisition Requirements". During A/D conversion cycle	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** When A/D is off, it will not consume any current other than minor leakage current. The power-down current specification includes any such leakage from the A/D module.

2: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

3: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

4: Maximum allowed impedance for analog voltage source is 10 kΩ. This requires higher acquisition time.

# PIC16F7X7





# FIGURE 19-4: MAXIMUM IDD vs. Fosc OVER VDD (XT MODE)



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