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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	10MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf767-i-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Name	PDIP Pin #	QFN Pin #	TQFP Pin #	I/O/P Type	Buffer Type	Description
						PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT/AN12 RB0 INT AN12	33	9	8	I/O I I	TTL/ST ⁽¹⁾	Digital I/O. External interrupt. Analog input channel 12.
RB1/AN10 RB1 AN10	34	10	9	I/O I	TTL	Digital I/O. Analog input channel 10.
RB2/AN8 RB2 AN8	35	11	10	I/O I	TTL	Digital I/O. Analog input channel 8.
RB3/CCP2/AN9 RB3 CCP2 ⁽⁵⁾ AN9	36	12	11	I/O I/O I	TTL	Digital I/O. CCP2 capture input, compare output, PWM output. Analog input channel 9.
RB4/AN11 RB4 AN11	37	14	14	I/O I	TTL	Digital I/O. Analog input channel 11
RB5/AN13/CCP3 RB5 AN13 CCP3	38	15	15	I/O I I	TTL	Digital I/O. Analog input channel 13. CCP3 capture input, compare output, PWM output.
RB6/PGC RB6 PGC	39	16	16	I/O I/O	TTL/ST ⁽²⁾	Digital I/O. In-Circuit Debugger and ICSP™ programming clock.
RB7/PGD RB7 PGD	40	17	17	I/O I/O	TTL/ST ⁽²⁾	Digital I/O. In-Circuit Debugger and ICSP programming data.
Legend: I = input — = Not used		O = ou TTL =	tput TTL inpu	t	I/O = inpu ST = Sch	nt/output P = power mitt Trigger input

TABLE 1-3: PIC16F747 AND PIC16F777 PINOUT DESCRIPTION (CONTINUED)

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: This buffer is a Schmitt Trigger input when configured as a general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

4: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

5: Pin location of CCP2 is determined by the CCPMX bit in Configuration Word Register 1.

2.2.2.1 Status Register

The Status register contains the arithmetic status of the ALU, the Reset status and the bank select bits for data memory.

The Status register can be the destination for any instruction, as with any other register. If the Status register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable, therefore, the result of an instruction with the Status register as destination may be different than intended.

For example, CLRF STATUS, will clear the upper three bits and set the Z bit. This leaves the Status register as $000u \ uluu$ (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the Status register because these instructions do not affect the Z, C or DC bits from the Status register. For other instructions not affecting any Status bits, see Section 16.0 "Instruction Set Summary".

Note 1: The <u>C</u> and <u>DC</u> bits operate as a borrow and digit borrow bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

REGISTER 2-1: STATUS: ARITHMETIC STATUS REGISTER (ADDRESS 03h, 83h, 103h, 183h)

11/00-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x						
IRP	RP1	RP0	TO	PD	Z	DC	С						
bit 7							bit 0						
IRP: Regis	ter Bank Sele	ct bit (used f	or indirect ac	ddressing)									
0 = Bank 0	, 1 (00h-FFh)	,											
RP1:RP0:	P1:RP0: Register Bank Select bits (used for direct addressing)												
11 = Bank 10 = Bank 01 = Bank 00 = Bank Each bank	3 (180h-1FFr 2 (100h-17Fh 1 (80h-FFh) 0 (00h-7Fh) is 128 bytes.	ı))											
TO: Time-c	out bit												
1 = After p 0 = A WDT	ower-up, CLR	WDT instructio	ON OF SLEEP	instruction									
PD: Power	-Down bit												
1 = After p 0 = By exe	ower-up or by cution of the s	the CLRWDT	instruction ction										
Z: Zero bit	bit												
1 = The re: 0 = The re:	sult of an arith sult of an arith	imetic or logi imetic or logi	c operation is c operation is	s zero s not zero									
DC: Digit C	C: Digit Carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)												
1 = A carry 0 = No car	v-out from the ry-out from the	4th low-orde e 4th low-ord	r bit of the re er bit of the i	esult occurre result	ed								
C: Carry/bo	orrow bit (ADD	WF, ADDLW	, SUBLW, S	SUBWF instr	uctions)								
1 = A carry 0 = No car	 A carry-out from the Most Significant bit of the result occurred No carry-out from the Most Significant bit of the result occurred 												
Note:	For borrow, two's comple	the polarity	is reversed second oper	. A subtract and. For rot	ction is exe ate (RRF,	ecuted by RLF) instru	adding the ictions, this						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

4.0 OSCILLATOR CONFIGURATIONS

4.1 Oscillator Types

The PIC16F7X7 can be operated in eight different oscillator modes. The user can program three configuration bits (FOSC2:FOSC0) to select one of these eight modes (modes 5-8 are new PIC16 oscillator configurations):

- 1. LP Low-Power Crystal
- 2. XT Crystal/Resonator
- 3. HS High-Speed Crystal/Resonator
- 4. RC External Resistor/Capacitor with FOSC/4 output on RA6
- 5. RCIO External Resistor/Capacitor with I/O on RA6
- 6. INTIO1 Internal Oscillator with Fosc/4 output on RA6 and I/O on RA7
- 7. INTIO2 Internal Oscillator with I/O on RA6 and RA7
- 8. ECIO External Clock with I/O on RA6

4.2 Crystal Oscillator/Ceramic Resonators

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKI and OSC2/CLKO pins to establish oscillation (see Figure 4-1 and Figure 4-2). The PIC16F7X7 oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturer's specifications.

FIGURE 4-1: CRYSTAL OPERATION (HS, XT OR LP OSC CONFIGURATION)



TABLE 4-1:CAPACITOR SELECTION FOR
CRYSTAL OSCILLATOR (FOR
DESIGN GUIDANCE ONLY)

Osc Type	Crystal	Typical Capacitor Values Tested:				
	Fieq	Typical Capacity C1 33 pF 15 pF 56 pF 15 pF	C2			
LP	32 kHz	33 pF	33 pF			
	200 kHz	15 pF	15 pF			
XT	200 kHz	56 pF	56 pF			
	1 MHz	15 pF	15 pF			
	4 MHz	15 pF	15 pF			
HS	4 MHz	15 pF	15 pF			
	8 MHz	15 pF	15 pF			
	20 MHz	15 pF	15 pF			

Capacitor values are for design guidance only.

These capacitors were tested with the crystals listed below for basic start-up and operation. These values were not optimized.

Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application.

See the notes following this table for additional information.

- Note 1: Higher capacitance increases the stability of oscillator but also increases the start-up time.
 - 2: Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.
 - **3:** Rs may be required in HS mode, as well as XT mode, to avoid overdriving crystals with low drive level specification.
 - **4:** Always verify oscillator performance over the VDD and temperature range that is expected for the application.

4.7.2 SEC_RUN MODE

The core and peripherals can be configured to be clocked by T1OSC using a 32.768 kHz crystal. The crystal must be connected to the T1OSO and T1OSI pins. This is the same configuration as the low-power timer circuit (see **Section 7.6** "**Timer1 Oscillator**"). When SCS bits are configured to run from T1OSC, a clock transition is generated. It will clear the OSTS bit, switch the system clock from either the primary system clock or INTRC, depending on the value of SCS<1:0> and FOSC<2:0>, to the external low-power Timer1 oscillator input (T1OSC) and shut-down the primary system clock to conserve power.

After a clock switch has been executed, the internal Q clocks are held in the Q1 state until eight falling edge clocks are counted on the T1OSC. After the eight clock periods have transpired, the clock input to the Q clocks is released and operation resumes (see Figure 4-8). In addition, T1RUN (in T1CON) is set to indicate that T1OSC is being used as the system clock.

Note 1: The T1OSCEN bit must be enabled and it is the user's responsibility to ensure T1OSC is stable before clock switching to the T1OSC input clock can occur.

2: When T1OSCEN = 0, the following possible effects result.

Original SCS<1:0>	Modified SCS<1:0>	Final SCS<1:0>							
00	01	00 – no change							
00	11	10 - INTRC							
10	11	10 - no change							
10	01	00 – Oscillator defined by FOSC<2:0>							

A clock switching event will occur if the final state of the SCS bits is different from the original.



FIGURE 4-8: TIMING DIAGRAM FOR SWITCHING TO SEC_RUN MODE

6.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- · Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Additional information on the Timer0 module is available in the "PIC[®] Mid-Range MCU Family Reference Manual" (DS33023).

Figure 6-1 is a block diagram of the Timer0 module and the prescaler shared with the WDT.

6.1 Timer0 Operation

Timer0 operation is controlled through the OPTION_REG register (see Register 2-2). Timer mode is selected by clearing bit TOCS (OPTION_REG<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting bit, T0CS (OPTION_REG<5>). In Counter mode, Timer0 will increment, either on every rising or falling edge of pin RA4/T0CKI/C1OUT. The incrementing edge is determined by the Timer0 Source Edge Select bit, T0SE (OPTION_REG<4>). Clearing bit T0SE selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.3 "Using Timer0 With an External Clock".

The prescaler is mutually, exclusively shared between the Timer0 module and the Watchdog Timer. The prescaler is not readable or writable. **Section 6.4** "**Prescaler**" details the operation of the prescaler.

6.2 Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets bit TMR0IF (INTCON<2>). The interrupt can be masked by clearing bit TMR0IE (INTCON<5>). Bit TMR0IF must be cleared in software by the Timer0 module Interrupt Service Routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from Sleep since the timer is shut-off during Sleep.





10.4.14 SLEEP OPERATION

While in Sleep mode, the I^2C module can receive addresses or data and when an address match or complete byte transfer occurs, wake the processor from Sleep (if the MSSP interrupt is enabled).

10.4.15 EFFECT OF A RESET

A Reset disables the MSSP module and terminates the current transfer.

10.4.16 MULTI-MASTER MODE

In Multi-Master mode, the interrupt generation on the detection of the Start and Stop conditions allows the determination of when the bus is free. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I^2C bus may be taken when the P bit (SSPSTAT<4>) is set or the bus is Idle, with both the S and P bits clear. When the bus is busy, enabling the SSP interrupt will generate the interrupt when the Stop condition occurs.

In multi-master operation, the SDA line must be monitored for arbitration to see if the signal level is at the expected output level. This check is performed in hardware with the result placed in the BCLIF bit.

The states where arbitration can be lost are:

- Address Transfer
- Data Transfer
- A Start Condition
- A Repeated Start Condition
- An Acknowledge Condition

10.4.17 MULTI-MASTER COMMUNICATION, BUS COLLISION AND BUS ARBITRATION

Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDA pin, arbitration takes place when the master outputs a '1' on SDA by letting SDA float high and another master asserts a '0'. When the SCL pin floats high, data should be stable. If the expected data on SDA is a '1' and the data sampled on the SDA pin = 0, then a bus collision has taken place. The master will set the Bus Collision Interrupt Flag, BCLIF and reset the I^2C port to its Idle state (Figure 10-25).

If a transmit was in progress when the bus collision occurred, the transmission is halted, the BF flag is cleared, the SDA and SCL lines are deasserted and the SSPBUF can be written to. When the user services the bus collision Interrupt Service Routine and if the I^2C bus is free, the user can resume communication by asserting a Start condition.

If a Start, Repeated Start, Stop or Acknowledge condition was in progress when the bus collision occurred, the condition is aborted, the SDA and SCL lines are deasserted and the respective control bits in the SSPCON2 register are cleared. When the user services the bus collision Interrupt Service Routine and if the I^2C bus is free, the user can resume communication by asserting a Start condition.

The master will continue to monitor the SDA and SCL pins. If a Stop condition occurs, the SSPIF bit will be set.

A write to the SSPBUF will start the transmission of data at the first data bit, regardless of where the transmitter left off when the bus collision occurred.

In Multi-Master mode, the interrupt generation on the detection of Start and Stop conditions allows the determination of when the bus is free. Control of the I^2C bus can be taken when the P bit is set in the SSPSTAT register or the bus is Idle and the S and P bits are cleared.

FIGURE 10-25: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE



Baud	Fosc = 8 MHz			Fosc = 4 MHz			Fosc = 2 MHz			Fosc = 1 MHz		
Rate (K)	Kbaud	% Error	SPBRG Value (decimal)									
0.3	NA	_		0.300	0	207	0.300	0	103	0.300	0	51
1.2	1.202	+0.16	103	1.202	+0.16	51	1.202	+0.16	25	1.202	+0.16	12
2.4	2.404	+0.16	51	2.404	+0.16	25	2.404	+0.16	12	2.232	-6.99	6
9.6	9.615	+0.16	12	8.929	-6.99	6	10.417	+8.51	2	NA	_	_
19.2	17.857	-6.99	6	20.833	+8.51	2	NA	_	_	NA	_	_
28.8	31.250	+8.51	3	31.250	+8.51	1	31.250	+8.51	0	NA	_	_
38.4	41.667	+8.51	2	NA	_	_	NA	_	_	NA	_	_
57.6	62.500	+8.51	1	62.500	8.51	0	NA	_	_	NA	_	_

TABLE 11-5: INTRC BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 0)

TABLE 11-6: INTRC BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 1)

Baud Rate (K)	Fosc = 8 MHz			Fosc = 4 MHz			Fosc = 2 MHz			Fosc = 1 MHz		
	Kbaud	% Error	SPBRG Value (decimal)									
0.3	NA	_	_	NA	_	_	NA	_	_	0.300	0	207
1.2	NA	_	_	1.202	+0.16	207	1.202	+0.16	103	1.202	+0.16	51
2.4	2.404	+0.16	207	2.404	+0.16	103	2.404	+0.16	51	2.404	+0.16	25
9.6	9.615	+0.16	51	9.615	+0.16	25	9.615	+0.16	12	8.929	-6.99	6
19.2	19.231	+0.16	25	19.231	+0.16	12	17.857	-6.99	6	20.833	+8.51	2
28.8	29.412	+2.12	16	27.778	-3.55	8	31.250	+8.51	3	31.250	+8.51	1
38.4	38.462	+0.16	12	35.714	-6.99	6	41.667	+8.51	2	NA	_	_
57.6	55.556	-3.55	8	62.500	+8.51	3	62.500	+8.51	1	62.500	+8.51	0

When setting up an Asynchronous Transmission, follow these steps:

- Initialize the SPBRG register for the appropriate baud rate. If a high-speed baud rate is desired, set bit BRGH (see Section 11.1 "AUSART Baud Rate Generator (BRG)").
- 2. Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
- 3. If interrupts are desired, then set enable bit TXIE.
- 4. If 9-bit transmission is desired, then set transmit bit TX9.

- 5. Enable the transmission by setting bit TXEN which will also set bit TXIF.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- 7. Load data to the TXREG register (starts transmission).
- 8. If using interrupts, ensure that GIE and PEIE (bits 7 and 6) of the INTCON register are set.

FIGURE 11-2: ASYNCHRONOUS MASTER TRANSMISSION







TABLE 11-7: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INTOIF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	x000 0000
19h	TXREG	AUSART '	Transmit	Data Regi	ister					0000 0000	0000 0000
8Ch	PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate	Baud Rate Generator Register								0000 0000

Legend: x = unknown, — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous transmission.
 Note 1: Bits PSPIE and PSPIF are reserved on 28-pin devices; always maintain these bits clear.

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REGISTER 12-3:	ADCON2:	ADCON2: A/D CONTROL REGISTER 2 (ADDRESS 9Bh)									
	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0			
			ACQT2	ACQT1	ACQT0	_	_				
	bit 7							bit 0			

bit 7-6 Unimplemented: Read as '0'

bit 5-3 ACQT<2:0>: A/D Acquisition Time Select bits

 $000 = 0^{(1)}$ 001 = 2 TAD 010 = 4 TAD011 = 6 TAD 100 = 8 TAD 101 = **12T**AD 110 = 16 TAD 111 = 20 TAD

> Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.



Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

The analog reference voltage is software selectable to either the device's positive and negative supply voltage (VDD and VSS) or the voltage level on the RA3/AN3/VREF+ and RA2/AN2/VREF-/CVREF pins.

The A/D converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the converter which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D converter can be configured as an analog input or as a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH/ADRESL registers, the GO/DONE bit (ADCON0 register) is cleared and A/D Interrupt Flag bit, ADIF, is set. The block diagram of the A/D module is shown in Figure 12-1.

14.0 COMPARATOR VOLTAGE **REFERENCE MODULE**

The comparator voltage reference generator is a 16-tap resistor ladder network that provides a fixed voltage reference when the comparators are in mode '110'. A programmable register controls the function of the reference generator. Register 14-1 lists the bit functions of the CVRCON register.

As shown in Figure 14-1, the resistor ladder is segmented to provide two ranges of CVREF values and has a power-down function to conserve power when the reference is not being used. The comparator reference supply voltage (also referred to as CVRSRC) comes directly from VDD. It should be noted, however, that the voltage at the top of the ladder is CVRSRC - VSAT, where VSAT is the saturation voltage of the power switch transistor. This reference will only be as accurate as the values of CVRSRC and VSAT.

The output of the reference generator may be connected to the RA2/AN2/VREF-/CVREF pin. This can be used as a simple D/A function by the user if a very high-impedance load is used. The primary purpose of this function is to provide a test path for testing the reference generator function.

REGISTER 14-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER (ADDRESS 9Dh)

	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0					
	CVREN	CVROE	CVRR		CVR3	CVR2	CVR1	CVR0					
	bit 7							bit 0					
bit 7	CVREN : C	CVREN: Comparator Voltage Reference Enable bit											
	1 = CVREF 0 = CVREF	circuit powe circuit powe	red on red down										
bit 6	CVROE: C 1 = CVREF	omparator V voltage leve	REF Output	Enable bit n RA2/AN2/	VREF-/CVRE	F pin							
	0 = CVREF voltage level is disconnected from RA2/AN2/VREF-/CVREF pin												
DIT 5	1 = 0 to 0.6 $0 = 0.25 \text{ C}^{2}$	Mparator VRI 625 CVRSRC, VRSRC to 0.7	er Range S with CVRSF 2 CVRSRC,	election bit RC/24 step s with CVRSR	ize c/32 step siz	ze							
bit 4	Unimplem	ented: Read	l as '0'										
bit 3-0	CVR3:CVF When CVR CVREF = (0 When CVR CVREF = 1/	CVR3:CVR0: Comparator VREF Value Selection bits $0 \le CVR3:CVR0 \le 15$ <u>When CVRR = 1:</u> CVREF = (CVR<3:0>/24) • (CVRSRC) <u>When CVRR = 0:</u> CVREF = 1/4 • (CVRSRC) + (CVR3:CVR0/32) • (CVRSRC)											
	Legend:												
	R = Reada	ble bit	W = W	ritable bit	U = Unim	nplemented	bit, read as '	0'					
	-n = Value	at POR	'1' = B	t is set	'0' = Bit i	s cleared	x = Bit is u	nknown					

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FIGURE 15-7: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD THROUGH PULL-UP RESISTOR)



FIGURE 15-8: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD THROUGH RC NETWORK): CASE 1



FIGURE 15-9: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD THROUGH RC NETWORK): CASE 2





18.2 DC Characteristics: Power-Down and Supply Current PIC16F737/747/767/777 (Industrial, Extended) PIC16LF737/747/767/777 (Industrial)

PIC16LF737/747/767/777 (Industrial)		Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial						
PIC16F737/747/767/777 (Industrial, Extended)		$ \begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for extended} \end{array} $						
Param No.	Тур	Max	Units	Conditions				
	Power-Down Current (IPD)	(1)						
	PIC16LF7X7	0.1	0.4	μΑ	-40°C			
		0.1	0.4	μΑ	+25°C	VDD = 2.0V	VDD = 2.0V	
		0.4	1.5	μΑ	+85°C			
	PIC16LF7X7	0.3	0.5	μΑ	-40°C			
		0.3	0.5	μΑ	+25°C	VDD = 3.0V		
		0.7	1.7	μA	+85°C			
	All devices	0.6	1.0	μA	-40°C			
		0.6	1.0	μΑ	+25°C	Vpp = 5.0V		
		1.2	5.0	μΑ	+85°C	VDD = 0.0V		
	Extended devices	6	28	μΑ	+125°C			

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSs and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

- OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
- MCLR = VDD; WDT enabled/disabled as specified.
- 3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in k Ω .

18.5 Timing Parameter Symbology

The timing parameter symbols have been created using one of the following formats:

1. TppS2ppS		3. Tcc:st	(I ² C specifications only)
2. TppS		4. Ts	(I ² C specifications only)
Т			
F	Frequency	Т	Time
Lowercas	e letters (pp) and their meanings:		
рр			
СС	CCP1	OSC	OSC1
ck	CLKO	rd	RD
CS	CS	rw	RD or WR
di	SDI	SC	SCK
do	SDO	SS	SS
dt	Data in	t0	TOCKI
io	I/O port	t1	T1CKI
mc	MCLR	wr	WR
Uppercas	e letters and their meanings:		
S			
F	Fall	Р	Period
н	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance
I ² C only			
AA	output access	High	High
BUF	Bus free	Low	Low
Tcc:st (I ²	C specifications only)		
CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	Stop condition
STA	Start condition		

FIGURE 18-4: LOAD CONDITIONS



Param No.	Symbol	Characterist	Min	Тур†	Max	Units	Conditions	
70*	TssL2scH, TssL2scL	$\overline{SS} \downarrow$ to SCK \downarrow or SCK \uparrow Inpu	t	Тсү	_	—	ns	
71*	TscH	SCK Input High Time (Slave r	Tcy + 20		_	ns		
72*	TscL	SCK Input Low Time (Slave m	node)	TCY + 20	_	_	ns	
73*	TDIV2SCH, TDIV2SCL	Setup Time of SDI Data Input	100	_	—	ns		
74*	TscH2diL, TscL2diL	Hold Time of SDI Data Input t	DI Data Input to SCK Edge		_	—	ns	
75*	TDOR	SDO Data Output Rise Time	PIC16F7X7 PIC16LF7X7		10 25	25 50	ns ns	
76*	TDOF	SDO Data Output Fall Time		—	10	25	ns	
77*	TssH2doZ	SS ↑ to SDO Output High-Impedance		10	_	50	ns	
78*	TSCR	SCK Output Rise Time (Master mode)	PIC16F7X7 PIC16LF7X7		10 25	25 50	ns ns	
79*	TscF	SCK Output Fall Time (Maste	r mode)	_	10	25	ns	
80*	TscH2doV, TscL2doV	SDO Data Output Valid after SCK Edge	PIC16F7X7 PIC16LF7X7		_	50 145	ns ns	
81*	TDOV2SCH, TDOV2SCL	SDO Data Output Setup to SCK Edge		Тсү	_	_	ns	
82*	TssL2doV	SDO Data Output Valid after $\overline{SS} \downarrow Edge$		_	_	50	ns	
83*	TscH2ssH, TscL2ssH	SS ↑ after SCK Edge		1.5 Tcy + 40	_	—	ns	

TABLE 18-10: SPI MODE REQUIREMENTS

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

I²C[™] BUS START/STOP BITS TIMING FIGURE 18-16:







FIGURE 19-12: AVERAGE FOSC vs. VDD FOR VARIOUS VALUES OF R (RC MODE, C = 100 pF, +25°C)



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28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-052C Sheet 1 of 2

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS			
Dimer	nsion Limits	MIN	NOM	MAX	
Number of Leads	Ν	44			
Lead Pitch	е	0.80 BSC			
Overall Height	А	-	-	1.20	
Molded Package Thickness	A2	0.95	1.00	1.05	
Standoff	A1	0.05 – 0.15			
Foot Length	L	0.45	0.60	0.75	
Footprint	L1	1.00 REF			
Foot Angle	φ	0° 3.5° 7°			
Overall Width	E	12.00 BSC			
Overall Length	D	12.00 BSC			
Molded Package Width	E1	10.00 BSC			
Molded Package Length	D1	10.00 BSC			
Lead Thickness	С	0.09	-	0.20	
Lead Width	b	0.30	0.37	0.45	
Mold Draft Angle Top	α	11° 12° 13°			
Mold Draft Angle Bottom	β	11° 12° 13°			

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Chamfers at corners are optional; size may vary.

3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B

PIC16F7X7

NOTES: