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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	10MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf767t-i-ss

TABLE 1-3: PIC16F747 AND PIC16F777 PINOUT DESCRIPTION (CONTINUED)

Pin Name	PDIP Pin #	QFN Pin #	TQFP Pin #	I/O/P Type	Buffer Type	Description
						PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT/AN12	33	9	8		TTL/ST(1)	
RB0				I/O		Digital I/O.
INT				I		External interrupt.
AN12				I		Analog input channel 12.
RB1/AN10	34	10	9		TTL	
RB1				I/O		Digital I/O.
AN10				I		Analog input channel 10.
RB2/AN8	35	11	10		TTL	
RB2				I/O		Digital I/O.
AN8				I		Analog input channel 8.
RB3/CCP2/AN9	36	12	11		TTL	
RB3				I/O		Digital I/O.
CCP2(5)				I/O		CCP2 capture input, compare output, PWM output.
AN9				I		Analog input channel 9.
RB4/AN11	37	14	14		TTL	
RB4				I/O		Digital I/O.
AN11				I		Analog input channel 11
RB5/AN13/CCP3	38	15	15		TTL	
RB5				I/O		Digital I/O.
AN13				I		Analog input channel 13.
CCP3				I		CCP3 capture input, compare output, PWM output.
RB6/PGC	39	16	16		TTL/ST(2)	
RB6				I/O		Digital I/O.
PGC				I/O		In-Circuit Debugger and ICSP™ programming clock.
RB7/PGD	40	17	17		TTL/ST(2)	
RB7				I/O		Digital I/O.
PGD				I/O		In-Circuit Debugger and ICSP programming data.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured as a general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).
4: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.
5: Pin location of CCP2 is determined by the CCPMX bit in Configuration Word Register 1.

TABLE 1-3: PIC16F747 AND PIC16F777 PINOUT DESCRIPTION (CONTINUED)

Pin Name	PDIP Pin #	QFN Pin #	TQFP Pin #	I/O/P Type	Buffer Type	Description
						PORTC is a bidirectional I/O port.
RC0/T1OSO/T1CKI	15	34	32		ST	
RC0				I/O		Digital I/O.
T1OSO				O		Timer1 oscillator output.
T1CKI				I		Timer1 external clock input.
RC1/T1OSI/CCP2	16	35	35		ST	
RC1				I/O		Digital I/O.
T1OSI				I		Timer1 oscillator input.
CCP2(5)				I/O		Capture 2 input, Compare 2 output, PWM 2 output.
RC2/CCP1	17	36	36		ST	
RC2				I/O		Digital I/O.
CCP1				I/O		Capture 1 input, Compare 1 output, PWM 1 output.
RC3/SCK/SCL	18	37	37		ST	
RC3				I/O		Digital I/O.
SCK				I/O		Synchronous serial clock input/output for SPI mode.
SCL				I/O		Synchronous serial clock input/output for I^2C™ mode.
RC4/SDI/SDA	23	42	42		ST	
RC4				I/O		Digital I/O.
SDI				I		SPI data in.
SDA				I/O		I^2C data I/O.
RC5/SDO	24	43	43		ST	
RC5				I/O		Digital I/O.
SDO				O		SPI data out.
RC6/TX/CK	25	44	44		ST	
RC6				I/O		Digital I/O.
TX				O		AUSART asynchronous transmit.
CK				I/O		AUSART synchronous clock.
RC7/RX/DT	26	1	1		ST	
RC7				I/O		Digital I/O.
RX				I		AUSART asynchronous receive.
DT				I/O		AUSART synchronous data.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: This buffer is a Schmitt Trigger input when configured as a general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).

4: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

5: Pin location of CCP2 is determined by the CCPMX bit in Configuration Word Register 1.

4.6 Clock Sources and Oscillator Switching

The PIC16F7X7 devices include a feature that allows the system clock source to be switched from the main oscillator to an alternate low-frequency clock source. PIC16F7X7 devices offer three alternate clock sources. When enabled, these give additional options for switching to the various power-managed operating modes.

Essentially, there are three clock sources for these devices:

- Primary oscillators
- Secondary oscillators
- Internal oscillator block (INTRC)

The **primary oscillators** include the External Crystal and Resonator modes, the External RC modes, the External Clock mode and the internal oscillator block. The particular mode is defined on POR by the contents of Configuration Word 1. The details of these modes are covered earlier in this chapter.

The **secondary oscillators** are those external sources not connected to the OSC1 or OSC2 pins. These sources may continue to operate even after the controller is placed in a power-managed mode.

PIC16F7X7 devices offer the Timer1 oscillator as a secondary oscillator. This oscillator continues to run when a SLEEP instruction is executed and is often the time base for functions, such as a real-time clock.

Most often, a 32.768 kHz watch crystal is connected between the RC0/T1OSO/T1CKI and RC1/T1OSI/CCP2 pins. Like the LP mode oscillator circuit, loading capacitors are also connected from each pin to ground. The Timer1 oscillator is discussed in greater detail in **Section 7.6 "Timer1 Oscillator"**.

In addition to being a primary clock source, the **internal oscillator block** is available as a power-managed mode clock source. The 31.25 kHz INTRC source is also used as the clock source for several special features, such as the WDT, Fail-Safe Clock Monitor, Power-up Timer and Two-Speed Start-up.

The clock sources for the PIC16F7X7 devices are shown in Figure 4-6. See **Section 7.0 "Timer1 Module"** for further details of the Timer1 oscillator. See **Section 15.1 "Configuration Bits"** for Configuration register details.

4.6.1 OSCCON REGISTER

The OSCCON register (Register 4-2) controls several aspects of the system clock's operation, both in full power operation and in power-managed modes.

The system clock select bits, SCS1:SCS0, select the clock source that is used when the device is operating in power-managed modes. When the bits are cleared (SCS<1:0> = 00), the system clock source comes from the main oscillator that is selected by the FOSC2:FOSC0 configuration bits in Configuration Register 1. When the bits are set in any other manner, the system clock source is provided by the Timer1 oscillator (SCS1:SCS0 = 01) or from the internal oscillator block (SCS1:SCS0 = 10). After a Reset, SCS<1:0> are always set to '00'.

The internal oscillator select bits, IRCF2:IRCF0, select the frequency output of the internal oscillator block that is used to drive the system clock. The choices are the INTRC source (31.25 kHz), the INTOSC source (8 MHz) or one of the six frequencies derived from the INTOSC postscaler (125 kHz to 4 MHz). Changing the configuration of these bits has an immediate change on the multiplexor's frequency output.

The OSTS and IOFS bits indicate the status of the primary oscillator and INTOSC source; these bits are set when their respective oscillators are stable. In particular, OSTS indicates that the Oscillator Start-up Timer has timed out.

4.6.2 CLOCK SWITCHING

Clock switching will occur for the following reasons:

- The FCMEN (CONFIG2<0>) bit is set, the device is running from the primary oscillator and the primary oscillator fails. The clock source will be the internal RC oscillator.
- The FCMEN bit is set, the device is running from the Timer1 oscillator (T1OSC) and T1OSC fails. The clock source will be the internal RC oscillator.
- Following a wake-up due to a Reset or a POR, when the device is configured for Two-Speed Start-up mode, switching will occur between the INTRC and the system clock defined by the FOSC<2:0> bits.
- A wake-up from Sleep occurs due to interrupt or WDT wake-up and Two-Speed Start-up is enabled. If the primary clock is XT, HS or LP, the clock will switch between the INTRC and the primary system clock after 1024 clocks and 8 clocks of the primary oscillator. This is conditional upon the SCS bits being set equal to '00'.
- SCS bits are modified from their original value.
- IRCF bits are modified from their original value.

Note:	Because the SCS bits are cleared on any Reset, no clock switching will occur on a Reset unless the Two-Speed Start-up is enabled and the primary clock is XT, HS or LP. The device will wait for the primary clock to become stable before execution begins (Two-Speed Start-up disabled).

4.7.2 SEC_RUN MODE

The core and peripherals can be configured to be clocked by T1OSC using a 32.768 kHz crystal. The crystal must be connected to the T1OSO and T1OSI pins. This is the same configuration as the low-power timer circuit (see **Section 7.6 "Timer1 Oscillator"**). When SCS bits are configured to run from T1OSC, a clock transition is generated. It will clear the OSTS bit, switch the system clock from either the primary system clock or INTRC, depending on the value of SCS<1:0> and FOSC<2:0>, to the external low-power Timer1 oscillator input (T1OSC) and shut-down the primary system clock to conserve power.

After a clock switch has been executed, the internal Q clocks are held in the Q1 state until eight falling edge clocks are counted on the T1OSC. After the eight clock periods have transpired, the clock input to the Q clocks is released and operation resumes (see Figure 4-8). In addition, T1RUN (in T1CON) is set to indicate that T1OSC is being used as the system clock.

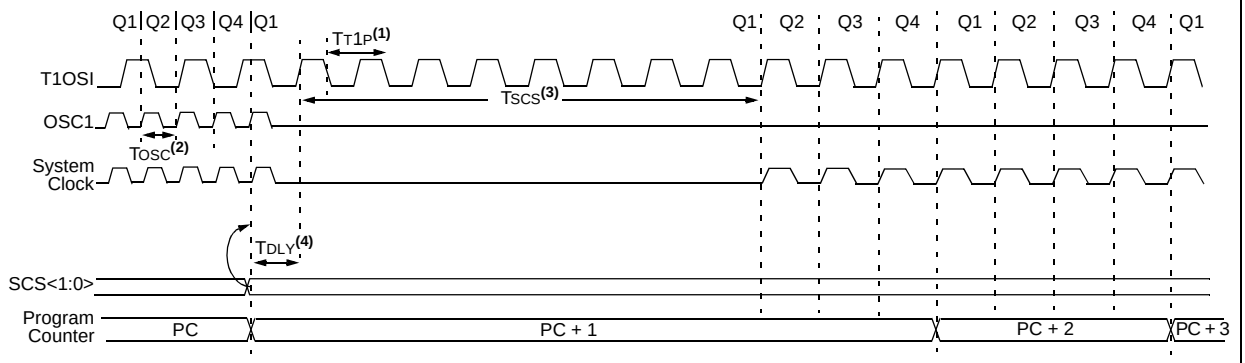
Note 1: The T1OSCEN bit must be enabled and it is the user's responsibility to ensure T1OSC is stable before clock switching to the T1OSC input clock can occur.

2: When T1OSCEN = 0, the following possible effects result.

Original SCS<1:0>	Modified SCS<1:0>	Final SCS<1:0>
00	01	00 – no change
00	11	10 – INTRC
10	11	10 – no change
10	01	00 – Oscillator defined by FOSC<2:0>

A clock switching event will occur if the final state of the SCS bits is different from the original.

FIGURE 4-8: TIMING DIAGRAM FOR SWITCHING TO SEC_RUN MODE



Note 1: TT1P = 30.52 μs.
2: TOSC = 50 ns minimum.
3: TSCS = 8 TT1P
4: TDLY = 1 TT1P.

7.9 Resetting Timer1 Register Pair (TMR1H, TMR1L)

TMR1H and TMR1L registers are not reset to 00h on a POR, or any other Reset, except by the CCP1 special event triggers.

T1CON register is reset to 00h on a Power-on Reset or a Brown-out Reset, which shuts off the timer and leaves a 1:1 prescale. In all other Resets, the register is unaffected.

7.10 Timer1 Prescaler

The prescaler counter is cleared on writes to the TMR1H or TMR1L registers.

7.11 Using Timer1 as a Real-Time Clock

Adding an external LP oscillator to Timer1 (such as the one described in **Section 7.6 "Timer1 Oscillator"**) gives users the option to include RTC functionality in their applications. This is accomplished with an inexpensive watch crystal to provide an accurate time base and several lines of application code to calculate the time. When operating in Sleep mode and using a battery or supercapacitor as a power source, it can completely eliminate the need for a separate RTC device and battery backup.

The application code routine, `RTCisr`, shown in Example 7-3, demonstrates a simple method to increment a counter at one-second intervals using an Interrupt Service Routine. Incrementing the TMR1 register pair to overflow, triggers the interrupt and calls the routine which increments the seconds counter by one; additional counters for minutes and hours are incremented as the previous counter overflows.

Since the register pair is 16 bits wide, counting up to overflow the register directly from a 32.768 kHz clock would take 2 seconds. To force the overflow at the required one-second intervals, it is necessary to preload it. The simplest method is to set the MSb of TMR1H with a `BSF` instruction. Note that the TMR1L register is never preloaded or altered; doing so may introduce cumulative error over many cycles.

For this method to be accurate, Timer1 must operate in Asynchronous mode and the Timer1 overflow interrupt must be enabled (PIE1<0> = `1`) as shown in the routine, `RTCinit`. The Timer1 oscillator must also be enabled and running at all times.

EXAMPLE 7-3: IMPLEMENTING A REAL-TIME CLOCK USING A TIMER1 INTERRUPT SERVICE

```
RTCinit     BANKSEL     TMR1H
            MOVLW       0x80                ; Preload TMR1 register pair
            MOVWF       TMR1H               ; for 1 second overflow
            CLRF        TMR1L
            MOVLW       b'00001111'         ; Configure for external clock,
            MOVWF       T1CON               ; Asynchronous operation, external oscillator
            CLRF        secs                ; Initialize timekeeping registers
            CLRF        mins
            MOVLW       .12
            MOVWF       hours
            BANKSEL     PIE1
            BSF         PIE1, TMR1IE        ; Enable Timer1 interrupt
            RETURN
RTCisr      BANKSEL     TMR1H
            BSF         TMR1H, 7            ; Preload for 1 sec overflow
            BCF         PIR1, TMR1IF        ; Clear interrupt flag
            INCF        secs, F             ; Increment seconds
            MOVF        secs, w
            SUBLW       .60
            BTFSS       STATUS, Z           ; 60 seconds elapsed?
            RETURN                          ; No, done
            CLRF        seconds             ; Clear seconds
            INCF        mins, f             ; Increment minutes
            MOVF        mins, w
            SUBLW       .60
            BTFSS       STATUS, Z           ; 60 seconds elapsed?
            RETURN                          ; No, done
            CLRF        mins                ; Clear minutes
            INCF        hours, f            ; Increment hours
            MOVF        hours, w
            SUBLW       .24
            BTFSS       STATUS, Z           ; 24 hours elapsed?
            RETURN                          ; No, done
            CLRF        hours               ; Clear hours
            RETURN                          ; Done
```

10.3.8 SLEEP OPERATION

In Master mode, all module clocks are halted and the transmission/reception will remain in that state until the device wakes from Sleep. After the device returns to normal mode, the module will continue to transmit/ receive data.

In Slave mode, the SPI Transmit/Receive Shift register operates asynchronously to the device. This allows the device to be placed in Sleep mode and data to be shifted into the SPI Transmit/Receive Shift register. When all 8 bits have been received, the MSSP interrupt flag bit will be set and if enabled, will wake the device from Sleep.

10.3.9 EFFECTS OF A RESET

A Reset disables the MSSP module and terminates the current transfer.

10.3.10 BUS MODE COMPATIBILITY

Table 10-1 shows the compatibility between the standard SPI modes and the states of the CKP and CKE control bits.

TABLE 10-1: SPI BUS MODES

Standard SPI Mode Terminology	Control Bits State	
	CKP	CKE
0, 0	0	1
0, 1	0	0
1, 0	1	1
1, 1	1	0

There is also an SMP bit which controls when the data is sampled.

TABLE 10-2: REGISTERS ASSOCIATED WITH SPI OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
TRISC	PORTC Data Direction Register								1111 1111	1111 1111
SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
TRISA	PORTA Data Direction Register								1111 1111	1111 1111
SSPSTAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, — = unimplemented, read as '0'. Shaded cells are not used by the MSSP in SPI mode.

Note 1: The PSPIF and PSPIE bits are reserved on 28-pin devices; always maintain these bits clear.

10.4 I²C Mode

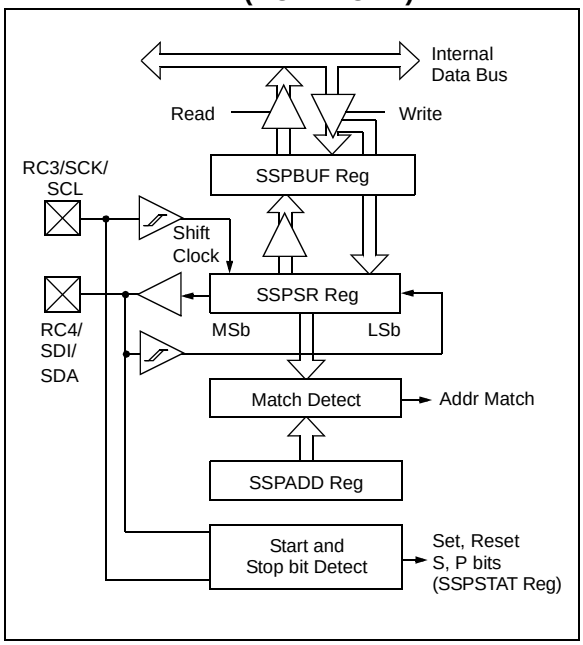
The MSSP module in I²C mode fully implements all master and slave functions (including general call support) and provides interrupts on Start and Stop bits in hardware to determine a free bus (multi-master function). The MSSP module implements the standard mode specifications, as well as 7-bit and 10-bit addressing.

Two pins are used for data transfer:

- Serial clock (SCL) – RC3/SCK/SCL
- Serial data (SDA) – RC4/SDI/SDA

The user must configure these pins as inputs or outputs through the TRISC<4:3> bits.

FIGURE 10-7: MSSP BLOCK DIAGRAM (I²C™ MODE)



10.4.1 REGISTERS

The MSSP module has six registers for I²C operation. These are:

- MSSP Control Register (SSPCON)
- MSSP Control Register 2 (SSPCON2)
- MSSP Status Register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- MSSP Shift Register (SSPSR) – Not directly accessible
- MSSP Address Register (SSPADD)

SSPCON, SSPCON2 and SSPSTAT are the control and status registers in I²C mode operation. The SSPCON and SSPCON2 registers are readable and writable. The lower 6 bits of the SSPSTAT are read-only. The upper two bits of the SSPSTAT are read/write.

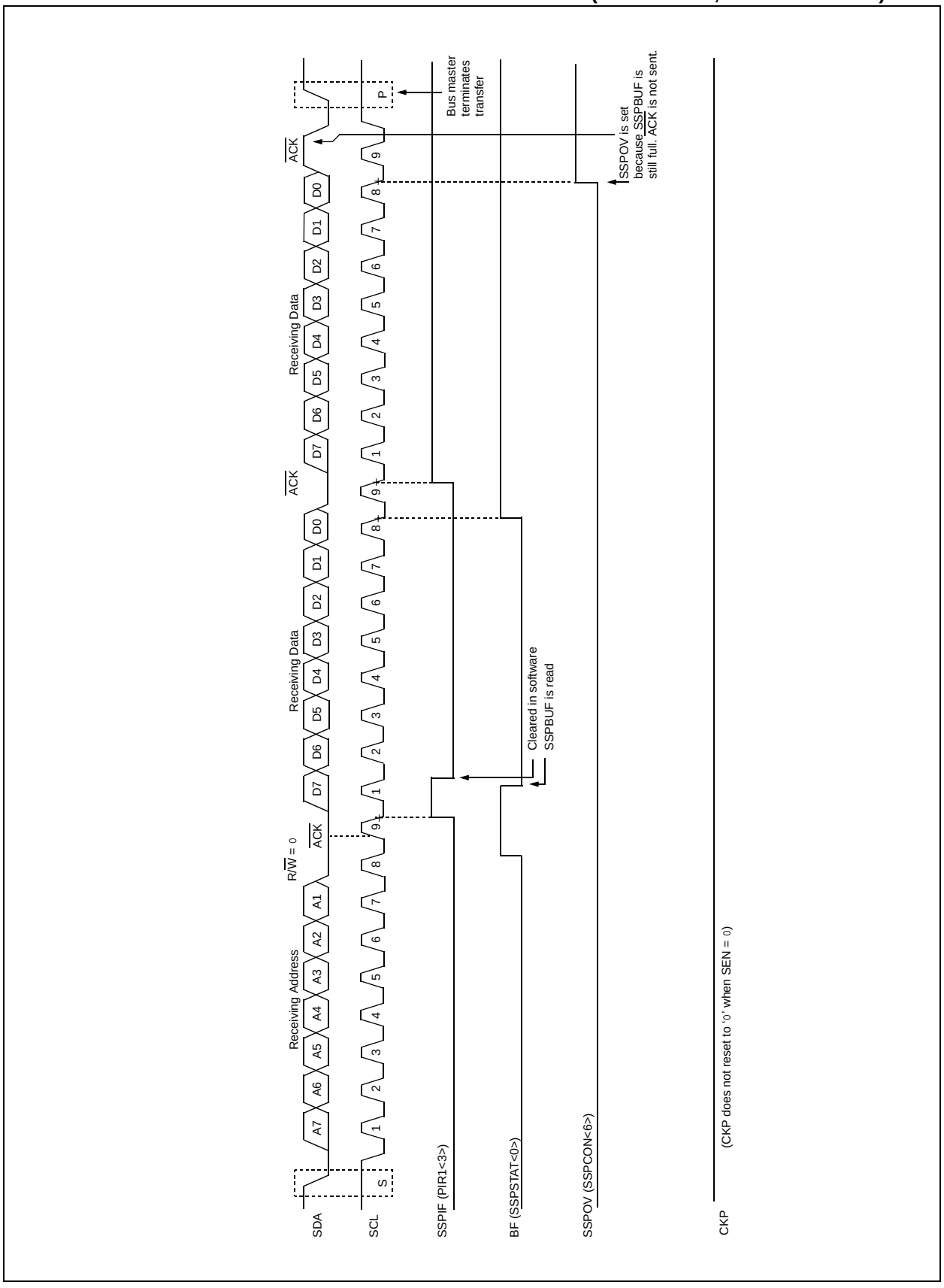
SSPSR is the shift register used for shifting data in or out. SSPBUF is the buffer register to which data bytes are written to or read from.

SSPADD register holds the slave device address when the SSP is configured in I²C Slave mode. When the SSP is configured in Master mode, the lower seven bits of SSPADD act as the Baud Rate Generator reload value.

In receive operations, SSPSR and SSPBUF together create a double-buffered receiver. When SSPSR receives a complete byte, it is transferred to SSPBUF and the SSPIF interrupt is set.

During transmission, the SSPBUF is not double-buffered. A write to SSPBUF will write to both SSPBUF and SSPSR.

FIGURE 10-8: I²C™ SLAVE MODE TIMING WITH SEN = 0 (RECEPTION, 7-BIT ADDRESS)



When setting up an Asynchronous Reception, follow these steps:

1. Initialize the SPBRG register for the appropriate baud rate. If a high-speed baud rate is desired, set bit BRGH (see **Section 11.1 "AUSART Baud Rate Generator (BRG)"**).
2. Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
3. If interrupts are desired, then set enable bit RCIE.
4. If 9-bit reception is desired, then set bit RX9.
5. Enable the reception by setting bit CREN.
6. Flag bit RCIF will be set when reception is complete and an interrupt will be generated if enable bit RCIE is set.
7. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
8. Read the 8-bit received data by reading the RCREG register.
9. If any error occurred, clear the error by clearing enable bit CREN.
10. If using interrupts, ensure that GIE and PEIE (bits 7 and 6) of the INTCON register are set.

TABLE 11-8: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
1Ah	RCREG	AUSART Receive Data Register								0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous reception.

Note 1: Bits PSPIE and PSPIF are reserved on 28-pin devices; always maintain these bits clear.

11.4 AUSART Synchronous Slave Mode

Synchronous Slave mode differs from the Master mode in the fact that the shift clock is supplied externally at the RC6/TX/CK pin (instead of being supplied internally in Master mode). This allows the device to transfer or receive data while in Sleep mode. Slave mode is entered by clearing bit, CSRC (TXSTA<7>).

11.4.1 AUSART SYNCHRONOUS SLAVE TRANSMIT

The operation of the Synchronous Master and Slave modes is identical, except in the case of Sleep mode.

If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

a) The first word will immediately transfer to the TSR register and transmit.
b) The second word will remain in the TXREG register.
c) Flag bit TXIF will not be set.
d) When the first word has been shifted out of TSR, the TXREG register will transfer the second word to the TSR and flag bit TXIF will now be set.
e) If enable bit TXIE is set, the interrupt will wake the chip from Sleep and if the global interrupt is enabled, the program will branch to the interrupt vector (0004h).

When setting up a Synchronous Slave Transmission, follow these steps:

1. Enable the synchronous slave serial port by setting bits SYNC and SPEN and clearing bit CSRC.
2. Clear bits CREN and SREN.
3. If interrupts are desired, then set enable bit TXIE.
4. If 9-bit transmission is desired, then set bit TX9.
5. Enable the transmission by setting enable bit TXEN.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
7. Start transmission by loading data to the TXREG register.
8. If using interrupts, ensure that GIE and PEIE (bits 7 and 6) of the INTCON register are set.

TABLE 11-12: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
19h	TXREG	AUSART Transmit Data Register								0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, — = unimplemented, read as '0'. Shaded cells are not used for synchronous slave transmission.
Note 1: Bits PSPIE and PSPIF are reserved on 28-pin devices; always maintain these bits clear.

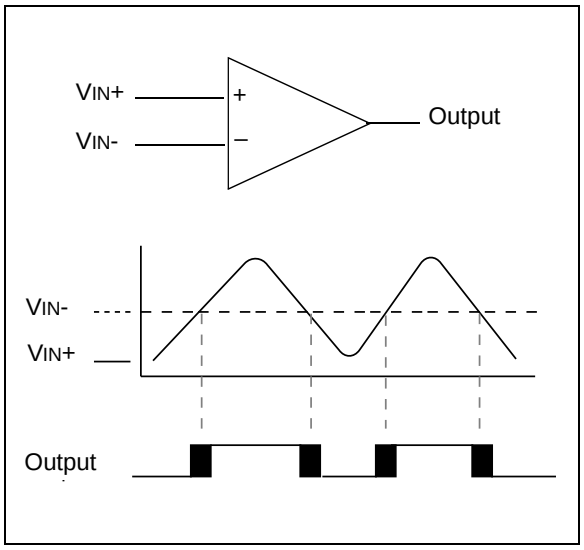
13.2 Comparator Operation

A single comparator is shown in Figure 13-2, along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN-, the output of the comparator is a digital low level. When the analog input at VIN+ is greater than the analog input VIN-, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 13-2 represent the uncertainty due to input offsets and response time.

13.3 Comparator Reference

An external or internal reference signal may be used depending on the comparator operating mode. The analog signal present at VIN- is compared to the signal at VIN+ and the digital output of the comparator is adjusted accordingly (Figure 13-2).

FIGURE 13-2: SINGLE COMPARATOR



13.3.1 EXTERNAL REFERENCE SIGNAL

When external voltage references are used, the comparator module can be configured to have the comparators operate from the same or different reference sources. However, threshold detector applications may require the same reference. The reference signal must be between VSS and VDD and can be applied to either pin of the comparator(s).

13.3.2 INTERNAL REFERENCE SIGNAL

The comparator module also allows the selection of an internally generated voltage reference for the comparators. **Section 14.0 "Comparator Voltage Reference Module"** contains a detailed description of the comparator voltage reference module that provides this signal. The internal reference signal is used when comparators are in mode CM<2:0> = 110 (Figure 13-1). In this mode, the internal voltage reference is applied to the VIN+ pin of both comparators.

13.4 Comparator Response Time

Response time is the minimum time after selecting a new reference voltage, or input source, before the comparator output has a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise, the maximum delay of the comparators should be used (**Section 18.0 "Electrical Characteristics"**).

13.5 Comparator Outputs

The comparator outputs are read through the CMCON register. These bits are read-only. The comparator outputs may also be directly output to the RA4 and RA5 I/O pins. When enabled, multiplexors in the output path of the RA4 and RA5 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 13-3 shows the comparator output block diagram.

The TRISA bits will still function as an output enable/ disable for the RA4 and RA5 pins while in this mode.

The polarity of the comparator outputs can be changed using the C2INV and C1INV bits (CMCON<5:4:>).

Note 1:	When reading the Port register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert an analog input according to the Schmitt Trigger input specification.
2:	Analog levels on any pin defined as a digital input may cause the input buffer to consume more current than is specified.
3:	RA4 is an open collector I/O pin. When used as an output, a pull-up resistor is required.

14.0 COMPARATOR VOLTAGE REFERENCE MODULE

The comparator voltage reference generator is a 16-tap resistor ladder network that provides a fixed voltage reference when the comparators are in mode '110'. A programmable register controls the function of the reference generator. Register 14-1 lists the bit functions of the CVRCON register.

As shown in Figure 14-1, the resistor ladder is segmented to provide two ranges of CV_{REF} values and has a power-down function to conserve power when the reference is not being used. The comparator reference supply voltage (also referred to as CV_{RSRC}) comes directly from V_{DD}. It should be noted, however, that the voltage at the top of the ladder is $CV_{RSRC} - V_{SAT}$, where V_{SAT} is the saturation voltage of the power switch transistor. This reference will only be as accurate as the values of CV_{RSRC} and V_{SAT}.

The output of the reference generator may be connected to the RA2/AN2/V_{REF}-/CV_{REF} pin. This can be used as a simple D/A function by the user if a very high-impedance load is used. The primary purpose of this function is to provide a test path for testing the reference generator function.

REGISTER 14-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER (ADDRESS 9Dh)

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVROE	CVRR	—	CVR3	CVR2	CVR1	CVR0
bit 7							bit 0

bit 7 **CVREN**: Comparator Voltage Reference Enable bit
1 = CV_{REF} circuit powered on
0 = CV_{REF} circuit powered down

bit 6 **CVROE:** Comparator V_{REF} Output Enable bit
1 = CV_{REF} voltage level is output on RA2/AN2/V_{REF}-/CV_{REF} pin
0 = CV_{REF} voltage level is disconnected from RA2/AN2/V_{REF}-/CV_{REF} pin

bit 5 **CVRR**: Comparator V_{REF} Range Selection bit
1 = 0 to 0.625 CV_{RSRC}, with CV_{RSRC}/24 step size
0 = 0.25 CV_{RSRC} to 0.72 CV_{RSRC}, with CV_{RSRC}/32 step size

bit 4 **Unimplemented:** Read as '0'

bit 3-0 **CVR3:CVR0:** Comparator V_{REF} Value Selection bits $0 \le CVR3:CVR0 \le 15$
When CVRR = 1:
$CV_{REF} = (CVR<3:0>/24) \bullet (CV_{RSRC})$
When CVRR = 0:
$CV_{REF} = 1/4 \bullet (CV_{RSRC}) + (CVR3:CVR0/32) \bullet (CV_{RSRC})$

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

FIGURE 14-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

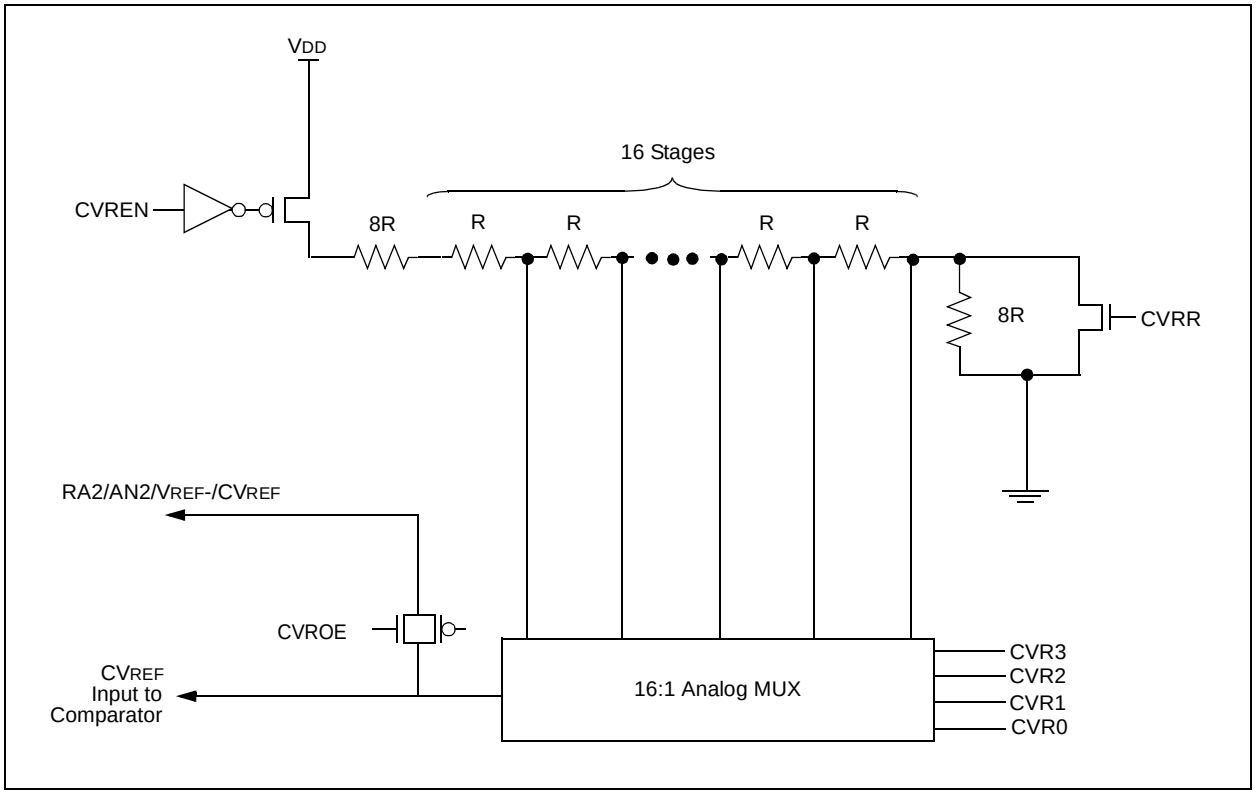


TABLE 14-1: REGISTERS ASSOCIATED WITH COMPARATOR VOLTAGE REFERENCE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on all other Resets
9Dh	CVRCON	CVREN	CVROE	CVRR	—	CVR3	CVR2	CVR1	CVR0	000- 0000	000- 0000
9Ch	CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0111	0000 0111

Legend: x = unknown, u = unchanged, — = unimplemented, read as '0'.
Shaded cells are not used with the comparator voltage reference.

REGISTER 15-1: CONFIGURATION WORD REGISTER 1 (ADDRESS 2007h)

R/P-1	R/P-1	R/P-1	U-1	U-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
CP	CCPMX	DEBUG	—	—	BORV1	BORV0	BOREN	MCLRE	FOSC2	$\overline{\text{PWRTEN}}$	WDTEN	FOSC1	FOSC0
bit 13													bit 0

bit 13 **CP:** Flash Program Memory Code Protection bits
1 = Code protection off
0 = 0000h to 1FFFh code-protected for PIC16F767/777 and 0000h to 0FFFh for PIC16F737/747 (all protected)

bit 12 **CCPMX:** CCP2 Multiplex bit
1 = CCP2 is on RC1
0 = CCP2 is on RB3

bit 11 **DEBUG:** In-Circuit Debugger Mode bit
1 = In-Circuit Debugger disabled, RB6 and RB7 are general purpose I/O pins
0 = In-Circuit Debugger enabled, RB6 and RB7 are dedicated to the debugger

bit 10-9 **Unimplemented:** Read as '1'

bit 8-7 **BORV<1:0>:** Brown-out Reset Voltage bits
11 = V_{BOR} set to 2.0V
10 = V_{BOR} set to 2.7V
01 = V_{BOR} set to 4.2V
00 = V_{BOR} set to 4.5V

bit 6 **BOREN:** Brown-out Reset Enable bit
BOREN combines with BORSEN to control when BOR is enabled and how it is controlled.
BOREN:BORSEN:
11 = BOR enabled and always on
10 = BOR enabled during operation and disabled during Sleep by hardware
01 = BOR controlled by software bit SBOREN – refer to Register 2-8 (PCON<2>)
00 = BOR disabled

bit 5 **MCLRE:** $\overline{\text{MCLR}}$/V_{PP}/RE3 Pin Function Select bit
1 = $\overline{\text{MCLR}}$/V_{PP}/RE3 pin function is $\overline{\text{MCLR}}$
0 = $\overline{\text{MCLR}}$/V_{PP}/RE3 pin function is digital input only, $\overline{\text{MCLR}}$ gated to '1'

bit 3 **$\overline{\text{PWRTEN}}$:** Power-up Timer Enable bit
1 = PWRT disabled
0 = PWRT enabled

bit 2 **WDTEN:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 4, 1-0 **FOSC2:FOSC0:** Oscillator Selection bits
111 = EXTRC oscillator; CLKO function on OSC2/CLKO/RA6
110 = EXTRC oscillator; port I/O function on OSC2/CLKO/RA6
101 = INTRC oscillator; CLKO function on OSC2/CLKO/RA6 and port I/O function on OSC1/CLKI/RA7
100 = INTRC oscillator; port I/O function on OSC1/CLKI/RA7 and OSC2/CLKO/RA6
011 = EXTCLK; port I/O function on OSC2/CLKO/RA6
010 = HS oscillator
001 = XT oscillator
000 = LP oscillator

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

18.2 DC Characteristics: Power-Down and Supply Current PIC16F737/747/767/777 (Industrial, Extended) PIC16LF737/747/767/777 (Industrial) (Continued)

PIC16LF737/747/767/777 (Industrial)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC16F737/747/767/777 (Industrial, Extended)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Module Differential Currents (ΔIWDT, ΔIBOR, ΔILVD, ΔIOSCB, ΔIAD)						
D022 (ΔIWDT)	**Watchdog Timer**	1.5	3.8	µA	-40°C	VDD = 2.0V	
		2.2	3.8	µA	+25°C		
		2.7	4.0	µA	+85°C		
		2.3	4.6	µA	-40°C	VDD = 3.0V	
		2.7	4.6	µA	+25°C		
		3.1	4.8	µA	+85°C		
		3.0	10.0	µA	-40°C	VDD = 5.0V	
		3.3	10.0	µA	+25°C		
		3.9	13.0	µA	+85°C		
	Extended devices	5.0	21.0	µA	+125°C		
D022A (ΔIBOR)	**Brown-out Reset**	17	35	µA	-40°C to +85°C	VDD = 3.0V	
		47	45	µA	-40°C to +85°C	VDD = 5.0V	
		0	0	µA	-40°C to +85°C	VDD = 2.0V VDD = 3.0V VDD = 5.0V	BOREN:BORSEN = 10 in Sleep mode
	Extended devices	48	50	µA	-40°C to +125°C	VDD = 5.0V	
D022B (ΔILVD)	**Low-Voltage Detect**	14	25	µA	-40°C to +85°C	VDD = 2.0V	
		18	35	µA	-40°C to +85°C	VDD = 3.0V	
		21	45	µA	-40°C to +85°C	VDD = 5.0V	
	Extended devices	24	50	µA	-40°C to +125°C	VDD = 5.0V	

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

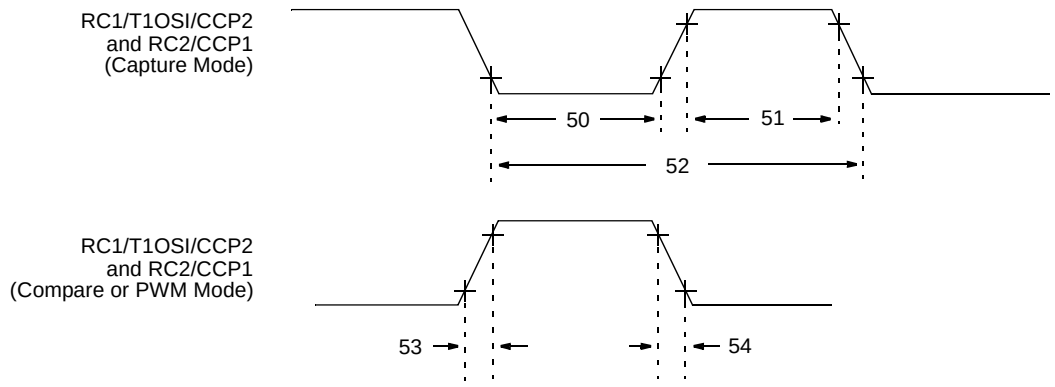
2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

FIGURE 18-10: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)



Note: Refer to Figure 18-4 for load conditions.

TABLE 18-8: CAPTURE/COMPARE/PWM REQUIREMENTS (ALL CCP MODULES)

Param No.	Symbol	Characteristic			Min	Typ†	Max	Units	Conditions
50*	TccL	CCP1, CCP2 and CCP3 Input Low Time	No prescaler		0.5 TCY + 20	—	—	ns	
			With prescaler	PIC16F7X7	10	—	—	ns	
				PIC16LF7X7	20	—	—	ns	
51*	TccH	CCP1, CCP2 and CCP3 Input High Time	No prescaler		0.5 TCY + 20	—	—	ns	
			With prescaler	PIC16F7X7	10	—	—	ns	
				PIC16LF7X7	20	—	—	ns	
52*	TccP	CCP1, CCP2 and CCP3 Input Period			$\frac{3\ T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1, 4 or 16)
53*	TccR	CCP1, CCP2 and CCP3 Output Rise Time		PIC16F7X7	—	10	25	ns	
				PIC16LF7X7	—	25	50	ns	
54*	TccF	CCP1, CCP2 and CCP3 Output Fall Time		PIC16F7X7	—	10	25	ns	
				PIC16LF7X7	—	25	45	ns	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 19-21: TYPICAL, MINIMUM AND MAXIMUM VOL vs. IOL (VDD = 5V, -40°C TO +125°C)

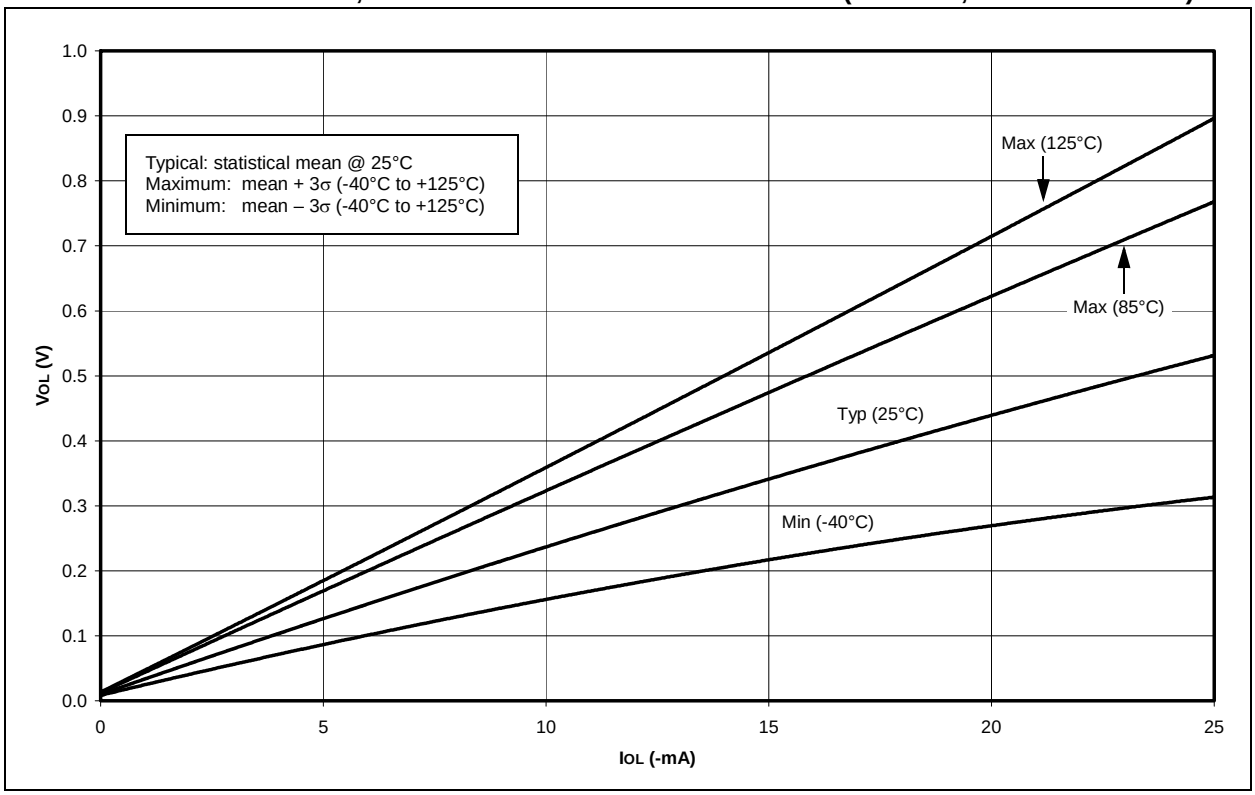
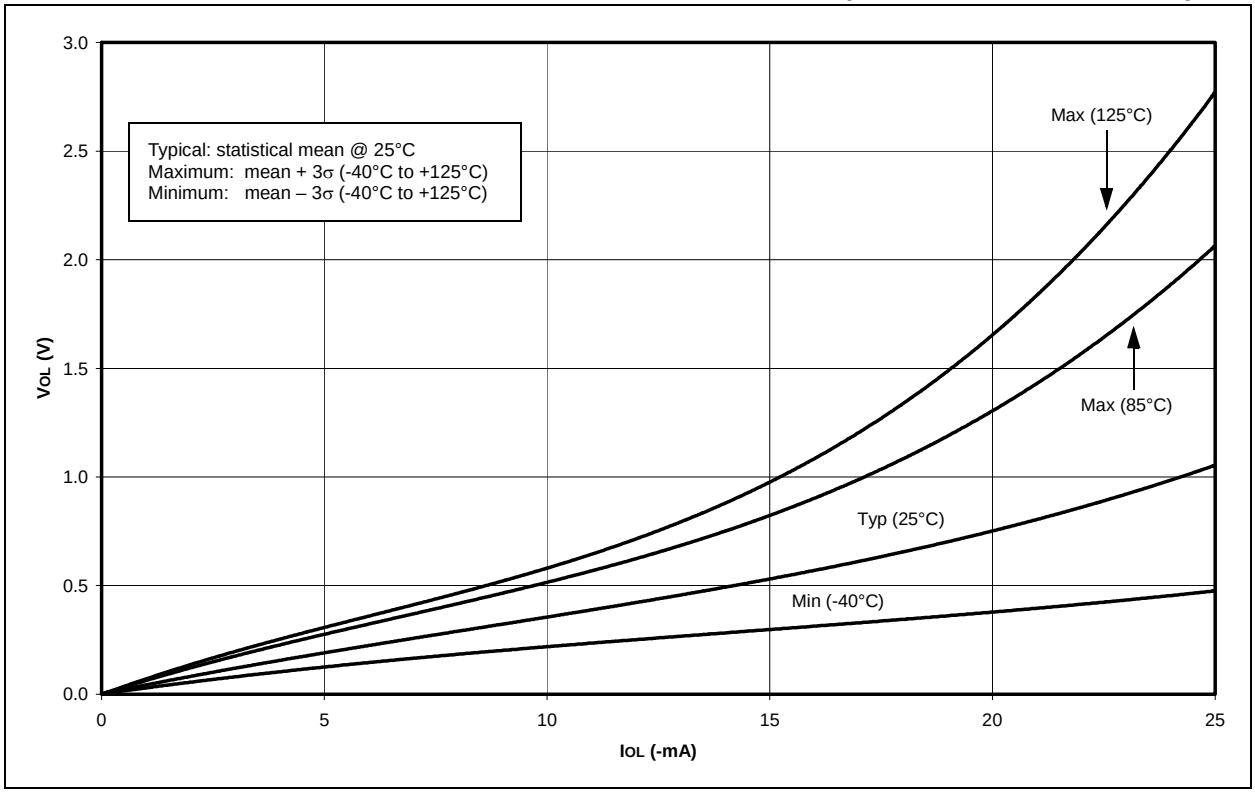
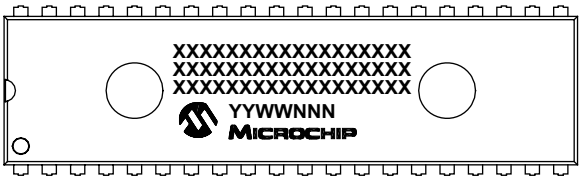


FIGURE 19-22: TYPICAL, MINIMUM AND MAXIMUM VOL vs. IOL (VDD = 3V, -40°C TO +125°C)

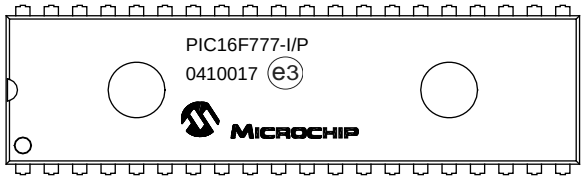


Package Marking Information (Continued)

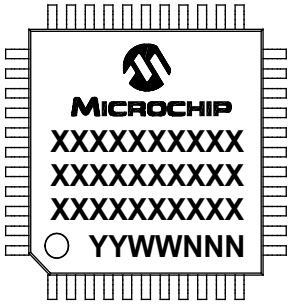
40-Lead PDIP (600 mil)



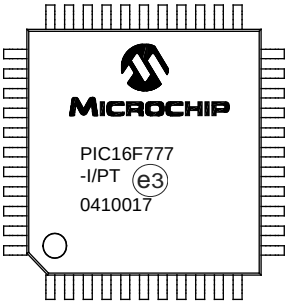
Example



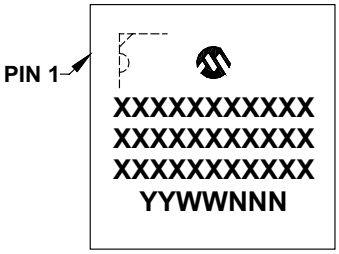
44-Lead TQFP (10x10x1 mm)



Example



44-Lead QFN (8x8x0.9 mm)



Example