



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1827-i-ml

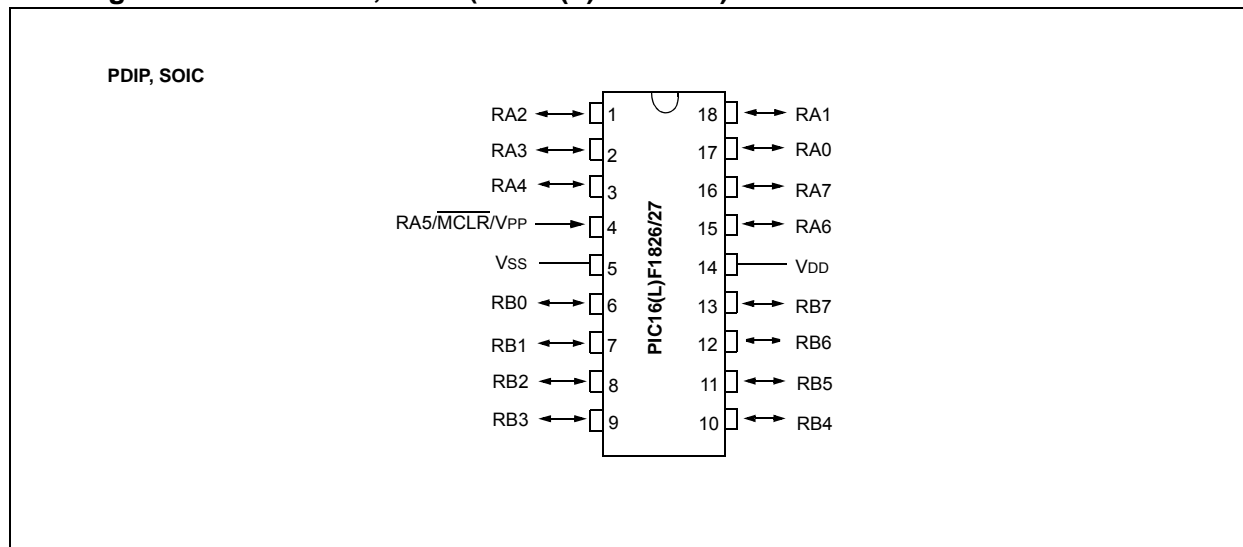
PIC16(L)F1826/27

PIC16(L)F1826/27 Family Types

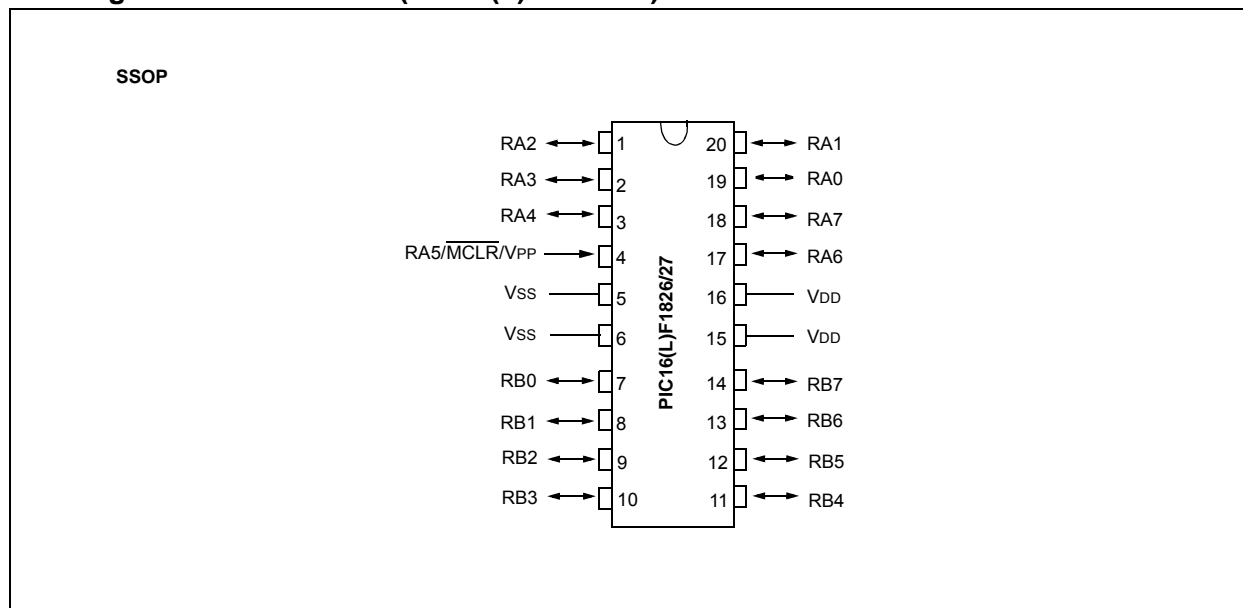
Device	Program Memory	Data Memory		I/O's ⁽¹⁾	10-bit ADC (ch)	CapSense (ch)	Comparators	Timers (8/16-bit)	EUSART	MSSP	ECCP (Full-Bridge)	ECCP (Half-Bridge)	CCP	SR Latch
	Words	SRAM (bytes)	Data EEPROM (bytes)											
PIC16LF1826	2K	256	256	16	12	12	2	2/1	1	1	1	—	—	Yes
PIC16F1826	2K	256	256	16	12	12	2	2/1	1	1	1	—	—	Yes
PIC16LF1827	4K	384	256	16	12	12	2	4/1	1	2	1	1	2	Yes
PIC16F1827	4K	384	256	16	12	12	2	4/1	1	2	1	1	2	Yes

Note 1: One pin is input only.

Pin Diagram – 18-Pin PDIP, SOIC (PIC16(L)F1826/27)



Pin Diagram – 20-Pin SSOP (PIC16(L)F1826/27)



3.2.6 CORE FUNCTION REGISTERS SUMMARY

The Core Function registers listed in Table 3-5 can be addressed from any Bank.

TABLE 3-5: CORE FUNCTION REGISTERS SUMMARY

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 0-31											
x00h or x80h	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
x01h or x81h	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
x02h or x82h	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
x03h or x83h	STATUS	—	—	—	\overline{TO}	\overline{PD}	Z	DC	C	---1 1000	---q quuu
x04h or x84h	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
x05h or x85h	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
x06h or x86h	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
x07h or x87h	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
x08h or x88h	BSR	—	—	—	BSR4	BSR3	BSR2	BSR1	BSR0	---0 0000	---0 0000
x09h or x89h	WREG	Working Register								0000 0000	uuuu uuuu
x0Ah or x8Ah	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
x0Bh or x8Bh	INTCON	GIE	PEIE	TMR0IE	INTE	IOCFE	TMR0IF	INTF	IOCF	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

FIGURE 3-6: ACCESSING THE STACK EXAMPLE 2

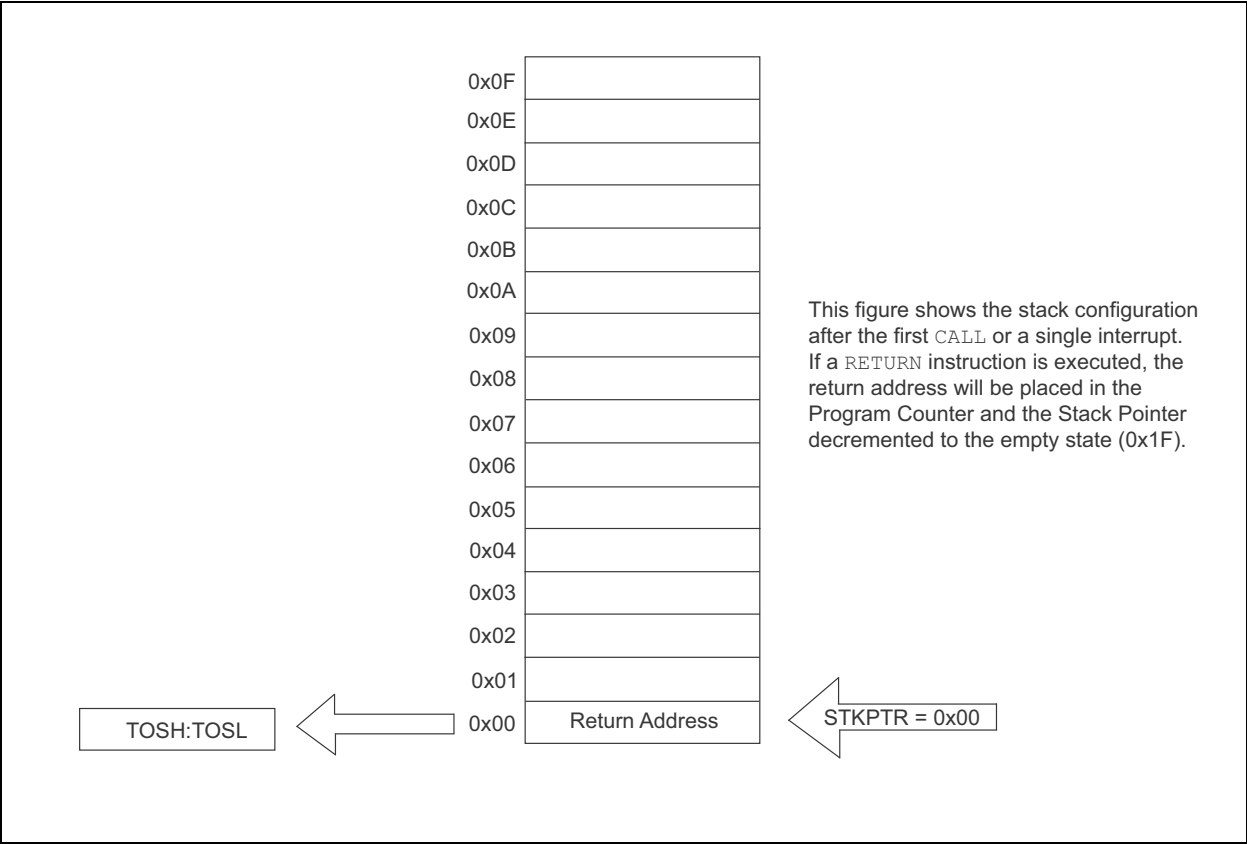
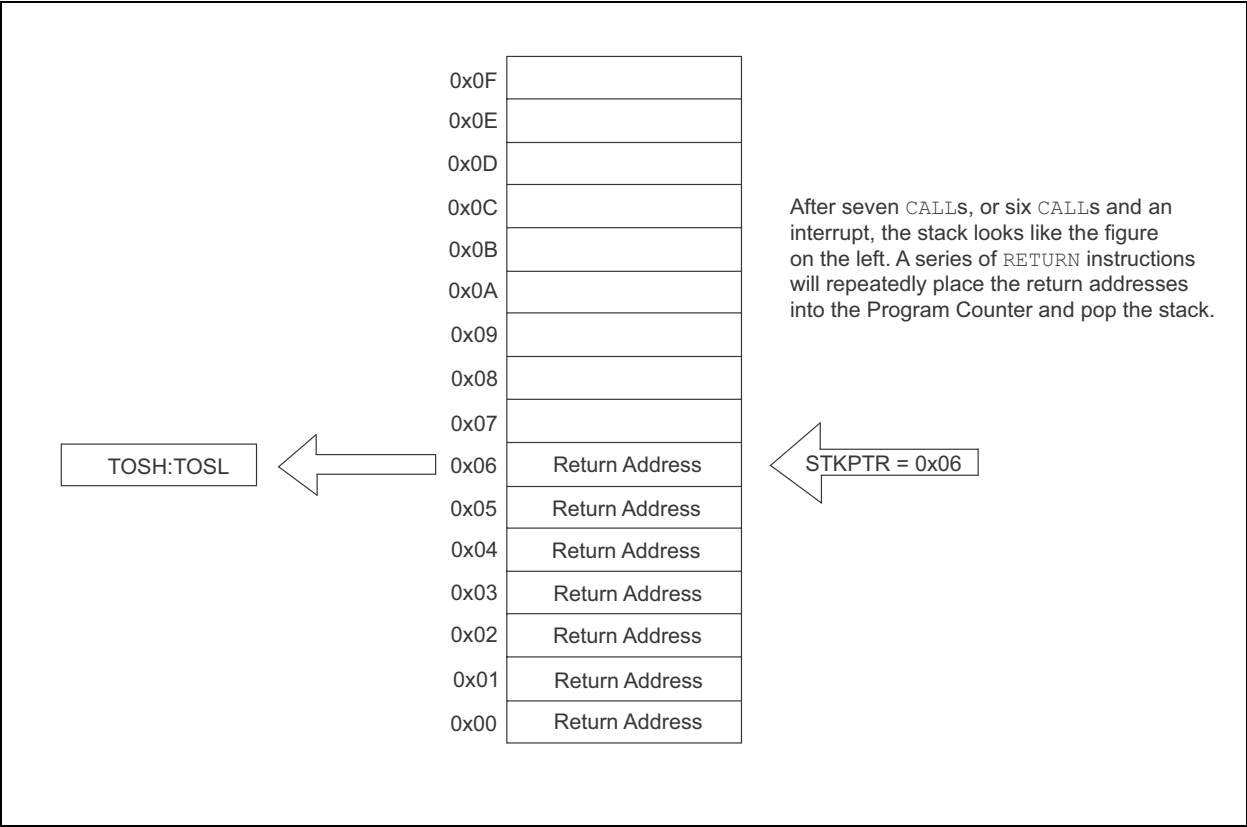


FIGURE 3-7: ACCESSING THE STACK EXAMPLE 3



REGISTER 4-1: CONFIGURATION WORD 1 (CONTINUED)

bit 2-0

FOSC<2:0>: Oscillator Selection bits

111 = ECH: External Clock, High-Power mode (4-20 MHz): device clock supplied to CLKIN pin

110 = ECM: External Clock, Medium-Power mode (0.5-4 MHz): device clock supplied to CLKIN pin

101 = ECL: External Clock, Low-Power mode (0-0.5 MHz): device clock supplied to CLKIN pin

100 = INTOSC oscillator: I/O function on CLKIN pin

011 = EXTRC oscillator: External RC circuit connected to CLKIN pin

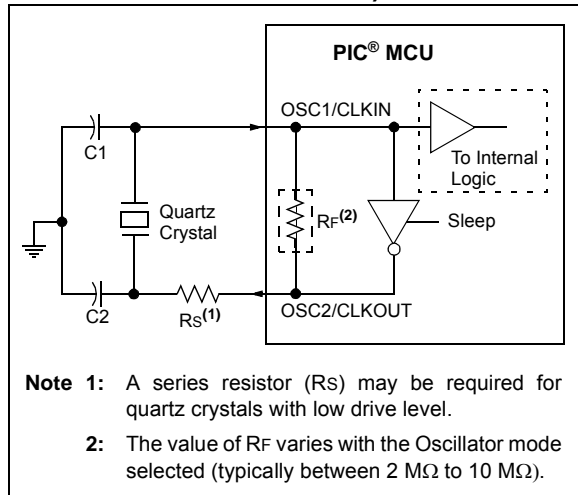
010 = HS oscillator: High-speed crystal/resonator connected between OSC1 and OSC2 pins

001 = XT oscillator: Crystal/resonator connected between OSC1 and OSC2 pins

000 = LP oscillator: Low-power crystal connected between OSC1 and OSC2 pins

PIC16(L)F1826/27

FIGURE 5-3: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)

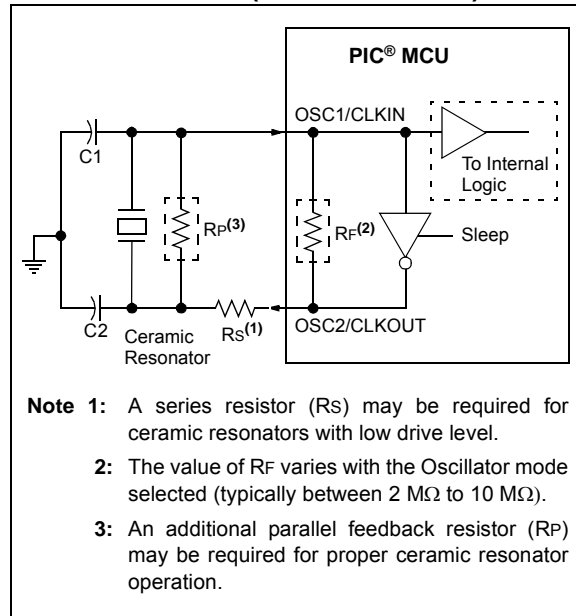


Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

- 2: Always verify oscillator performance over the V_{DD} and temperature range that is expected for the application.
- 3: For oscillator design assistance, reference the following Microchip Applications Notes:

- AN826, "Crystal Oscillator Basics and Crystal Selection for *rPIC*® and *PIC*® Devices" (DS00826)
- AN849, "Basic *PIC*® Oscillator Design" (DS00849)
- AN943, "Practical *PIC*® Oscillator Analysis and Design" (DS00943)
- AN949, "Making Your Oscillator Work" (DS00949)

FIGURE 5-4: CERAMIC RESONATOR OPERATION (XT OR HS MODE)



5.2.1.3 Oscillator Start-up Timer (OST)

If the oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the oscillator module.

In order to minimize latency between external oscillator start-up and code execution, the Two-Speed Clock Start-up mode can be selected (see **Section 5.4 "Two-Speed Clock Start-up Mode"**).

5.2.1.4 4X PLL

The oscillator module contains a 4X PLL that can be used with both external and internal clock sources to provide a system clock source. The input frequency for the 4X PLL must fall within specifications. See the PLL Clock Timing Specifications in **Section 30.0 "Electrical Specifications"**.

The 4X PLL may be enabled for use by one of two methods:

1. Program the PLEN bit in Configuration Word 2 to a '1'.
2. Write the SPLLEN bit in the OSCCON register to a '1'. If the PLEN bit in Configuration Word 2 is programmed to a '1', then the value of SPLLEN is ignored.

5.6 Oscillator Control Registers

REGISTER 5-1: OSCCON: OSCILLATOR CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-1/1	R/W-1/1	R/W-1/1	U-0	R/W-0/0	R/W-0/0
SPLLEN	IRCF<3:0>				—	SCS<1:0>	
bit 7					bit 0		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7

SPLLEN: Software PLL Enable bit

If PLEN in Configuration Word 1 = 1:

SPLLEN bit is ignored. 4x PLL is always enabled (subject to oscillator requirements)

If PLEN in Configuration Word 1 = 0:

1 = 4x PLL is enabled

0 = 4x PLL is disabled

bit 6-3

IRCF<3:0>: Internal Oscillator Frequency Select bits

000x = 31 kHz LF

0010 = 31.25 kHz MF

0011 = 31.25 kHz HF⁽¹⁾

0100 = 62.5 kHz MF

0101 = 125 kHz MF

0110 = 250 kHz MF

0111 = 500 kHz MF (default upon Reset)

1000 = 125 kHz HF⁽¹⁾

1001 = 250 kHz HF⁽¹⁾

1010 = 500 kHz HF⁽¹⁾

1011 = 1 MHz HF

1100 = 2 MHz HF

1101 = 4 MHz HF

1110 = 8 MHz or 32 MHz HF (see **Section 5.2.2.1 "HFINTOSC"**)

1111 = 16 MHz HF

bit 2

Unimplemented: Read as '0'

bit 1-0

SCS<1:0>: System Clock Select bits

1x = Internal oscillator block

01 = Timer1 oscillator

00 = Clock determined by FOSC<2:0> in Configuration Word 1.

Note 1: Duplicate frequency derived from HFINTOSC.

17.0 DIGITAL-TO-ANALOG CONVERTER (DAC) MODULE

The Digital-to-Analog Converter supplies a variable voltage reference, ratiometric with the input source, with 32 selectable output levels.

The input of the DAC can be connected to:

- External VREF pins
- VDD supply voltage
- FVR (Fixed Voltage Reference)

The output of the DAC can be configured to supply a reference voltage to the following:

- Comparator positive input
- ADC input channel
- DACOUT pin
- Capacitive Sensing module (CSM)

The Digital-to-Analog Converter (DAC) can be enabled by setting the DACEN bit of the DACCON0 register.

17.1 Output Voltage Selection

The DAC has 32 voltage level ranges. The 32 levels are set with the DACR<4:0> bits of the DACCON1 register.

The DAC output voltage is determined by the equations in Equation 17-1.

EQUATION 17-1: DAC OUTPUT VOLTAGE

IF DACEN = 1

$$V_{OUT} = \left((V_{SOURCE+} - V_{SOURCE-}) \times \frac{DACR[4:0]}{2^5} \right) + V_{SOURCE-}$$

IF DACEN = 0 and DACLPS = 1 and DACR[4:0] = 1111

$$V_{OUT} = V_{SOURCE+}$$

IF DACEN = 0 and DACLPS = 0 and DACR[4:0] = 0000

$$V_{OUT} = V_{SOURCE-}$$

$V_{SOURCE+} = V_{DD}, V_{REF}, \text{ or } FVR \text{ BUFFER } 2$

$V_{SOURCE-} = V_{SS}$

17.2 Ratiometric Output Level

The DAC output value is derived using a resistor ladder with each end of the ladder tied to a positive and negative voltage reference input source. If the voltage of either input source fluctuates, a similar fluctuation will result in the DAC output value.

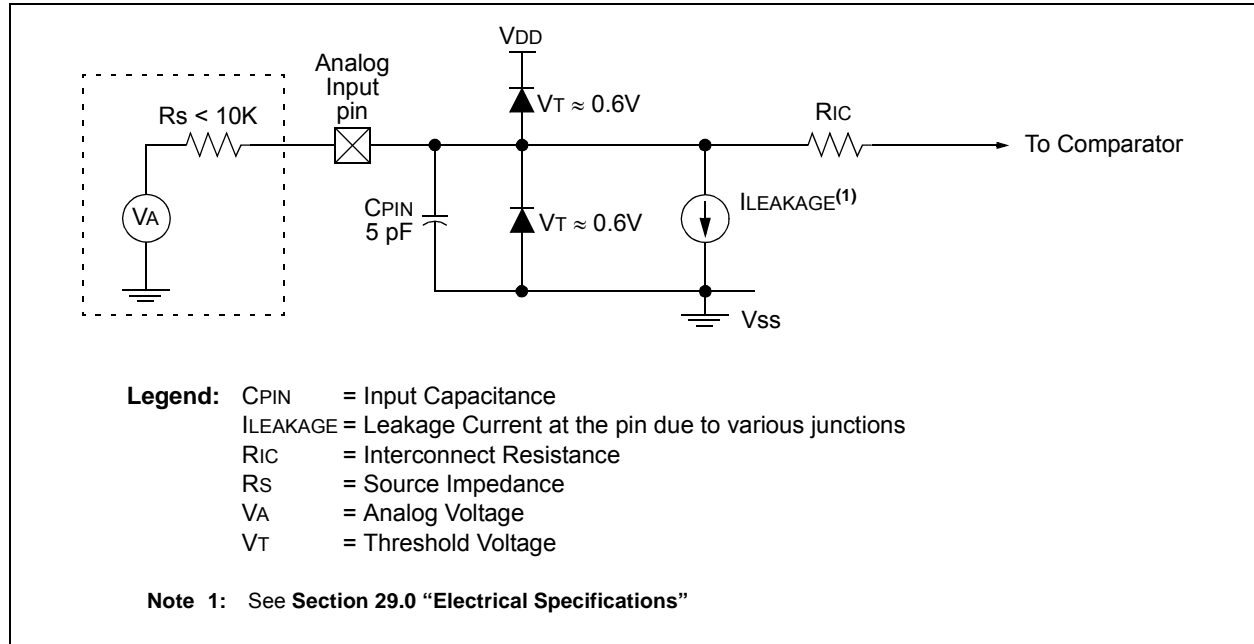
The value of the individual resistors within the ladder can be found in **Section 29.0 “Electrical Specifications”**.

17.3 DAC Voltage Reference Output

The DAC can be output to the DACOUT pin by setting the DACOE bit of the DACCON0 register to ‘1’. Selecting the DAC reference voltage for output on the DACOUT pin automatically overrides the digital output buffer and digital input threshold detector functions of that pin. Reading the DACOUT pin when it has been configured for DAC reference voltage output will always return a ‘0’.

Due to the limited current drive capability, a buffer must be used on the DAC voltage reference output for external connections to DACOUT. Figure 17-2 shows an example buffering technique.

FIGURE 19-4: ANALOG INPUT MODEL



21.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

21.4 Timer1 Oscillator

A dedicated low-power 32.768 kHz oscillator circuit is built-in between pins T1OSI (input) and T1OSO (amplifier output). This internal circuit is to be used in conjunction with an external 32.768 kHz crystal.

The oscillator circuit is enabled by setting the T1OSCEN bit of the T1CON register. The oscillator will continue to run during Sleep.

Note: The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to using Timer1. A suitable delay similar to the OST delay can be implemented in software by clearing the TMR1IF bit then presetting the TMR1H:TMR1L register pair to FC00h. The TMR1IF flag will be set when 1024 clock cycles have elapsed, thereby indicating that the oscillator is running and reasonably stable.

21.5 Timer1 Operation in Asynchronous Counter Mode

If control bit T1SYNC of the T1CON register is set, the external clock input is not synchronized. The timer increments asynchronously to the internal phase clocks. If the external clock source is selected then the timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see **Section 21.5.1 “Reading and Writing Timer1 in Asynchronous Counter Mode”**).

Note: When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce an additional increment.

21.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TMR1L register pair.

21.6 Timer1 Gate

Timer1 can be configured to count freely or the count can be enabled and disabled using Timer1 gate circuitry. This is also referred to as Timer1 gate enable.

Timer1 gate can also be driven by multiple selectable sources.

21.6.1 TIMER1 GATE ENABLE

The Timer1 Gate Enable mode is enabled by setting the TMR1GE bit of the T1GCON register. The polarity of the Timer1 Gate Enable mode is configured using the T1GPOL bit of the T1GCON register.

When Timer1 Gate Enable mode is enabled, Timer1 will increment on the rising edge of the Timer1 clock source. When Timer1 Gate Enable mode is disabled, no incrementing will occur and Timer1 will hold the current count. See Figure 21-3 for timing details.

TABLE 21-3: TIMER1 GATE ENABLE SELECTIONS

T1CLK	T1GPOL	T1G	Timer1 Operation
↑	0	0	Counts
↑	0	1	Holds Count
↑	1	0	Holds Count
↑	1	1	Counts

23.5 Carrier Source Polarity Select

The signal provided from any selected input source for the carrier high and carrier low signals can be inverted. Inverting the signal for the carrier high source is enabled by setting the MDCHPOL bit of the MDCARH register. Inverting the signal for the carrier low source is enabled by setting the MDCLPOL bit of the MDCARL register.

23.6 Carrier Source Pin Disable

Some peripherals assert control over their corresponding output pin when they are enabled. For example, when the CCP1 module is enabled, the output of CCP1 is connected to the CCP1 pin.

This default connection to a pin can be disabled by setting the MDCHODIS bit in the MDCARH register for the carrier high source and the MDCLDIS bit in the MDCARL register for the carrier low source.

23.7 Programmable Modulator Data

The MDBIT of the MDCON register can be selected as the source for the modulator signal. This gives the user the ability to program the value used for modulation.

23.8 Modulator Source Pin Disable

The modulator source default connection to a pin can be disabled by setting the MDMSODIS bit in the MDSRC register.

23.9 Modulated Output Polarity

The modulated output signal provided on the MDOUT pin can also be inverted. Inverting the modulated output signal is enabled by setting the MDOPOL bit of the MDCON register.

23.10 Slew Rate Control

The slew rate limitation on the output port pin can be disabled. The slew rate limitation can be removed by clearing the MDSLRL bit in the MDCON register.

23.11 Operation in Sleep Mode

The DSM module is not affected by Sleep mode. The DSM can still operate during Sleep, if the Carrier and Modulator input sources are also still operable during Sleep.

23.12 Effects of a Reset

Upon any device Reset, the data signal modulator module is disabled. The user's firmware is responsible for initializing the module before enabling the output. The registers are reset to their default values.

PIC16(L)F1826/27

24.4.2 FULL-BRIDGE MODE

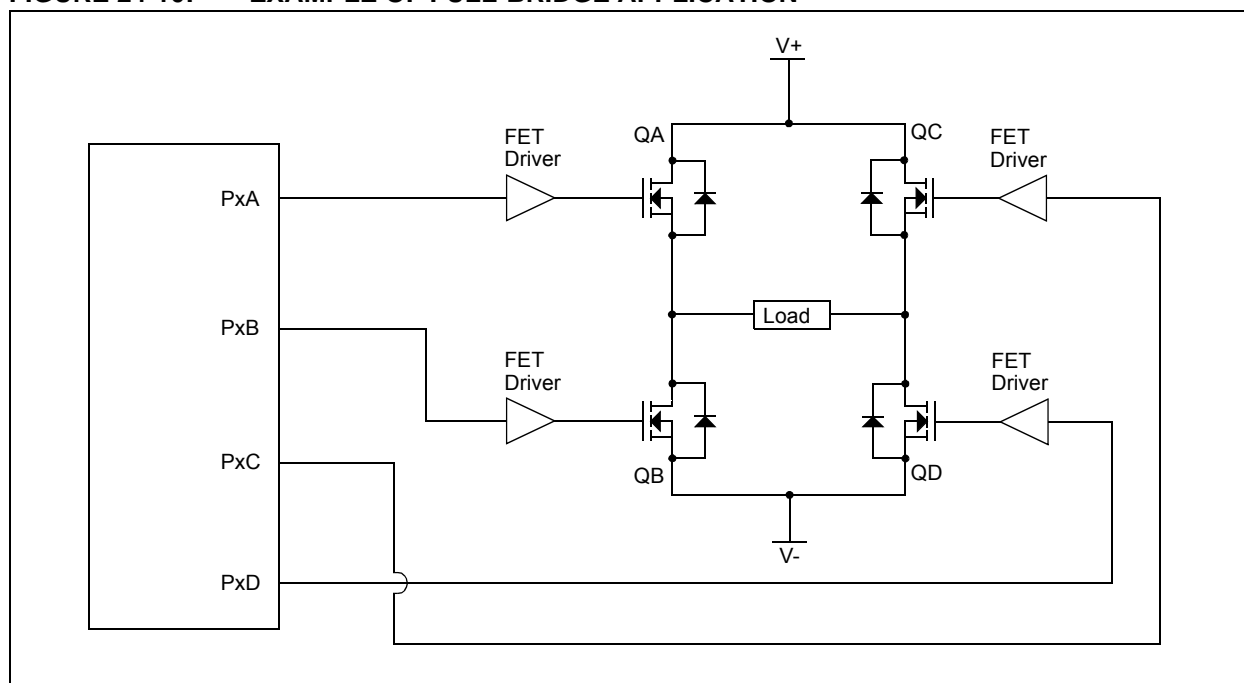
In Full-Bridge mode, all four pins are used as outputs. An example of Full-Bridge application is shown in Figure 24-10.

In the Forward mode, pin CCPx/PxA is driven to its active state, pin PxD is modulated, while PxB and PxC will be driven to their inactive state as shown in Figure 24-11.

In the Reverse mode, PxC is driven to its active state, pin PxB is modulated, while PxA and PxD will be driven to their inactive state as shown Figure 24-11.

PxA, PxB, PxC and PxD outputs are multiplexed with the PORT data latches. The associated TRIS bits must be cleared to configure the PxA, PxB, PxC and PxD pins as outputs.

FIGURE 24-10: EXAMPLE OF FULL-BRIDGE APPLICATION



PIC16(L)F1826/27

REGISTER 24-3: CCPxAS: CCPx AUTO-SHUTDOWN CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
CCPxASE	CCPxAS<2:0>			PSSxAC<1:0>		PSSxBD<1:0>	
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

- bit 7 **CCPxASE:** CCPx Auto-Shutdown Event Status bit
1 = A shutdown event has occurred; CCPx outputs are in shutdown state
0 = CCPx outputs are operating
- bit 6-4 **CCxPAS<2:0>:** CCPx Auto-Shutdown Source Select bits
000 = Auto-shutdown is disabled
001 = Comparator C1 output high⁽¹⁾
010 = Comparator C2 output high⁽¹⁾
011 = Either Comparator C1 or C2 high⁽¹⁾
100 = VIL on INT pin
101 = VIL on INT pin or Comparator C1 high⁽¹⁾
110 = VIL on INT pin or Comparator C2 high⁽¹⁾
111 = VIL on INT pin or Comparator C1 or Comparator C2 high⁽¹⁾
- bit 3-2 **PSSxAC<1:0>:** Pins PxA and PxC Shutdown State Control bits
00 = Drive pins PxA and PxC to '0'
01 = Drive pins PxA and PxC to '1'
1x = Pins PxA and PxC tri-state
- bit 1-0 **PSSxBD<1:0>:** Pins PxB and PxD Shutdown State Control bits
00 = Drive pins PxB and PxD to '0'
01 = Drive pins PxB and PxD to '1'
1x = Pins PxB and PxD tri-state

Note 1: If CxSYNC is enabled, the shutdown will be delayed by Timer1.

25.5.8 GENERAL CALL ADDRESS SUPPORT

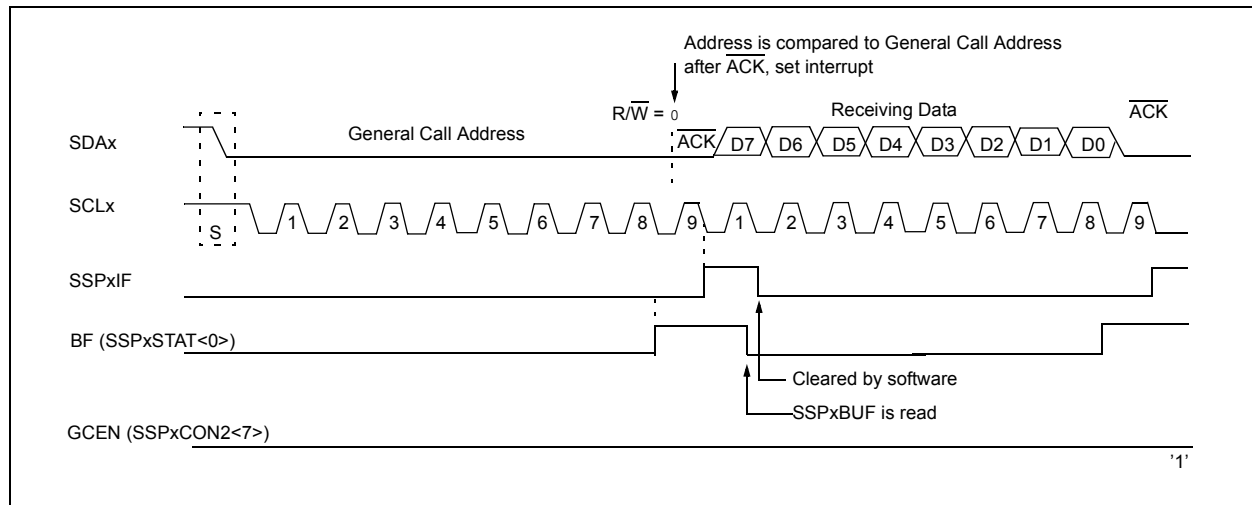
The addressing procedure for the I²C bus is such that the first byte after the Start condition usually determines which device will be the slave addressed by the master device. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge.

The general call address is a reserved address in the I²C protocol, defined as address 0x00. When the GCEN bit of the SSPxCON2 register is set, the slave module will automatically ACK the reception of this address regardless of the value stored in SSPxADD. After the slave clocks in an address of all zeros with the R/W bit clear, an interrupt is generated and slave software can read SSPxBUF and respond. Figure 25-23 shows a general call reception sequence.

In 10-bit Address mode, the UA bit will not be set on the reception of the general call address. The slave will prepare to receive the second byte as data, just as it would in 7-bit mode.

If the AHEN bit of the SSPxCON3 register is set, just as with any other address reception, the slave hardware will stretch the clock after the 8th falling edge of SCLx. The slave must then set its ACKDT value and release the clock with communication progressing as it would normally.

FIGURE 25-24: SLAVE MODE GENERAL CALL ADDRESS SEQUENCE



25.5.9 SSPX MASK REGISTER

An SSPx Mask (SSPxMSK) register (Register 25-5) is available in I²C Slave mode as a mask for the value held in the SSPxSR register during an address comparison operation. A zero ('0') bit in the SSPxMSK register has the effect of making the corresponding bit of the received address a "don't care".

This register is reset to all '1's upon any Reset condition and, therefore, has no effect on standard SSPx operation until written with a mask value.

The SSPx Mask register is active during:

- 7-bit Address mode: address compare of A<7:1>.
- 10-bit Address mode: address compare of A<7:0> only. The SSPx mask has no effect during the reception of the first (high) byte of the address.

PIC16(L)F1826/27

REGISTER 25-4: SSPxCON3: SSPx CONTROL REGISTER 3

R-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

- bit 7 **ACKTIM:** Acknowledge Time Status bit (I²C mode only)⁽³⁾
1 = Indicates the I²C bus is in an Acknowledge sequence, set on 8TH falling edge of SCLx clock
0 = Not an Acknowledge sequence, cleared on 9TH rising edge of SCLx clock
- bit 6 **PCIE:** Stop Condition Interrupt Enable bit (I²C mode only)
1 = Enable interrupt on detection of Stop condition
0 = Stop detection interrupts are disabled⁽²⁾
- bit 5 **SCIE:** Start Condition Interrupt Enable bit (I²C mode only)
1 = Enable interrupt on detection of Start or Restart conditions
0 = Start detection interrupts are disabled⁽²⁾
- bit 4 **BOEN:** Buffer Overwrite Enable bit
In SPI Slave mode:⁽¹⁾
1 = SSPxBUF updates every time that a new data byte is shifted in ignoring the BF bit
0 = If new byte is received with BF bit of the SSPxSTAT register already set, SSPxOV bit of the SSPxCON1 register is set, and the buffer is not updated
In I²C Master mode and SPI Master mode:
This bit is ignored.
In I²C Slave mode:
1 = SSPxBUF is updated and $\overline{\text{ACK}}$ is generated for a received address/data byte, ignoring the state of the SSPxOV bit only if the BF bit = 0.
0 = SSPxBUF is only updated when SSPxOV is clear
- bit 3 **SDAHT:** SDAx Hold Time Selection bit (I²C mode only)
1 = Minimum of 300 ns hold time on SDAx after the falling edge of SCLx
0 = Minimum of 100 ns hold time on SDAx after the falling edge of SCLx
- bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I²C Slave mode only)
If on the rising edge of SCLx, SDAx is sampled low when the module is outputting a high state, the BCLxIF bit of the PIR2 register is set, and bus goes Idle
1 = Enable slave bus collision interrupts
0 = Slave bus collision interrupts are disabled
- bit 1 **AHEN:** Address Hold Enable bit (I²C Slave mode only)
1 = Following the 8th falling edge of SCLx for a matching received address byte; CKP bit of the SSPxCON1 register will be cleared and the SCLx will be held low.
0 = Address holding is disabled
- bit 0 **DHEN:** Data Hold Enable bit (I²C Slave mode only)
1 = Following the 8th falling edge of SCLx for a received data byte; slave hardware clears the CKP bit of the SSPxCON1 register and SCLx is held low.
0 = Data holding is disabled

- Note 1:** For daisy-chained SPI operation; allows the user to ignore all but the last received byte. SSPxOV is still set when a new byte is received and BF = 1, but hardware continues to write the most recent byte to SSPxBUF.
- 2:** This bit has no effect in Slave modes that Start and Stop condition detection is explicitly listed as enabled.
- 3:** The ACKTIM Status bit is only active when the AHEN bit or DHEN bit is set.

TABLE 26-2: SUMMARY OF REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON0	RXDTSSEL	SDO1SEL	SS1SEL	P2BSEL ⁽¹⁾	CCP2SEL ⁽¹⁾	P1DSEL	P1CSEL	CCP1SEL	119
APFCON1	—	—	—	—	—	—	—	TXCKSEL	119
BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	296
INTCON	GIE	PEIE	TMR0IE	INTE	IOCFE	TMR0IF	INTF	IOCF	86
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	87
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	91
RCREG	EUSART Receive Data Register								290*
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	295
SPBRGL	BRG<7:0>								297*
SPBRGH	BRG<15:8>								297*
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	127
TXSTA	CSRC	TX9	TXEN	SYNC	SEnDB	BRGH	TRMT	TX9D	294

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for Asynchronous Reception.

* Page provides register information.

Note 1: PIC16(L)F1827 only.

MOVWI Move W to INDFn

Syntax: [*label*] MOVWI ++FSRn
[*label*] MOVWI --FSRn
[*label*] MOVWI FSRn++
[*label*] MOVWI FSRn--
[*label*] MOVWI k[FSRn]

Operands: n ∈ [0,1]
mm ∈ [00,01, 10, 11]
-32 ≤ k ≤ 31

Operation: W → INDFn
Effective address is determined by

- FSR + 1 (preincrement)
- FSR - 1 (predecrement)
- FSR + k (relative offset)

After the Move, the FSR value will be either:

- FSR + 1 (all increments)
- FSR - 1 (all decrements)

Unchanged

Status Affected: None

Mode	Syntax	mm
Preincrement	++FSRn	00
Predecrement	--FSRn	01
Postincrement	FSRn++	10
Postdecrement	FSRn--	11

Description: This instruction is used to move data between W and one of the indirect registers (INDFn). Before/after this move, the pointer (FSRn) is updated by pre/post incrementing/decrementing it.

Note: The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the FSRn.

FSRn is limited to the range 0000h - FFFFh. Incrementing/decrementing it beyond these bounds will cause it to wrap around.

The increment/decrement operation on FSRn WILL NOT affect any Status bits.

NOP No Operation

Syntax: [*label*] NOP

Operands: None

Operation: No operation

Status Affected: None

Description: No operation.

Words: 1

Cycles: 1

Example: NOP

OPTION Load OPTION_REG Register with W

Syntax: [*label*] OPTION

Operands: None

Operation: (W) → OPTION_REG

Status Affected: None

Description: Move data from W register to OPTION_REG register.

Words: 1

Cycles: 1

Example: OPTION

Before Instruction
OPTION_REG = 0xFF
W = 0x4F

After Instruction
OPTION_REG = 0x4F
W = 0x4F

RESET Software Reset

Syntax: [*label*] RESET

Operands: None

Operation: Execute a device Reset. Resets the nRI flag of the PCON register.

Status Affected: None

Description: This instruction provides a way to execute a hardware Reset by software.

32.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers and dsPIC® digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
 - MPLAB® IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB C Compiler for Various Device Families
 - HI-TECH C for Various Device Families
 - MPASM™ Assembler
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
 - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
 - MPLAB ICD 3
 - PICKit™ 3 Debug Express
- Device Programmers
 - PICKit™ 2 Programmer
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

32.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
 - Simulator
 - Programmer (sold separately)
 - In-Circuit Emulator (sold separately)
 - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
 - Source files (C or assembly)
 - Mixed C and assembly
 - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

Steering Synchronization	224
PWM Mode. See Enhanced Capture/Compare/PWM	212
PWM Steering	223
PWMxCON Register	229

R

RCREG	292
RCREG Register	29
RCSTA Register	29, 295
Reader Response	404
Read-Modify-Write Operations	325
Reference Clock	69
Associated Registers	71
Registers	
ADCON0 (ADC Control 0)	145
ADCON1 (ADC Control 1)	146
ADRESH (ADC Result High) with ADFM = 0)	147
ADRESH (ADC Result High) with ADFM = 1)	148
ADRESL (ADC Result Low) with ADFM = 0)	147
ADRESL (ADC Result Low) with ADFM = 1)	148
ANSELA (PORTA Analog Select)	123
ANSELB (PORTB Analog Select)	128
APFCON0 (Alternate Pin Function Control 0)	119
APFCON1 (Alternate Pin Function Control 1)	119
BAUDCON (Baud Rate Control)	296
BORCON Brown-out Reset Control)	75
CCPTMRS (PWM Timer Selection Control)	227
CCPxAS (CCPx Auto-Shutdown Control)	228
CCPxCON (ECCPx Control)	226
CLKRCON (Reference Clock Control)	70
CMOUT (Comparator Output)	171
CMxCON0 (Cx Control)	170
CMxCON1 (Cx Control 1)	171
Configuration Word 1	44
Configuration Word 2	46
Core Function, Summary	27
CPSCON0 (Capacitive Sensing Control Register 0)	318
CPSCON1 (Capacitive Sensing Control Register 1)	319
DACCON0	156
DACCON1	156
Device ID	49
EEADRL (EEPROM Address)	113
EECON1 (EEPROM Control 1)	115
EECON2 (EEPROM Control 2)	116
EEDATH (EEPROM Data)	113, 114
EEDATL (EEPROM Data)	113
FVRCON	136
INTCON (Interrupt Control)	86
IOCBF (Interrupt-on-Change Flag)	132
IOCBN (Interrupt-on-Change Negative Edge)	132
IOCBP (Interrupt-on-Change Positive Edge)	132
LATA (Data Latch PORTA)	122
LATB (Data Latch PORTB)	127
MDCARH (Modulation High Carrier Control Register)	200
MDCARL (Modulation Low Carrier Control Register)	201
MDCON (Modulation Control Register)	198
MDSRC (Modulation Source Control Register)	199
OPTION_REG (OPTION)	176
OSCCON (Oscillator Control)	65
OSCSTAT (Oscillator Status)	66
OSCTUNE (Oscillator Tuning)	67
PCON (Power Control Register)	79
PCON (Power Control)	79
PIE1 (Peripheral Interrupt Enable 1)	87
PIE2 (Peripheral Interrupt Enable 2)	88

PIE3 (Peripheral Interrupt Enable 3)	89
PIE4 (Peripheral Interrupt Enable 4)	90
PIR1 (Peripheral Interrupt Register 1)	91
PIR2 (Peripheral Interrupt Request 2)	92
PIR3 (Peripheral Interrupt Request 3)	93
PIR4 (Peripheral Interrupt Request 4)	94
PORTA	122
PORTB	127
PSTRxCON (PWM Steering Control)	230
PWMxCON (Enhanced PWM Control)	229
RCREG	302
RCSTA (Receive Status and Control)	295
SPBRGH	297
SPBRGL	297
Special Function, Summary	28
SRCON0 (SR Latch Control 0)	159
SRCON1 (SR Latch Control 1)	160
SSPxADD (MSSPx Address and Baud Rate, I ² C Mode)	283
SSPxCON1 (MSSPx Control 1)	280
SSPxCON2 (SSPx Control 2)	281
SSPxCON3 (SSPx Control 3)	282
SSPxMSK (SSPx Mask)	283
SSPxSTAT (SSPx Status)	279
STATUS	21
T1CON (Timer1 Control)	185
T1GCON (Timer1 Gate Control)	186
TRISA (Tri-State PORTA)	122
TRISB (Tri-State PORTB)	127
TXCON	191
TXSTA (Transmit Status and Control)	294
WDTCON (Watchdog Timer Control)	99
WPUB (Weak Pull-up PORTB)	123, 128
RESET	335
Reset	73
Reset Instruction	76
Resets	73
Associated Registers	80
Revision History	393

S

Shoot-through Current	222
Software Simulator (MPLAB SIM)	381
SPBRG Register	29
SPBRGH Register	297
SPBRGL Register	297
Special Event Trigger	143
Special Function Registers (SFRs)	28
SPI Mode (MSSPx)	
Associated Registers	241
SPI Clock	237
SR Latch	157
Associated registers w/ SR Latch	161
SRCON0 Register	159
SRCON1 Register	160
SSP1ADD Register	30
SSP1BUF Register	30
SSP1CON Register	30
SSP1CON2 Register	30
SSP1CON3 Register	30
SSP1MSK Register	30
SSP1STAT Register	30
SSP2ADD Register	30
SSP2BUF Register	30
SSP2CON1 Register	30
SSP2CON2 Register	30

PIC16(L)F1826/27

SSP2CON3 Register	30
SSP2MSK Register	30
SSP2STAT Register	30
SSPxADD Register	283
SSPxCON1 Register	280
SSPxCON2 Register	281
SSPxCON3 Register	282
SSPxMSK Register	283
SSPxOV	268
SSPxOV Status Flag	268
SSPxSTAT Register	279
R/W Bit	247
Stack	37
Accessing	37
Reset	39
Stack Overflow/Underflow	76
STATUS Register	21
SUBWFB	337

T

T1CON Register	28, 185
T1GCON Register	186
T2CON Register	28, 32
Temperature Indicator Module	137
Thermal Considerations	352
Timer0	173, 192
Associated Registers	176
Operation	173
Specifications	360
Timer1	177
Associated registers	187
Asynchronous Counter Mode	179
Reading and Writing	179
Clock Source Selection	178
Interrupt	181
Operation	178
Operation During Sleep	181
Oscillator	179
Prescaler	179
Specifications	360
Timer1 Gate	
Selecting Source	179
TMR1H Register	177
TMR1L Register	177
Timer2	
Associated registers	192
Timer2/4/6	189
Associated registers	192
Timers	
Timer1	
T1CON	185
T1GCON	186
Timer2/4/6	
TXCON	191
Timing Diagrams	
A/D Conversion	362
A/D Conversion (Sleep Mode)	362
Acknowledge Sequence	270
Asynchronous Reception	292
Asynchronous Transmission	288
Asynchronous Transmission (Back to Back)	288
Auto Wake-up Bit (WUE) During Normal Operation	304
Auto Wake-up Bit (WUE) During Sleep	304
Automatic Baud Rate Calibration	302
Baud Rate Generator with Clock Arbitration	263
BRG Reset Due to SDA Arbitration During Start Condition	274
Brown-out Reset (BOR)	358
Brown-out Reset Situations	75
Bus Collision During a Repeated Start Condition (Case 1)	275
Bus Collision During a Repeated Start Condition (Case 2)	275
Bus Collision During a Start Condition (SCL = 0)	276
Bus Collision During a Stop Condition (Case 1)	276
Bus Collision During a Stop Condition (Case 2)	276
Bus Collision During Start Condition (SDA only)	273
Bus Collision for Transmit and Acknowledge	272
CLKOUT and I/O	356
Clock Synchronization	260
Clock Timing	354
Comparator Output	163
Enhanced Capture/Compare/PWM (ECCP)	360
Fail-Safe Clock Monitor (FSCM)	64
First Start Bit Timing	264
Full-Bridge PWM Output	217
Half-Bridge PWM Output	215, 222
I ² C Bus Data	368
I ² C Bus Start/Stop Bits	367
I ² C Master Mode (7 or 10-Bit Transmission)	267
I ² C Master Mode (7-Bit Reception)	269
I ² C Stop Condition Receive or Transmit Mode	271
INT Pin Interrupt	84
Internal Oscillator Switch Timing	59
PWM Auto-shutdown	221
Firmware Restart	220
PWM Direction Change	218
PWM Direction Change at Near 100% Duty Cycle	219
PWM Output (Active-High)	213
PWM Output (Active-Low)	214
Repeat Start Condition	265
Reset Start-up Sequence	77
Reset, WDT, OST and Power-up Timer	357
Send Break Character Sequence	305
SPI Master Mode (CKE = 1, SMP = 1)	365
SPI Mode (Master Mode)	237
SPI Slave Mode (CKE = 0)	366
SPI Slave Mode (CKE = 1)	366
Synchronous Reception (Master Mode, SREN)	310
Synchronous Transmission	307
Synchronous Transmission (Through TXEN)	307
Timer0 and Timer1 External Clock	359
Timer1 Incrementing Edge	181
Two Speed Start-up	62
USART Synchronous Receive (Master/Slave)	364
USART Synchronous Transmission (Master/Slave)	364
Wake-up from Interrupt	96
Timing Diagrams and Specifications	
PLL Clock	355
Timing Parameter Symbolology	353
Timing Requirements	
I ² C Bus Data	369
I ² C Bus Start/Stop Bits	368
SPI Mode	367
TMR0 Register	28
TMR1H Register	28
TMR1L Register	28
TMR2 Register	28, 32
TRIS	338
TRISA Register	28, 122

Worldwide Sales and Service

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta

Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston

Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago

Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland

Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas

Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit

Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Indianapolis

Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles

Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara

Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto

Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office

Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney

Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing

Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu

Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing

Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hong Kong SAR

Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing

Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao

Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai

Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang

Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen

Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan

Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian

Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen

Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai

Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore

Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi

Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune

Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama

Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu

Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul

Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur

Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang

Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila

Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore

Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu

Tel: 886-3-6578-300
Fax: 886-3-6578-370

Taiwan - Kaohsiung

Tel: 886-7-213-7830
Fax: 886-7-330-9305

Taiwan - Taipei

Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok

Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels

Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen

Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris

Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich

Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan

Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen

Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid

Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham

Tel: 44-118-921-5869
Fax: 44-118-921-5820