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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1826-e-ml

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3.0 MEMORY ORGANIZATION

There are three types of memory in PIC16(L)F1826/27: Data Memory, Program Memory and Data EEPROM Memory⁽¹⁾.

- Program Memory
- Data Memory
 - Core Registers
 - Special Function Registers
 - General Purpose RAM
 - Common RAM
 - Device Memory Maps
 - Special Function Registers Summary
- Data EEPROM memory⁽¹⁾

Note 1: The Data EEPROM Memory and the method to access Flash memory through the EECON registers is described in Section 11.0 "Data EEPROM and Flash Program Memory Control". The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

3.1 Program Memory Organization

The enhanced mid-range core has a 15-bit program counter capable of addressing a $32K \times 14$ program memory space. Table 3-1 shows the memory sizes implemented for the PIC16(L)F1826/27 family. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figures 3-1 and 3-2).

TABLE 3-1:DEVICE SIZES AND ADDRESSES

Device	Program Memory Space (Words)	Last Program Memory Address		
PIC16(L)F1826	2,048	07FFh		
PIC16(L)F1827	4,096	0FFFh		

TABLE 3-3: PIC16(L)F1826/27 MEMORY MAP (CONTINUED)

	BANK 8		BANK 9		BANK 10		BANK 11		BANK 12		BANK 13		BANK 14		BANK 15
400h	Core Registers (Table 3-2)	480h	Core Registers (Table 3-2)	500h	Core Registers (Table 3-2)	580h	Core Registers (Table 3-2)	600h	Core Registers (Table 3-2)	680h	Core Registers (Table 3-2)	700h	Core Registers (Table 3-2)	780h	Core Registers (Table 3-2)
40Bh		48Bh		50Bh		58Bh		60Bh		68Bh		70Bh		78Bh	
40Ch	_	48Ch	_	50Ch	_	58Ch	_	60Ch	_	68Ch	_	70Ch	—	78Ch	_
40Dh	_	48Dh	—	50Dh	—	58Dh	—	60Dh	—	68Dh	—	70Dh	—	78Dh	—
40Eh	—	48Eh	—	50Eh	—	58Eh	—	60Eh	—	68Eh	—	70Eh	—	78Eh	—
40Fh	—	48Fh	—	50Fh	—	58Fh	—	60Fh	—	68Fh	—	70Fh	—	78Fh	—
410h	_	490h	_	510h	_	590h	—	610h	_	690h	_	710h		790h	—
411h	_	491h		511h		591h		611h		691h		711h		791h	—
412h	—	492h	_	512h	_	592h		612h	_	692h	_	712h	_	792h	_
413h	_	493h		513h		593h		613h		693h		713h		793h	_
414h	(1)	494h	_	514h		594h	—	614h		694h		714h		794h	_
415h	TMR4 ⁽¹⁾	495h		515h		595h		615h		695h		715h	_	795h	_
416h	PR4 ⁽¹⁾	496h	—	516h	—	596h	—	616h	—	696h	—	716h	—	796h	—
417h	T4CON ⁽¹⁾	497h	—	517h	—	597h	_	617h	—	697h	—	717h	—	797h	_
418h	_	498h	—	518h	—	598h	—	618h	—	698h	—	718h	—	798h	—
419h	—	499h	—	519h	—	599h	—	619h	—	699h	—	719h	—	799h	—
41Ah	_	49Ah	—	51Ah	_	59Ah	—	61Ah	_	69Ah	_	71Ah	_	79Ah	_
41Bh	_	49Bh	—	51Bh	—	59Bh	—	61Bh	—	69Bh	—	71Bh	_	79Bh	_
41Ch	TMR6 ⁽¹⁾	49Ch	—	51Ch	—	59Ch	—	61Ch	—	69Ch	—	71Ch	—	79Ch	—
41Dh	PR6 ⁽¹⁾	49Dh	—	51Dh	—	59Dh	_	61Dh	—	69Dh	—	71Dh	—	79Dh	_
41Eh	T6CON ⁽¹⁾	49Eh	—	51Eh	—	59Eh	—	61Eh	—	69Eh	—	71Eh	—	79Eh	—
41Fh	—	49Fh	_	51Fh	_	59Fh		61Fh	_	69Fh	_	71Fh	—	79Fh	—
420h		4A0h		520h		5A0h		620h		6A0h		720h		7A0h	
	Unimplemented Read as '0'														
46Fh		4EFh		56Fh		5EFh		66Fh		6EFh		76Fh		7EFh	
470h		4F0h		570h		5F0h		670h		6F0h		770h		7F0h	
	Accesses 70h – 7Fh	AEEh	Accesses 70h – 7Fh	57Eb	Accesses 70h – 7Fh		Accesses 70h – 7Fh	075	Accesses 70h – 7Fh	055	Accesses 70h – 7Fh		Accesses 70h – 7Fh	7661	Accesses 70h – 7Fh
47⊦h		4660		5/11		5⊢⊦h		67⊦h		ö⊢⊦h		//⊦h		/⊦⊦h	

Legend: = Unimplemented data memory locations, read as '0'

4.0 DEVICE CONFIGURATION

Device Configuration consists of Configuration Word 1 and Configuration Word 2, Code Protection and Device ID.

4.1 Configuration Words

There are several Configuration Word bits that allow different oscillator and memory protection options. These are implemented as Configuration Word 1 at 8007h and Configuration Word 2 at 8008h.

Note:	The DEBUG bit in Configuration Word is
	managed automatically by device
	development tools including debuggers
	and programmers. For normal device
	operation, this bit should be maintained as
	a '1'.

7.1 Power-on Reset (POR)

The POR circuit holds the device in Reset until VDD has reached an acceptable level for minimum operation. Slow rising VDD, fast operating speeds or analog performance may require greater than minimum VDD. The PWRT, BOR or MCLR features can be used to extend the start-up period until all device operation conditions have been met.

7.1.1 POWER-UP TIMER (PWRT)

The Power-up Timer provides a nominal 64 ms timeout on POR or Brown-out Reset.

The device is held in Reset as long as PWRT is active. The PWRT delay allows additional time for the VDD to rise to an acceptable level. The Power-up Timer is enabled by clearing the PWRTE bit in Configuration Word 1.

The Power-up Timer starts after the release of the POR and BOR.

For additional information, refer to Application Note AN607, *"Power-up Trouble Shooting"* (DS00607).

7.2 Brown-Out Reset (BOR)

The BOR circuit holds the device in Reset when Vdd reaches a selectable minimum level. Between the POR and BOR, complete voltage range coverage for execution protection can be implemented.

The Brown-out Reset module has four operating modes controlled by the BOREN<1:0> bits in Configuration Word 1. The four operating modes are:

- · BOR is always on
- · BOR is off when in Sleep
- · BOR is controlled by software
- · BOR is always off

Refer to Table 7-1 for more information.

The Brown-out Reset voltage level is selectable by configuring the BORV bit in Configuration Word 2.

A VDD noise rejection filter prevents the BOR from triggering on small events. If VDD falls below VBOR for a duration greater than parameter TBORDC, the device will reset. See Figure 7-2 for more information.

BOREN<1:0>	SBOREN	Device Mode	BOR Mode	Device Operation upon release of POR	Device Operation upon wake- up from Sleep		
11	Х	Х	Active	Waits for BOR ready ⁽¹⁾			
1.0		Awake Active		Maita far	Waits for DOD ready		
10	Х	Sleep	Disabled	Waits for BOR feady			
0.1	1	×	Active	Begins immediately			
UL	0	^	Disabled	Begins immediately			
00	Х	х	Disabled	Begins immediately			

TABLE 7-1:BOR OPERATING MODES

Note 1: Even though this case specifically waits for the BOR, the BOR is already operating, so there is no delay in start-up.

7.2.1 BOR IS ALWAYS ON

When the BOREN bits of Configuration Word 1 are set to '11', the BOR is always on. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is active during Sleep. The BOR does not delay wake-up from Sleep.

7.2.2 BOR IS OFF IN SLEEP

When the BOREN bits of Configuration Word 1 are set to '10', the BOR is on, except in Sleep. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is not active during Sleep. The device wake-up will be delayed until the BOR is ready.

7.2.3 BOR CONTROLLED BY SOFTWARE

When the BOREN bits of Configuration Word 1 are set to '01', the BOR is controlled by the SBOREN bit of the BORCON register. The device start-up is not delayed by the BOR ready condition or the VDD level.

BOR protection begins as soon as the BOR circuit is ready. The status of the BOR circuit is reflected in the BORRDY bit of the BORCON register.

BOR protection is unchanged by Sleep.

				00	0-0	0-0
	- WPUA5	—	_	—	—	—
bit 7						bit 0

REGISTER 12-6: WPUA: WEAK PULL-UP PORTA REGISTER

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6	Unimplemented: Read as '0'
bit 5	WPUA5: Weak Pull-up RA5 Control bit
	If $\overline{\text{MCLRE}}$ in Configuration Word 1 = 0, $\overline{\text{MCLR}}$ is disabled):
	1 = Weak Pull-up enabled ⁽¹⁾
	0 = Weak Pull-up disabled
	If MCLRE in Configuration Word 1 = 1, MCLR is enabled):
	Weak Pull-up is always enabled.

bit 4-0 Unimplemented: Read as '0'

Note 1: Global WPUEN bit of the OPTION register must be cleared for individual pull-ups to be enabled.

2: The weak pull-up device is automatically disabled if the pin is in configured as an output.

REGISTER 12-7: ANSELA: PORTA ANALOG SELECT REGISTER

U-0	U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
—	—	—	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-5 Unimplemented: Read as '0'

bit 4-0

ANSA<4:0>: Analog Select between Analog or Digital Function on pins RA<4:0>, respectively

0 = Digital I/O. Pin is assigned to port or digital special function.

1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital input buffer disabled.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	
WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0	
bit 7							bit 0	
Legend:								
R = Readable I	R = Readable bit W = Writable bit			U = Unimplemented bit, read as '0'				
u = Bit is unchanged x = Bit is unknown -n/				-n/n = Value at POR and BOR/Value at all other Resets				

REGISTER 12-11: WPUB: WEAK PULL-UP PORTB REGISTER

bit 7-0 WPUB<7:0>: Weak Pull-up Register bits

1 = Pull-up enabled

'1' = Bit is set

0 = Pull-up disabled

Note 1: Global WPUEN bit of the OPTION register must be cleared for individual pull-ups to be enabled.

2: The weak pull-up device is automatically disabled if the pin is in configured as an output.

REGISTER 12-12: ANSELB: PORTB ANALOG SELECT REGISTER

'0' = Bit is cleared

R/W-1/1	U-0						
ANSB7	ANSB6	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-1 **ANSB<7:1>**: Analog Select between Analog or Digital Function on Pins RB<7:1>, respectively 0 = Digital I/O. Pin is assigned to port or digital special function.

1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital input buffer disabled.

bit 0 Unimplemented: Read as '0'

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

NOTES:

NOTES:



FIGURE 18-1: SR LATCH SIMPLIFIED BLOCK DIAGRAM

21.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module is a 16-bit timer/counter with the following features:

- 16-bit timer/counter register pair (TMR1H:TMR1L)
- Programmable internal or external clock source
- 2-bit prescaler
- · Dedicated 32 kHz oscillator circuit
- · Optionally synchronized comparator out
- Multiple Timer1 gate (count enable) sources
- · Interrupt on overflow
- Wake-up on overflow (external clock, Asynchronous mode only)
- Time base for the Capture/Compare function
- Special Event Trigger (with CCP/ECCP)
- · Selectable Gate Source Polarity

- Gate Toggle mode
- Gate Single-pulse mode
- Gate Value Status
- Gate Event Interrupt
- Figure 21-1 is a block diagram of the Timer1 module.



FIGURE 21-1: TIMER1 BLOCK DIAGRAM

24.4.6 PWM STEERING MODE

In Single Output mode, PWM steering allows any of the PWM pins to be the modulated signal. Additionally, the same PWM signal can be simultaneously available on multiple pins.

Once the Single Output mode is selected (CCPxM<3:2> = 11 and PxM<1:0> = 00 of the CCPxCON register), the user firmware can bring out the same PWM signal to one, two, three or four output pins by setting the appropriate STRx<D:A> bits of the PSTRxCON register, as shown in Register 24-5.

Note: The associated TRIS bits must be set to output ('0') to enable the pin output driver in order to see the PWM signal on the pin.

While the PWM Steering mode is active, CCPxM<1:0> bits of the CCPxCON register select the PWM output polarity for the Px<D:A> pins.

The PWM auto-shutdown operation also applies to PWM Steering mode as described in **Section 24.4.3 "Enhanced PWM Auto-shutdown mode"**. An auto-shutdown event will only affect pins that have PWM outputs enabled.

FIGURE 24-18: SIMPLIFIED STEERING BLOCK DIAGRAM



25.2.2 SPI MODE OPERATION

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits (SSPxCON1<5:0> and SSPxSTAT<7:6>). These control bits allow the following to be specified:

- · Master mode (SCKx is the clock output)
- · Slave mode (SCKx is the clock input)
- Clock Polarity (Idle state of SCKx)
- Data Input Sample Phase (middle or end of data output time)
- Clock Edge (output data on rising/falling edge of SCKx)
- Clock Rate (Master mode only)
- · Slave Select mode (Slave mode only)

To enable the serial port, SSPx Enable bit, SSPxEN of the SSPxCON1 register, must be set. To reset or reconfigure SPI mode, clear the SSPxEN bit, re-initialize the SSPxCONx registers and then set the SSPxEN bit. This configures the SDIx, SDOx, SCKx and SSx pins as serial port pins. For the pins to behave as the serial port function, some must have their data direction bits (in the TRIS register) appropriately programmed as follows:

- · SDIx must have corresponding TRIS bit set
- · SDOx must have corresponding TRIS bit cleared
- SCKx (Master mode) must have corresponding TRIS bit cleared
- SCKx (Slave mode) must have corresponding TRIS bit set
- SSx must have corresponding TRIS bit set

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value.

The MSSPx consists of a transmit/receive shift register (SSPxSR) and a buffer register (SSPxBUF). The SSPxSR shifts the data in and out of the device, MSb first. The SSPxBUF holds the data that was written to the SSPxSR until the received data is ready. Once the 8 bits of data have been received, that byte is moved to the SSPxBUF register. Then, the Buffer Full Detect bit, BF of the SSPxSTAT register, and the interrupt flag bit, SSPxIF, are set. This double-buffering of the received data (SSPxBUF) allows the next byte to start reception before reading the data that was just received. Any write to the **SSPxBUF** reaister durina transmission/reception of data will be ignored and the write collision detect bit WCOL of the SSPxCON1 register, will be set. User software must clear the WCOL bit to allow the following write(s) to the SSPxBUF register to complete successfully.

When the application software is expecting to receive valid data, the SSPxBUF should be read before the next byte of data to transfer is written to the SSPxBUF. The Buffer Full bit, BF of the SSPxSTAT register, indicates when SSPxBUF has been loaded with the received data (transmission is complete). When the SSPxBUF is read, the BF bit is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally, the MSSPx interrupt is used to determine when the transmission/reception has completed. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur.



FIGURE 25-5: SPI MASTER/SLAVE CONNECTION

25.4.5 START CONDITION

The I^2C specification defines a Start condition as a transition of SDAx from a high to a low state while SCLx line is high. A Start condition is always generated by the master and signifies the transition of the bus from an Idle to an Active state. Figure 25-10 shows wave forms for Start and Stop conditions.

A bus collision can occur on a Start condition if the module samples the SDAx line low before asserting it low. This does not conform to the I²C Specification that states no bus collision can occur on a Start.

25.4.6 STOP CONDITION

A Stop condition is a transition of the SDAx line from low-to-high state while the SCLx line is high.

Note: At least one SCLx low time must appear before a Stop is valid, therefore, if the SDAx line goes low then high again while the SCLx line stays high, only the Start condition is detected.

25.4.7 RESTART CONDITION

A Restart is valid any time that a Stop would be valid. A master can issue a Restart if it wishes to hold the bus after terminating the current transfer. A Restart has the same effect on the slave that a Start would, resetting all slave logic and preparing it to clock in an address. The master may want to address the same or another slave.

In 10-bit Addressing Slave mode a Restart is required for the master to clock data out of the addressed slave. Once a slave has been fully addressed, matching both high and low address bytes, the master can issue a Restart and the high address byte with the R/\overline{W} bit set. The slave logic will then hold the clock and prepare to clock out data.

After a full match with R/\overline{W} clear in 10-bit mode, a prior match flag is set and maintained. Until a Stop condition, a high address with R/\overline{W} clear, or high address match fails.

25.4.8 START/STOP CONDITION INTERRUPT MASKING

The SCIE and PCIE bits of the SSPxCON3 register can enable the generation of an interrupt in Slave modes that do not typically support this function. Slave modes where interrupt on Start and Stop detect are already enabled, these bits will have no effect.









25.5.2 SLAVE RECEPTION

When the R/\overline{W} bit of a matching received address byte is clear, the R/\overline{W} bit of the SSPxSTAT register is cleared. The received address is loaded into the SSPx-BUF register and acknowledged.

When the overflow condition exists for a received address, then not Acknowledge is given. An overflow condition is defined as either bit BF of the SSPxSTAT register is set, or bit SSPxOV of the SSPxCON1 register is set. The BOEN bit of the SSPxCON3 register modifies this operation. For more information see Register 25-4.

An MSSPx interrupt is generated for each transferred data byte. Flag bit, SSPxIF, must be cleared by software.

When the SEN bit of the SSPxCON2 register is set, SCLx will be held low (clock stretch) following each received byte. The clock must be released by setting the CKP bit of the SSPxCON1 register, except sometimes in 10-bit mode. See **Section 25.2.3 "SPI Master Mode"** for more detail.

25.5.2.1 7-bit Addressing Reception

This section describes a standard sequence of events for the MSSPx module configured as an I^2C Slave in 7-bit Addressing mode. All decisions made by hardware or software and their effect on reception. Figure 25-13 and Figure 25-14 is used as a visual reference for this description.

This is a step by step process of what typically must be done to accomplish I^2C communication.

- 1. Start bit detected.
- 2. S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
- 3. Matching address with R/\overline{W} bit clear is received.
- 4. The slave pulls SDAx low sending an ACK to the master, and sets SSPxIF bit.
- 5. Software clears the SSPxIF bit.
- 6. Software reads received address from SSPx-BUF clearing the BF flag.
- 7. If SEN = 1; Slave software sets CKP bit to release the SCLx line.
- 8. The master clocks out a data byte.
- 9. Slave drives SDAx low sending an ACK to the master, and sets SSPxIF bit.
- 10. Software clears SSPxIF.
- 11. Software reads the received byte from SSPx-BUF clearing BF.
- 12. Steps 8-12 are repeated for all received bytes from the Master.
- 13. Master sends Stop condition, setting P bit of SSPxSTAT, and the bus goes Idle.

25.5.2.2 7-bit Reception with AHEN and DHEN

Slave device reception with AHEN and DHEN set operate the same as without these options with extra interrupts and clock stretching added after the 8th falling edge of SCLx. These additional interrupts allow the slave software to decide whether it wants to ACK the receive address or data byte, rather than the hardware. This functionality adds support for PMBus[™] that was not present on previous versions of this module.

This list describes the steps that need to be taken by slave software to use these options for I^2C communcation. Figure 25-15 displays a module using both address and data holding. Figure 25-16 includes the operation with the SEN bit of the SSPxCON2 register set.

- 1. S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
- Matching address with R/W bit clear is clocked in. SSPxIF is set and CKP cleared after the 8th falling edge of SCLx.
- 3. Slave clears the SSPxIF.
- Slave can look at the ACKTIM bit of the SSPxCON3 register to determine if the SSPxIF was after or before the ACK.
- 5. Slave reads the address value from SSPxBUF, clearing the BF flag.
- 6. Slave sets ACK value clocked out to the master by setting ACKDT.
- 7. Slave releases the clock by setting CKP.
- 8. SSPxIF is set after an ACK, not after a NACK.
- 9. If SEN = 1 the slave hardware will stretch the clock after the ACK.

10. Slave clears SSPxIF.

Note: SSPxIF is still set after the 9th falling edge of SCLx even if there is no clock stretching and BF has been cleared. Only if NACK is sent to Master is SSPxIF not set

- 11. SSPxIF set and CKP cleared after 8th falling edge of SCLx for a received data byte.
- 12. Slave looks at ACKTIM bit of SSPxCON3 to determine the source of the interrupt.
- 13. Slave reads the received data from SSPxBUF clearing BF.
- 14. Steps 7-14 are the same for each received data byte.
- 15. Communication is ended by either the slave sending an ACK = 1, or the master sending a Stop condition. If a Stop is sent and Interrupt on Stop Detect is disabled, the slave will only know by polling the P bit of the SSTSTAT register.

-				-			1	
R-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	
ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	
bit 7	bit 7 bit 0							
Legend:								
R = Readal	ble bit	W = Writable bit		U = Unimpler	mented bit, read	as '0'		
u = Bit is ur	nchanged	x = Bit is unknown		-n/n = Value at POR and BOR/Value at all other Resets				
'1' = Bit is s	et	'0' = Bit is clea	i' = Bit is cleared					
bit 7	ACKTIM: Ack	ACKTIM: Acknowledge Time Status bit (I ² C mode only) ⁽³⁾						
	1 = Indicates	1 = Indicates the I ² C bus is in an Acknowledge sequence, set on 8 TH falling edge of SCLx clock				Lx clock		
	0 = Not an Ac	knowledge sec	quence, cleare	ed on 9 [™] rising	g edge of SCLx	clock		
bit 6	PCIE: Stop Co	ondition Interru	pt Enable bit	(I ² C mode only	()			
	1 = Enable int 0 = Stop dete	terrupt on deteo	are disabled	2)				
bit 5	SCIE: Start Co	ondition Interru	pt Enable bit	(I ² C mode only	()			
	1 = Enable int	terrupt on dete	ction of Start of	or Restart cond	litions			
	0 = Start dete	ction interrupts	are disabled	2)				
bit 4	BOEN: Buffer	Overwrite Ena	able bit					
	In SPI Slave r	node: ⁽¹⁾			1		- 1 1	
	1 = SSPX 0 = If per	(BUF updates (every time that	t a new data b	iyte is snifted in	Ignoring the BF	- DIT vOV bit of the	
	SSPx	CON1 register	is set, and th	e buffer is not	updated			
	<u>In I²C Master</u>	mode and SPI	Master mode	<u>e:</u>				
	This bit is	ignored.						
	$\frac{\text{In I}=C \text{ Slave n}}{1 = SSP}$	<u>node:</u> «RUE is undate	ed and \overline{ACK} is	s generated fo	r a received ad	dress/data byte	ianorina the	
	state	of the SSPxO\	/ bit only if the	e BF bit = 0.		areoo, aata byte	, ignoring the	
	0 = SSPx	BUF is only up	dated when s	SSPxOV is clea	ar			
bit 3	SDAHT: SDA	SDAHT: SDAx Hold Time Selection bit (I ² C mode only)						
	1 = Minimum of 300 ns hold time on SDAx after the falling edge of SCLx							
bit 2	SBCDE: Slav	0 = Minimum of 100 hs hold time of SDAx after the failing edge of SCLx SBCDE: Slave Mode Rus Collision Detect Enable bit (I^2 C Slave mode only)						
	If on the rising edge of SCLX. SDAx is sampled low when the module is outputting a high state, the							
	BCLxIF bit of	the PIR2 regist	ter is set, and	bus goes Idle		s outputting u i	light state, the	
	1 = Enable sla	ave bus collisio	n interrupts					
	0 = Slave bus	collision interr	upts are disal	bled				
bit 1	AHEN: Addre	ss Hold Enable	e bit (I ² C Slav	e mode only)				
	1 = Following	the 8th falling	g edge of SC	Lx for a match	hing received a	ddress byte; C	CKP bit of the	
	0 = Address h	N1 register Will	be cleared a	nd the SCLX w	ill be held low.			
hit 0	DHEN. Data 4	Hold Enable bit	(1 ² C Slave m	ode only)				
DILU	1 = Following	the 8th falling	edue of SCL x	for a received	data hyte: slave	hardware clea	rs the CKP hit	
	of the SS	PxCON1 regis	ter and SCLx	is held low.		naroware cica		
	0 = Data hold	ing is disabled						
Note 1	For daisy-chained	SPI operation: a	allows the use	r to ignore all h	out the last receiv	ved byte SSPx	OV is still set	
\	when a new byte is	received and E	3F = 1, but ha	rdware continu	es to write the m	nost recent byte	to SSPxBUF.	

REGISTER 25-4: SSPxCON3: SSPx CONTROL REGISTER 3

2: This bit has no effect in Slave modes that Start and Stop condition detection is explicitly listed as enabled.

3: The ACKTIM Status bit is only active when the AHEN bit or DHEN bit is set.

26.1.2.8 Asynchronous Reception Set-up:

- Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Section 26.3 "EUSART Baud Rate Generator (BRG)").
- 2. Clear the ANSEL bit for the RX pin (if applicable).
- Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
- 4. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 5. If 9-bit reception is desired, set the RX9 bit.
- 6. Enable reception by setting the CREN bit.
- 7. The RCIF interrupt flag bit will be set when a character is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
- 8. Read the RCSTA register to get the error flags and, if 9-bit data reception is enabled, the ninth data bit.
- 9. Get the received 8 Least Significant data bits from the receive buffer by reading the RCREG register.
- 10. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.

26.1.2.9 9-bit Address Detection Mode Set-up

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable:

- Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Section 26.3 "EUSART Baud Rate Generator (BRG)").
- 2. Clear the ANSEL bit for the RX pin (if applicable).
- Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
- If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 5. Enable 9-bit reception by setting the RX9 bit.
- 6. Enable address detection by setting the ADDEN bit.
- 7. Enable reception by setting the CREN bit.
- The RCIF interrupt flag bit will be set when a character with the ninth bit set is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
- 9. Read the RCSTA register to get the error flags. The ninth data bit will always be set.
- 10. Get the received 8 Least Significant data bits from the receive buffer by reading the RCREG register. Software determines if this is the device's address.
- 11. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.
- 12. If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and generate interrupts.



FIGURE 26-5: ASYNCHRONOUS RECEPTION

29.0 INSTRUCTION SET SUMMARY

Each PIC16 instruction is a 14-bit word containing the operation code (opcode) and all required operands. The op codes are broken into three broad categories.

- Byte Oriented
- · Bit Oriented
- Literal and Control

The literal and control category contains the most varied instruction word format.

Table 29-3 lists the instructions recognized by the MPASM $^{\rm TM}$ assembler.

All instructions are executed within a single instruction cycle, with the following exceptions, which may take two or three cycles:

- Subroutine takes two cycles (CALL, CALLW)
- Returns from interrupts or subroutines take two cycles (RETURN, RETLW, RETFIE)
- Program branching takes two cycles (GOTO, BRA, BRW, BTFSS, BTFSC, DECFSZ, INCSFZ)
- One additional instruction cycle will be used when any instruction references an indirect file register and the file select register is pointing to program memory.

One instruction cycle consists of 4 oscillator cycles; for an oscillator frequency of 4 MHz, this gives a nominal instruction execution rate of 1 MHz.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

29.1 Read-Modify-Write Operations

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

TABLE 29-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0 . It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.
n	FSR or INDF number. (0-1)
mm	Pre-post increment-decrement mode selection

TABLE 29-2: ABBREVIATION DESCRIPTIONS

Field	Description		
PC	Program Counter		
TO	Time-out bit		
С	Carry bit		
DC	Digit carry bit		
Z	Zero bit		
PD	Power-down bit		



FIGURE 30-18: SPI SLAVE MODE TIMING (CKE = 0)





Param. No.	Symbol	Characteristic		Min.	Max.	Units	Conditions
SP100*	Тнідн	Clock high time	100 kHz mode	4.0	—	μS	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	_	μS	Device must operate at a minimum of 10 MHz
			SSPx module	1.5Tcy			
SP101* TLOW	TLOW	Clock low time	100 kHz mode	4.7	-	μS	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	-	μS	Device must operate at a minimum of 10 MHz
			SSPx module	1.5Tcy	_	—	
SP102* Tr	TR	SDAx and SCLx rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1Св	300	ns	CB is specified to be from 10-400 pF
SP103*	TF	SDAx and SCLx fall	100 kHz mode	—	250	ns	
		time	400 kHz mode	20 + 0.1Св	250	ns	CB is specified to be from 10-400 pF
SP106*	THD:DAT	Data input hold time	100 kHz mode	0		ns	
		400 kHz mode	0	0.9	μS		
SP107*	SP107* TSU:DAT	Data input setup time	100 kHz mode	250		ns	(Note 2)
			400 kHz mode	100		ns	
SP109* TAA	ΤΑΑ	Output valid from clock	100 kHz mode	—	3500	ns	(Note 1)
			400 kHz mode	—		ns	
SP110* TBUF	TBUF	Bus free time	100 kHz mode	4.7		μS	Time the bus must be free
			400 kHz mode	1.3	—	μS	before a new transmission can start
SP111	Св	Bus capacitive loading		_	400	pF	

TABLE 30-16:	I ² C™ BUS DATA	REQUIREMENTS
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These parameters are characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCLx to avoid unintended generation of Start or Stop conditions.

2: A Fast mode (400 kHz) I²C[™] bus device can be used in a Standard mode (100 kHz) I²C bus system, but the requirement TsU:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the low period of the SCLx signal. If such a device does stretch the low period of the SCLx signal, it must output the next data bit to the SDAx line TR max. + TSU:DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification), before the SCLx line is released.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	x <u>/xx xxx</u>	Examples:
Device	Temperature Package Pattern Range	 a) PIC16F1826 - I/ML 301 = Industrial temp., QFN package, Extended VDD limits, QTP pattern #301. b) PIC16F1826 - I/P = Industrial temp., PDIP package, Extended VDD limits.
Device:	PIC16F1826 ⁽¹⁾ , PIC16F1827 ⁽¹⁾ , PIC16F1826T ⁽²⁾ , PIC16F1827T ⁽²⁾ ; VDD range 1.8V to 5.5V PIC16LF1826 ⁽¹⁾ , PIC16LF1827 ⁽¹⁾ , PIC16LF1826T ⁽²⁾ , PIC16LF1827T ⁽²⁾ ; VDD range 1.8V to 3.6V	 c) PIC16F1827 - E/SS= Extended temp., SSOP package, normal VDD limits.
Temperature Range:	I = -40° C to $+85^{\circ}$ C (Industrial) E = -40° C to $+125^{\circ}$ C (Extended)	
Package:	ML = Micro Lead Frame (QFN) 6x6 MV = Micro Lead Frame (UQFN) 4x4 P = Plastic DIP SO = SOIC SS = SSOP	Note 1: F = Wide Voltage Range LF = Standard Voltage Range 2: T = in tape and reel SOIC, SSOP, and QFN/UQFN packages only.
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)	