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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1827-i-ss

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3.2.1.1 STATUS Register

The STATUS register, shown in Register 3-1, contains:

- the arithmetic status of the ALU
- · the Reset status

'1' = Bit is set

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

REGISTER 3-1: STATUS: STATUS REGISTER

'0' = Bit is cleared

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS register as '000u uluu' (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (Refer to Section 29.0 "Instruction Set Summary").

Note 1: The <u>C and DC</u> bits operate as Borrow and Digit Borrow out bits, respectively, in subtraction.

U-0	U-0	U-0	R-1/q	R-1/q	R/W-0/u	R/W-0/u	R/W-0/u			
—	_	_	TO	PD	Z	DC ⁽¹⁾	C ⁽¹⁾			
bit 7		•				•	bit 0			
Legend:										
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'										
u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Rese										

q = Value depends on condition

bit 7-5	Unimplemented: Read as '0'
bit 4	TO: Time-out bit
	 1 = After power-up, CLRWDT instruction or SLEEP instruction 0 = A WDT time-out occurred
bit 3	PD: Power-down bit
	1 = After power-up or by the CLRWDT instruction
	0 = By execution of the SLEEP instruction
bit 2	Z: Zero bit
	 1 = The result of an arithmetic or logic operation is zero 0 = The result of an arithmetic or logic operation is not zero
bit 1	DC: Digit Carry/Digit Borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions) ⁽¹⁾
	 1 = A carry-out from the 4th low-order bit of the result occurred 0 = No carry-out from the 4th low-order bit of the result
bit 0	C: Carry/Borrow bit ⁽¹⁾ (ADDWF, ADDLW, SUBLW, SUBWF instructions) ⁽¹⁾
	1 = A carry-out from the Most Significant bit of the result occurred
	0 = No carry-out from the Most Significant bit of the result occurred
Note 1:	For Borrow, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high-order or low-order

bit of the source register.

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		-				(-	/			
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 8											
40Ch	—	Unimplemen	ted							_	_
40Dh	—	Unimplement	ted							_	_
40Eh	—	Unimplemen	ted							_	_
40Fh	—	Unimplemen	ted							_	_
410h	—	Unimplemen	ted							_	_
411h	—	Unimplemen	ted							_	_
412h	—	Unimplemen	ted							_	_
413h	—	Unimplemen	ted							_	_
414h	—	Unimplemen	ted							_	_
415h	TMR4 ⁽¹⁾	Timer4 Modu	ile Register							0000 0000	0000 0000
416h	PR4 ⁽¹⁾	Timer4 Perio	d Register							1111 1111	1111 1111
417h	T4CON ⁽¹⁾	_	T4OUTPS3	T4OUTPS2	T4OUTPS1	T4OUTPS0	TMR4ON	T4CKPS1	T4CKPS0	-000 0000	-000 0000
418h	—	Unimplemen	ted							_	_
419h	—	Unimplemen	ted							_	_
41Ah	—	Unimplemen	ted							_	_
41Bh	—	Unimplemen	ted							_	_
41Ch	TMR6 ⁽¹⁾	Timer6 Modu	ile Register							0000 0000	0000 0000
41Dh	PR6 ⁽¹⁾	Timer6 Perio	d Register							1111 1111	1111 1111
41Eh	T6CON ⁽¹⁾		T6OUTPS3	T6OUTPS2	T6OUTPS1	T6OUTPS0	TMR6ON	T6CKPS1	T6CKPS0	-000 0000	-000 0000
41Fh	_	Unimplement	ted	•	•	-				_	_

SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED) **TABLE 3-6:**

x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved. Shaded locations are unimplemented, read as '0'. Legend:

Note 1: PIC16(L)F1827 only.



3.4.2 OVERFLOW/UNDERFLOW RESET

If the STVREN bit in Configuration Word 2 is programmed to '1', the device will be reset if the stack is PUSHed beyond the sixteenth level or POPed beyond the first level, setting the appropriate bits (STKOVF or STKUNF, respectively) in the PCON register.

3.5 Indirect Addressing

The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the File Select Registers (FSR). If the FSRn address specifies one of the two INDFn registers, the read will return '0' and the write will not occur (though Status bits may be affected). The FSRn register value is created by the pair FSRnH and FSRnL.

The FSR registers form a 16-bit address that allows an addressing space with 65536 locations. These locations are divided into three memory regions:

- Traditional Data Memory
- Linear Data Memory
- Program Flash Memory

5.2.2 INTERNAL CLOCK SOURCES

The device may be configured to use the internal oscillator block as the system clock by performing one of the following actions:

- Program the FOSC<2:0> bits in Configuration Word 1 to select the INTOSC clock source, which will be used as the default system clock upon a device Reset.
- Write the SCS<1:0> bits in the OSCCON register to switch the system clock source to the internal oscillator during run-time. See **Section 5.3** "**Clock Switching**"for more information.

In **INTOSC** mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT is available for general purpose I/O or CLKOUT.

The function of the OSC2/CLKOUT pin is determined by the state of the $\overline{\text{CLKOUTEN}}$ bit in Configuration Word 1.

The internal oscillator block has two independent oscillators and a dedicated Phase-Lock Loop, HFPLL that can produce one of three internal system clock sources.

- 1. The **HFINTOSC** (High-Frequency Internal Oscillator) is factory calibrated and operates at 16 MHz. The HFINTOSC source is generated from the 500 kHz MFINTOSC source and the dedicated Phase-Lock Loop, HFPLL. The frequency of the HFINTOSC can be user-adjusted via software using the OSCTUNE register (Register 5-3).
- The MFINTOSC (Medium-Frequency Internal Oscillator) is factory calibrated and operates at 500 kHz. The frequency of the MFINTOSC can be user-adjusted via software using the OSCTUNE register (Register 5-3).
- 3. The **LFINTOSC** (Low-Frequency Internal Oscillator) is uncalibrated and operates at 31 kHz.

5.2.2.1 HFINTOSC

The High-Frequency Internal Oscillator (HFINTOSC) is a factory calibrated 16 MHz internal clock source. The frequency of the HFINTOSC can be altered via software using the OSCTUNE register (Register 5-3).

The output of the HFINTOSC connects to a postscaler and multiplexer (see Figure 5-1). One of nine frequencies derived from the HFINTOSC can be selected via software using the IRCF<3:0> bits of the OSCCON register. See **Section 5.2.2.7** "Internal Oscillator Clock Switch Timing" for more information.

The HFINTOSC is enabled by:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired HF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to '1x'.

The High Frequency Internal Oscillator Ready bit (HFIOFR) of the OSCSTAT register indicates when the HFINTOSC is running and can be utilized.

The High Frequency Internal Oscillator Status Locked bit (HFIOFL) of the OSCSTAT register indicates when the HFINTOSC is running within 2% of its final value.

The High Frequency Internal Oscillator Status Stable bit (HFIOFS) of the OSCSTAT register indicates when the HFINTOSC is running within 0.5% of its final value.

5.2.2.2 MFINTOSC

The Medium-Frequency Internal Oscillator (MFINTOSC) is a factory calibrated 500 kHz internal clock source. The frequency of the MFINTOSC can be altered via software using the OSCTUNE register (Register 5-3).

The output of the MFINTOSC connects to a postscaler and multiplexer (see Figure 5-1). One of nine frequencies derived from the MFINTOSC can be selected via software using the IRCF<3:0> bits of the OSCCON register. See **Section 5.2.2.7** "Internal Oscillator Clock Switch Timing" for more information.

The MFINTOSC is enabled by:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired HF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to '1x'

The Medium Frequency Internal Oscillator Ready bit (MFIOFR) of the OSCSTAT register indicates when the MFINTOSC is running and can be utilized.

5.2.2.6 32 MHz Internal Oscillator Frequency Selection

The Internal Oscillator Block can be used with the 4X PLL associated with the External Oscillator Block to produce a 32 MHz internal system clock source. The following settings are required to use the 32 MHz internal clock source:

- The FOSC bits in Configuration Word 1 must be set to use the INTOSC source as the device system clock (FOSC<2:0> = 100).
- The SCS bits in the OSCCON register must be cleared to use the clock determined by FOSC<2:0> in Configuration Word 1 (SCS<1:0> = 00).
- The IRCF bits in the OSCCON register must be set to the 8 MHz HFINTOSC set to use (IRCF<3:0> = 1110).
- The SPLLEN bit in the OSCCON register must be set to enable the 4xPLL, or the PLLEN bit of the Configuration Word 2 must be programmed to a '1'.
- Note: When using the PLLEN bit of the Configuration Word 2, the 4xPLL cannot be disabled by software and the 8 MHz HFINTOSC option will no longer be available.

The 4xPLL is not available for use with the internal oscillator when the SCS bits of the OSCCON register are set to '1x'. The SCS bits must be set to '00' to use the 4xPLL with the internal oscillator.

5.2.2.7 Internal Oscillator Clock Switch Timing

When switching between the HFINTOSC, MFINTOSC and the LFINTOSC, the new oscillator may already be shut down to save power (see Figure 5-7). If this is the case, there is a delay after the IRCF<3:0> bits of the OSCCON register are modified before the frequency selection takes place. The OSCSTAT register will reflect the current active status of the HFINTOSC, MFINTOSC and LFINTOSC oscillators. The sequence of a frequency selection is as follows:

- 1. IRCF<3:0> bits of the OSCCON register are modified.
- 2. If the new clock is shut down, a clock start-up delay is started.
- 3. Clock switch circuitry waits for a falling edge of the current clock.
- 4. The current clock is held low and the clock switch circuitry waits for a rising edge in the new clock.
- 5. The new clock is now active.
- 6. The OSCSTAT register is updated as required.
- 7. Clock switch is complete.

See Figure 5-7 for more details.

If the internal oscillator speed is switched between two clocks of the same source, there is no start-up delay before the new frequency is selected. Clock switching time delays are shown in Table 5-1.

Start-up delay specifications are located in the oscillator tables of **Section 30.0** "**Electrical Specifications**".

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8.6.9 PIR4 REGISTER⁽¹⁾

The PIR4 register contains the interrupt flag bits, as shown in Register 8-9.

- **Note 1:** The PIR4 register is available only on the PIC16(L)F1827 device.
 - 2: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 8-9: PIR4: PERIPHERAL INTERRUPT REQUEST REGISTER 4⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	R/W/HS-0/0	R/W/HS-0/0
—	—	—	—	—	—	BCL2IF	SSP2IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Bit is set by hardware

bit 7-2	Unimplemented: Read as '0'
bit 1	BCL2IF: MSSP2 Bus Collision Interrupt Flag bit
	1 = A Bus Collision was detected (must be cleared in software)0 = No Bus collision was detected
bit 0	 SSP2IF: Master Synchronous Serial Port 2 (MSSP2) Interrupt Flag bit 1 = The Transmission/Reception/Bus Condition is complete (must be cleared in software) 0 = Waiting to Transmit/Receive/Bus Condition in progress

Note 1: This register is only available on PIC16(L)F1827.

TABLE 8-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	86
OPTION_REG	WPUEN	INTEDG	TMR0CS	TMR0SE	PSA	PS2	PS1	PS0	177
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	87
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	—	_	CCP2IE ⁽¹⁾	88
PIE3 ⁽¹⁾	_	_	CCP4IE	CCP3IE	TMR6IE	_	TMR4IE	_	89
PIE4 ⁽¹⁾	_	_	_	_	-	_	BCL2IE	SSP2IE	90
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	91
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	—	—	CCP2IF ⁽¹⁾	92
PIR3 ⁽¹⁾	_	_	CCP4IF	CCP3IF	TMR6IF	_	TMR4IF	_	93
PIR4 ⁽¹⁾	_	_	_	_	_	_	BCL2IF	SSP2IF	94

Legend: — = unimplemented locations read as '0'. Shaded cells are not used by Interrupts.

Note 1: PIC16(L)F1827 only.

EXAMPLE 11-2: DATA EEPROM WRITE

		BANKSEL	EEADRL		i
		MOVLW	DATA_EE_	_ADDR	i
		MOVWF	EEADRL		;Data Memory Address to write
		MOVLW	DATA_EE_	_DATA	i
		MOVWF	EEDATL		;Data Memory Value to write
		BCF	EECON1,	CFGS	;Deselect Configuration space
		BCF	EECON1,	EEPGD	;Point to DATA memory
		BSF	EECON1,	WREN	;Enable writes
		BCF	INTCON,	GIE	;Disable INTs.
ſ		MOVLW	55h		;
	e e	MOVWF	EECON2		;Write 55h
	luire	MOVLW	0AAh		;
	equ	MOVWF	EECON2		;Write AAh
	чs	BSF	EECON1,	WR	;Set WR bit to begin write
		BSF	INTCON,	GIE	;Enable Interrupts
		BCF	EECON1,	WREN	;Disable writes
		BTFSC	EECON1,	WR	;Wait for write to complete
		GOTO	\$-2		;Done

REGISTER 11-6: EECON2	: EEPROM CO	ONTROL 2 REGISTER	2
-----------------------	-------------	-------------------	---

W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0
			EEPROM Co	ontrol Register 2	2		
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable	bit	U = Unimplen	nented bit, read	l as '0'	
S = Bit can only	y be set	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	R/Value at all o	other Resets
'1' = Bit is set		'0' = Bit is cle	ared				

bit 7-0 Data EEPROM Unlock Pattern bits

To unlock writes, a 55h must be written first, followed by an AAh, before setting the WR bit of the EECON1 register. The value written to this register is used to unlock the writes. There are specific timing requirements on these writes. Refer to **Section 11.2.2** "Writing to the Data EEPROM Memory" for more information.

TABLE 11-3: SUMMARY OF REGISTERS ASSOCIATED WITH DATA EEPROM

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
EECON1	EEPGD	CFGS	LWLO	FREE	WRERR	WREN	WR	RD	115
EECON2	EEPROM	Control Reg	ister 2 (not a	a physical re	egister)				101*
EEADRL	EEADRL7	EEADRL6	EEADRL5	EEADRL4	EEADRL3	EEADRL2	EEADRL1	EEADRL0	113
EEADRH	—	EEADRH6	EEADRH5	EEADRH4	EEADRH3	EEADRH2	EEADRH1	EEADRH0	114
EEDATL	EEDATL7	EEDATL6	EEDATL5	EEDATL4	EEDATL3	EEDATL2	EEDALT1	EEDATL0	113
EEDATH	_	_	EEDATH5	EEDATH4	EEDATH3	EEDATH2	EEDATH1	EEDATH0	113
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	91
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	—	—	CCP2IE	93
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	_	_	CCP2IF	97

Legend: — = unimplemented read as '0'. Shaded cells are not used by data EEPROM module.

* Page provides register information.

19.2 Comparator Control

Each comparator has 2 control registers: CMxCON0 and CMxCON1.

The CMxCON0 registers (see Register 19-1) contain Control and Status bits for the following:

- Enable
- · Output selection
- Output polarity
- · Speed/Power selection
- · Hysteresis enable
- · Output synchronization

The CMxCON1 registers (see Register 19-2) contain Control bits for the following:

- · Interrupt enable
- · Interrupt edge polarity
- · Positive input channel selection
- Negative input channel selection

19.2.1 COMPARATOR ENABLE

Setting the CxON bit of the CMxCON0 register enables the comparator for operation. Clearing the CxON bit disables the comparator resulting in minimum current consumption.

19.2.2 COMPARATOR OUTPUT SELECTION

The output of the comparator can be monitored by reading either the CxOUT bit of the CMxCON0 register or the MCxOUT bit of the CMOUT register. In order to make the output available for an external connection, the following conditions must be true:

- · CxOE bit of the CMxCON0 register must be set
- · Corresponding TRIS bit must be cleared
- · CxON bit of the CMxCON0 register must be set

Note 1:	The CxOE bit of the CMxCON0 register
	overrides the PORT data latch. Setting
	the CxON bit of the CMxCON0 register
	has no impact on the port override.

2: The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched.

19.2.3 COMPARATOR OUTPUT POLARITY

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CxPOL bit of the CMxCON0 register. Clearing the CxPOL bit results in a non-inverted output.

Table 19-1 shows the output state versus input conditions, including polarity control.

TABLE 19-1: COMPARATOR OUTPUT STATE VS. INPUT CONDITIONS

Input Condition	CxPOL	CxOUT
CxVN > CxVP	0	0
CxVN < CxVP	0	1
CxVN > CxVP	1	1
CxVN < CxVP	1	0

19.2.4 COMPARATOR SPEED/POWER SELECTION

The trade-off between speed or power can be optimized during program execution with the CxSP control bit. The default state for this bit is '1' which selects the normal speed mode. Device power consumption can be optimized at the cost of slower comparator propagation delay by clearing the CxSP bit to '0'.

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
C4TSEL<1:0>		C3TSEL<1:0>		C2TSEL<1:0>		C1TSEL<1:0>	
bit 7							bit 0
r							
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimpler	nented bit, read	l as '0'	
u = Bit is unch	nanged	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	R/Value at all o	other Resets
'1' = Bit is set		'0' = Bit is clea	ared				
bit 7-6	C4TSEL<1:0 00 =CCP4 is 01 =CCP4 is 10 =CCP4 is 11 =Reserve	CCP4 Timer based off Time based off Time based off Time d	⁻ Selection er 2 in PWM M er 4 in PWM M er 6 in PWM M	ode ode ode			
bit 5-4	C3TSEL<1:0 00 =CCP3 is 01 =CCP3 is 10 =CCP3 is 11 =Reserve	 CCP3 Timer based off Time based off Time based off Time d 	Selection er 2 in PWM M er 4 in PWM M er 6 in PWM M	ode ode ode			
bit 3-2	C2TSEL<1:0 00 =CCP2 is 01 =CCP2 is 10 =CCP2 is 11 =Reserve	CCP2 Timer based off Time based off Time based off Time d	Selection er 2 in PWM M er 4 in PWM M er 6 in PWM M	ode ode ode			
bit 1-0	C1TSEL<1:0 00 =CCP1 is 01 =CCP1 is 10 =CCP1 is 11 =Reserve	CCP1 Timer based off Time based off Time based off Time d	Selection er 2 in PWM M er 4 in PWM M er 6 in PWM M	ode ode ode			

REGISTER 24-2: CCPTMRS: PWM TIMER SELECTION CONTROL REGISTER

25.5.3 SLAVE TRANSMISSION

When the R/\overline{W} bit of the incoming address byte is set and an address match occurs, the R/\overline{W} bit of the SSPxSTAT register is set. The received address is loaded into the SSPxBUF register, and an ACK pulse is sent by the slave on the ninth bit.

Following the ACK, slave hardware clears the CKP bit and the SCLx pin is held low (see **Section 25.5.6** "**Clock Stretching**" for more detail). By stretching the clock, the master will be unable to assert another clock pulse until the slave is done preparing the transmit data.

The transmit data must be loaded into the SSPxBUF register which also loads the SSPxSR register. Then the SCLx pin should be released by setting the CKP bit of the SSPxCON1 register. The eight data bits are shifted out on the falling edge of the SCLx input. This ensures that the SDAx signal is valid during the SCLx high time.

The ACK pulse from the master-receiver is latched on the rising edge of the ninth SCLx input pulse. This ACK value is copied to the ACKSTAT bit of the SSPxCON2 register. If ACKSTAT is set (not ACK), then the data transfer is complete. In this case, when the not ACK is latched by the slave, the slave goes Idle and waits for another occurrence of the Start bit. If the SDAx line was low (ACK), the next transmit data must be loaded into the SSPxBUF register. Again, the SCLx pin must be released by setting bit CKP.

An MSSPx interrupt is generated for each data transfer byte. The SSPxIF bit must be cleared by software and the SSPxSTAT register is used to determine the status of the byte. The SSPxIF bit is set on the falling edge of the ninth clock pulse.

25.5.3.1 Slave Mode Bus Collision

A slave receives a Read request and begins shifting data out on the SDAx line. If a bus collision is detected and the SBCDE bit of the SSPxCON3 register is set, the BCLxIF bit of the PIRx register is set. Once a bus collision is detected, the slave goes Idle and waits to be addressed again. User software can use the BCLxIF bit to handle a slave bus collision.

25.5.3.2 7-bit Transmission

A master device can transmit a read request to a slave, and then clock data out of the slave. The list below outlines what software for a slave will need to do to accomplish a standard transmission. Figure 25-17 can be used as a reference to this list.

- 1. Master sends a Start condition on SDAx and SCLx.
- 2. S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
- Matching address with R/W bit set is received by the Slave setting SSPxIF bit.
- 4. Slave hardware generates an ACK and sets SSPxIF.
- 5. SSPxIF bit is cleared by user.
- 6. Software reads the received address from SSPxBUF, clearing BF.
- 7. R/\overline{W} is set so CKP was automatically cleared after the ACK.
- 8. The slave software loads the transmit data into SSPxBUF.
- 9. CKP bit is set releasing SCLx, allowing the master to clock the data out of the slave.
- 10. SSPxIF is set after the ACK response from the master is loaded into the ACKSTAT register.
- 11. SSPxIF bit is cleared.
- 12. The slave software checks the ACKSTAT bit to see if the master wants to clock out more data.
 - **Note 1:** If the master ACKs the clock will be stretched.
 - ACKSTAT is the only bit updated on the rising edge of SCLx (9th) rather than the falling.
- 13. Steps 9-13 are repeated for each transmitted byte.
- 14. If the master sends a not ACK; the clock is not held, but SSPxIF is still set.
- 15. The master sends a Restart condition or a Stop.
- 16. The slave is no longer addressed.

26.1.2.8 Asynchronous Reception Set-up:

- Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Section 26.3 "EUSART Baud Rate Generator (BRG)").
- 2. Clear the ANSEL bit for the RX pin (if applicable).
- Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
- 4. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 5. If 9-bit reception is desired, set the RX9 bit.
- 6. Enable reception by setting the CREN bit.
- 7. The RCIF interrupt flag bit will be set when a character is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
- 8. Read the RCSTA register to get the error flags and, if 9-bit data reception is enabled, the ninth data bit.
- 9. Get the received 8 Least Significant data bits from the receive buffer by reading the RCREG register.
- 10. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.

26.1.2.9 9-bit Address Detection Mode Set-up

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable:

- Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Section 26.3 "EUSART Baud Rate Generator (BRG)").
- 2. Clear the ANSEL bit for the RX pin (if applicable).
- Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
- If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 5. Enable 9-bit reception by setting the RX9 bit.
- 6. Enable address detection by setting the ADDEN bit.
- 7. Enable reception by setting the CREN bit.
- The RCIF interrupt flag bit will be set when a character with the ninth bit set is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
- 9. Read the RCSTA register to get the error flags. The ninth data bit will always be set.
- 10. Get the received 8 Least Significant data bits from the receive buffer by reading the RCREG register. Software determines if this is the device's address.
- 11. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.
- 12. If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and generate interrupts.



FIGURE 26-5: ASYNCHRONOUS RECEPTION

PIC16(L)F1826/27

NOTES:

Mnemonic,		Description	Qualas	14-Bit Opcode)	Status	Neter	
Oper	rands	Description	Cycles	MSb			LSb	Affected	Notes	
BYTE-ORIENTED FILE REGISTER OPERATIONS										
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C, DC, Z	2	
ADDWFC	f, d	Add with Carry W and f	1	11	1101	dfff	ffff	C, DC, Z	2	
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	2	
ASRF	f, d	Arithmetic Right Shift	1	11	0111	dfff	ffff	C, Z	2	
LSLF	f, d	Logical Left Shift	1	11	0101	dfff	ffff	C, Z	2	
LSRF	f, d	Logical Right Shift	1	11	0110	dfff	ffff	C, Z	2	
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2	
CLRW	_	Clear W	1	00	0001	0000	00xx	Z		
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	2	
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	2	
INCF	f. d	Increment f	1	00	1010	dfff	ffff	z	2	
IORWE	f. d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	2	
MOVE	fd	Move f	1	00	1000	dfff	ffff	7	2	
MOVWE	., ⊆ f	Move W to f	1	00	0000	1fff	ffff	-	2	
RIF	fd	Rotate Left f through Carry	1	00	1101	dfff	ffff	С	2	
RRF	f d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	2	
SUBWE	f d	Subtract W from f	1	00	0010	dfff	ffff		2	
SUBWEB	fd	Subtract with Borrow W from f	1	11	1011	dfff	ffff	C DC Z	2	
SWAPE	f d	Swan nibbles in f	1	00	1110	dfff	ffff	0, 00, 2	2	
XORWE	f d	Exclusive OR W with f	1	00	0110	dfff	ffff	7	2	
									2	
	fd	Decrement f Skin if 0			1011	4fff	<i>f f f f f f f f f f </i>		1 2	
DECFSZ	r, u f d	Increment f. Skip if 0	1(2)	00	1111	JEEE			1, 2	
INCFSZ	1, u		1(2)	00		aiii	IIII		1, 2	
		BIT-ORIENTED FILE REGIST	ER OPER	RATION	IS					
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		2	
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		2	
	1	BIT-ORIENTED SKIP O	PERATIO	NS						
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		1, 2	
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		1, 2	
LITERAL OPERATIONS										
ADDLW	k	Add literal and W	1	11	1110	kkkk	kkkk	C, DC, Z		
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z		
MOVLB	k	Move literal to BSR	1	00	0000	001k	kkkk			
MOVLP	k	Move literal to PCLATH	1	11	0001	1kkk	kkkk			
MOVLW	k	Move literal to W	1	11	0000	kkkk	kkkk			
SUBLW	k	Subtract W from literal	1	11	1100	kkkk	kkkk	C, DC, Z		
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z		
L			ı							

TABLE 29-3: PIC16(L)F1826/27 ENHANCED INSTRUCTION SET

Note 1:If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

2: If this instruction addresses an INDF register and the MSb of the corresponding FSR is set, this instruction will require one additional instruction cycle.



FIGURE 30-4: POR AND POR REARM WITH SLOW RISING VDD

30.3 DC Characteristics: PIC16(L)F1826/27-I/E (Power-Down)

PIC16LF1826/27			Standard Operating Conditions (Operating temperature $-40^{\circ}C \leq -40^{\circ}C < -40^$				s (unless otherwise stated) $C \le TA \le +85^{\circ}C$ for industrial $C \le TA \le +125^{\circ}C$ for extended			
PIC16F1826/27			Standard Operating Cond Operating temperature			itions (unless otherwise stated) -40°C \leq TA \leq +85°C for industrial -40°C \leq TA \leq +125°C for extended				
Param	ram Dovice Characteristics Mi		Typt	Max.	Max.	Units		Conditions		
No.	Device Unaracteristics		וקעי	+85°C	+125°C	onita	VDD	Note		
Power-down Base Current (IPD) ⁽²⁾										
D022			0.02	1.0	4.0	μA	1.8	WDT, BOR, FVR, and T1OSC		
			0.03	1.1	7.0	μA	3.0	disabled, all Peripherals Inactive		
D022		_	15	35	50	μA	1.8	WDT, BOR, FVR, and T1OSC		
		_	18	40	60	μA	3.0	disabled, all Peripherals Inactive		
		—	19	45	70	μA	5.0			
D023			0.5	1.1	5.0	μA	1.8	LPWDT Current (Note 1)		
			0.8	2.0	8.0	μA	3.0			
D023		—	16	35	50	μA	1.8	LPWDT Current (Note 1)		
			19	40	60	μA	3.0			
		—	20	45	70	μA	5.0			
D023A			8.5	23	32	μA	1.8	FVR current (Note 1)		
		—	8.5	26	40	μA	3.0			
D023A			32	62	66	μA	1.8	FVR current (Note 1)		
			39	70	80	μA	3.0			
			70	110	120	μA	5.0			
D024			8.1	14	20	μA	3.0	BOR Current (Note 1)		
D024		_	34	57	70	μA	3.0	BOR Current (Note 1)		
		_	67	100	115	μA	5.0			
D025			0.6	1.5	5.0	μA	1.8	T1OSC Current (Note 1)		
		—	0.8	2.5	8.0	μA	3.0			
D025			16	35	50	μA	1.8	T1OSC Current (Note 1)		
			21	40	60	μA	3.0			
		—	25	45	70	μA	5.0			
D026			0.1	1.1	5.0	μA	1.8	A/D Current (Note 1, Note 3), no		
			0.1	2.0	8.0	μA	3.0	conversion in progress		
D026		_	16	35	50	μA	1.8	A/D Current (Note 1, Note 3), no		
		_	21	40	60	μA	3.0	conversion in progress		
		_	25	45	70	μA	5.0			

These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral △ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins set to inputs state and tied to VDD.

3: A/D oscillator source is FRC.

30.4 DC Characteristics: PIC16(L)F1826/27-I/E

DC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions (unless otherwise stated)} \\ \mbox{Operating temperature -40°C \leq TA \leq +85°C for industrial} \\ \mbox{-40°C \leq TA \leq +125°C for extended} \end{array}$								
Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions				
	VIL	Input Low Voltage									
		I/O PORT:									
D030		with TTL buffer	_	_	0.8	V	$4.5V \leq V\text{DD} \leq 5.5V$				
D030A			_	_	0.15 VDD	V	$1.8V \leq V\text{DD} \leq 4.5V$				
D031		with Schmitt Trigger buffer	_	_	0.2 VDD	V	$2.0V \leq V\text{DD} \leq 5.5V$				
		with I ² C™ levels		_	0.3 VDD	V					
		with SMBus™ levels	_	_	0.8	V	$2.7V \le VDD \le 5.5V$				
D032		MCLR, OSC1 (RC mode) ⁽¹⁾	_	_	0.2 VDD	V					
D033		OSC1 (HS mode)		_	0.3 VDD	V					
	VIH	Input High Voltage	ļI								
		I/O ports:		_	_						
D040		with TTL buffer	2.0	_	_	V	$4.5V \le VDD \le 5.5V$				
D040A			0.25 VDD + 0.8	_	-	V	$1.8V \leq V\text{DD} \leq 4.5V$				
D041		with Schmitt Trigger buffer	0.8 VDD	_	_	V	$2.0V \le VDD \le 5.5V$				
		with I ² C™ levels	0.7 Vdd	_	_	V					
		with SMBus™ levels	2.1	_	_	V	$2.7V \le VDD \le 5.5V$				
D042		MCLR	0.8 VDD	_	_	V					
D043A		OSC1 (HS mode)	0.7 VDD	_	_	V					
D043B		OSC1 (RC mode)	0.9 Vdd	_	_	V	(Note 1)				
	lı∟	Input Leakage Current ⁽²⁾									
D060		I/O ports	—	± 5	± 100	nA	Vss ≤ VPIN ≤ VDD, Pin at high- impedance at 85°C				
D 004		<u></u>		± 5	± 1000	nA	125°C				
D061		MCLR ⁽⁹⁾	—	± 50	± 200	nA	VSS \leq VPIN \leq VDD at 85°C				
D070*	IPUR	weak Pull-up Current	05	100	000						
D070^			25 25	100	200		VDD = 3.3V, VPIN = VSS				
	Voi		25	140	500	μΛ	VDD - 5.00, VFIN - V33				
080	VOL				T		loi = 8mA $VDD = 5V$				
DUUU				_	0.6	V	OL = 6mA, VDD = 3.3V				
							IOL = 1.8mA, VDD = 1.8V				
	Voн	Output High Voltage ⁽⁴⁾									
D090		I/O ports	Vdd - 0.7	_	_	V	IOH = 3.5mA, VDD = 5V IOH = 3mA, VDD = 3.3V IOH = 1mA, VDD = 1.8V				
		Capacitive Loading Specs on	Output Pins		·		•				
D101*	COSC2	OSC2 pin	—	_	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1				
D101A*	Сю	All I/O pins	—	_	50	pF					
*	These					-	•				

These parameters are characterized but not tested.

Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are † not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: Including OSC2 in CLKOUT mode.

32.0 DEVELOPMENT SUPPORT

The PIC[®] microcontrollers and dsPIC[®] digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
- MPLAB[®] IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB C Compiler for Various Device Families
 - HI-TECH C for Various Device Families
 - MPASM[™] Assembler
 - MPLINK[™] Object Linker/ MPLIB[™] Object Librarian
 - MPLAB Assembler/Linker/Librarian for Various Device Families
- · Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
 - MPLAB ICD 3
 - PICkit™ 3 Debug Express
- Device Programmers
 - PICkit[™] 2 Programmer
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

32.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows[®] operating system-based application that contains:

- A single graphical interface to all debugging tools
 - Simulator
 - Programmer (sold separately)
 - In-Circuit Emulator (sold separately)
 - In-Circuit Debugger (sold separately)
- · A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- · High-level source code debugging
- · Mouse over variable inspection
- Drag and drop variables from source to watch windows
- · Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- · Debug using:
 - Source files (C or assembly)
 - Mixed C and assembly
 - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

28-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-152A Sheet 1 of 2

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