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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	6
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	A/D 4x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24123a-24sxit

Getting Started

For in depth information, along with detailed programming details, see the PSoC® Technical Reference Manual.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

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Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to the CYPros Consultants web site.

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Technical Support

Technical support – including a searchable knowledge base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Pinouts

This section describes, lists, and illustrates the CY8C24x23A PSoC device pins and pinout configurations. Every port pin (labeled with a “P”) is capable of digital I/O. However, V_{SS}, V_{DD}, SMP, and XRES are not capable of digital I/O.

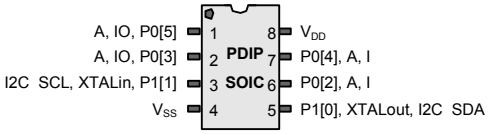
8-Pin Part Pinout

Table 2. 8-Pin PDIP and SOIC

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I/O	P0[5]	Analog column mux input and column output
2	I/O	I/O	P0[3]	Analog column mux input and column output
3	I/O		P1[1]	Crystal input (XTALin), I^2C serial clock (SCL), ISSP-SCLK[4]
4	Power		V_{SS}	Ground connection
5	I/O		P1[0]	Crystal output (XTALout), I^2C serial data (SDA), ISSP-SDATA[4]
6	I/O	I	P0[2]	Analog column mux input
7	I/O	I	P0[4]	Analog column mux input
8	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 4. CY8C24123A 8-Pin PSoC Device



Note
4. These are the ISSP pins, which are not high Z at POR. See the PSoC Technical Reference Manual for details.

Table 0-1. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASC10CR0	80	RW		C0	
PRT0DM1	01	RW		41		ASC10CR1	81	RW		C1	
PRT0IC0	02	RW		42		ASC10CR2	82	RW		C2	
PRT0IC1	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DM0	04	RW		44		ASD11CR0	84	RW		C4	
PRT1DM1	05	RW		45		ASD11CR1	85	RW		C5	
PRT1IC0	06	RW		46		ASD11CR2	86	RW		C6	
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50		ASD20CR0	90	RW	GDI_O_IN	D0	RW
	11			51		ASD20CR1	91	RW	GDI_E_IN	D1	RW
	12			52		ASD20CR2	92	RW	GDI_O_OU	D2	RW
	13			53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW		D6	
	17			57		ASC21CR3	97	RW		D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW		6C			AC			EC	
DCB03IN	2D	RW		6D			AD			ED	
DCB03OU	2E	RW		6E			AE			EE	
	2F			6F			AF			EF	
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. # Access is bit specific.

DC Operational Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

The operational amplifier is a component of both the analog continuous time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the analog continuous time PSoC block. Typical parameters are measured at 5 V at 25 °C and are for design guidance only.

Table 14. 5-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 1.6 1.3 1.2	 10 8 7.5	 mV mV mV	
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	20	–	pA	Gross tested to 1 µA
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range Common mode voltage range (high power or high Opamp bias)	0.0 0.5	– –	V_{DD} V_{DD} – 0.5	V	The common mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 60 60 80	 – – –	 – – –	 dB dB dB	Specification is applicable at high Opamp bias. For low Opamp bias mode, minimum is 60 dB.
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.5	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 0.2 0.2 0.5	 V V V	
I_{SOA}	Supply current (including associated AGND buffer) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – – – –	 150 300 600 1200 2400 4600	 200 400 800 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply voltage rejection ratio	64	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$

Table 15. 3.3-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 1.65 1.32 –	 10 8 –	 mV mV mV	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	20	–	pA	Gross tested to 1 µA
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0.2	–	V_{DD} – 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain Power = low, ppamp Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 60 60 80	 – – –	 – – –	 dB dB dB	Specification is applicable at low Opamp bias. For high Opamp bias mode (except high power, high Opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.2	 – – –	 – – –	 V V V	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, ppamp Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 – – –	 – – –	 0.2 0.2 0.2	 V V V	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
I_{SOA}	Supply current (including associated AGND buffer) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – – – –	 150 300 600 1200 2400 –	 200 400 800 1600 3200 –	 µA µA µA µA µA µA	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
$PSRR_{OA}$	Supply voltage rejection ratio	64	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$

DC Analog Output Buffer Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 18. 5-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (absolute value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	µV/°C	
V_{CMOB}	Common mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 1 1	 – –	 W W	
$V_{OHIGHOB}$	High output voltage swing (Load = 32 ohms to $V_{DD/2}$) Power = low Power = high	 0.5 × V_{DD} + 1.1 0.5 × V_{DD} + 1.1	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 32 ohms to $V_{DD/2}$) Power = low Power = high	 – –	 – –	 .5 × V_{DD} – 1.3 0.5 × V_{DD} – 1.3	 V V	
I_{SOB}	Supply current including Opamp bias cell (No Load) Power = low Power = high	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	52	64	–	dB	V_{OUT} > (V_{DD} – 1.25)

Table 19. 3.3-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (absolute value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	µV/°C	
V_{CMOB}	Common mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (Load = 1 K ohms to $V_{DD/2}$) Power = low Power = high	 0.5 × V_{DD} + 1.0 0.5 × V_{DD} + 1.0	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 1 K ohms to $V_{DD/2}$) Power = low Power = high	 – –	 – –	 0.5 × V_{DD} – 1.0 0.5 × V_{DD} – 1.0	 V V	
I_{SOB}	Supply current including Opamp bias cell (no load) Power = low Power = high	 – –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	52	64	–	dB	V_{OUT} > (V_{DD} – 1.25)

DC Analog Reference Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

The guaranteed specifications for RefHI and RefLo are measured through the Analog Continuous Time PSoC blocks. The power levels for RefHi and RefLo refer to the Analog Reference Control register. AGND is measured at P2[4] in AGND bypass mode. Each Analog Continuous Time PSoC block adds a maximum of 10 mV additional offset error to guaranteed AGND specifications from the local AGND buffer. Reference control power can be set to medium or high unless otherwise noted.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the analog reference. Some coupling of the digital signal may appear on the AGND.

Table 22. 5-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.136	$V_{DD}/2$ + 1.288	$V_{DD}/2$ + 1.409	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.138	$V_{DD}/2$ + 0.003	$V_{DD}/2$ + 0.132	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.417	$V_{DD}/2$ – 1.289	$V_{DD}/2$ – 1.154	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.202	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.358	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.055	$V_{DD}/2$ + 0.001	$V_{DD}/2$ + 0.055	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.369	$V_{DD}/2$ – 1.295	$V_{DD}/2$ – 1.218	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.211	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.357	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.055	$V_{DD}/2$	$V_{DD}/2$ + 0.052	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.368	$V_{DD}/2$ – 1.298	$V_{DD}/2$ – 1.224	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.215	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.353	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.040	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.033	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.368	$V_{DD}/2$ – 1.299	$V_{DD}/2$ – 1.225	V
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.076	P2[4] + P2[6] – 0.021	P2[4] + P2[6] + 0.041	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.025	P2[4] – P2[6] + 0.011	P2[4] – P2[6] + 0.085	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.069	P2[4] + P2[6] – 0.014	P2[4] + P2[6] + 0.043	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.029	P2[4] – P2[6] + 0.005	P2[4] – P2[6] + 0.052	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.072	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.048	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.031	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.057	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.070	P2[4] + P2[6] – 0.009	P2[4] + P2[6] + 0.047	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.033	P2[4] – P2[6] + 0.001	P2[4] – P2[6] + 0.039	V

Table 22. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b101	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.228	P2[4] + 1.284	P2[4] + 1.332	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.358	P2[4] – 1.293	P2[4] – 1.226	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.236	P2[4] + 1.289	P2[4] + 1.332	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.357	P2[4] – 1.297	P2[4] – 1.229	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.237	P2[4] + 1.291	P2[4] + 1.337	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.356	P2[4] – 1.299	P2[4] – 1.232	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.237	P2[4] + 1.292	P2[4] + 1.337	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.357	P2[4] – 1.300	P2[4] – 1.233	V
0b110	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.512	2.594	2.654	V
		V_{AGND}	AGND	Bandgap	1.250	1.303	1.346	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.011	V_{SS} + 0.027	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.515	2.592	2.654	V
		V_{AGND}	AGND	Bandgap	1.253	1.301	1.340	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.02	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.518	2.593	2.651	V
		V_{AGND}	AGND	Bandgap	1.254	1.301	1.338	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.017	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.517	2.594	2.650	V
		V_{AGND}	AGND	Bandgap	1.255	1.300	1.337	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.015	V
0b111	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	3.2 × Bandgap	4.011	4.143	4.203	V
		V_{AGND}	AGND	1.6 × Bandgap	2.020	2.075	2.118	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.011	V_{SS} + 0.026	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	3.2 × Bandgap	4.022	4.138	4.203	V
		V_{AGND}	AGND	1.6 × Bandgap	2.023	2.075	2.114	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.017	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	3.2 × Bandgap	4.026	4.141	4.207	V
		V_{AGND}	AGND	1.6 × Bandgap	2.024	2.075	2.114	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.015	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	3.2 × Bandgap	4.030	4.143	4.206	V
		V_{AGND}	AGND	1.6 × Bandgap	2.024	2.076	2.112	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.013	V

Table 23. 3.3-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2 + 1.170$	$V_{DD}/2 + 1.288$	$V_{DD}/2 + 1.376$	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.098$	$V_{DD}/2 + 0.003$	$V_{DD}/2 + 0.097$	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2 – 1.386$	$V_{DD}/2 – 1.287$	$V_{DD}/2 – 1.169$	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2 + 1.210$	$V_{DD}/2 + 1.290$	$V_{DD}/2 + 1.355$	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.055$	$V_{DD}/2 + 0.001$	$V_{DD}/2 + 0.054$	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2 – 1.359$	$V_{DD}/2 – 1.292$	$V_{DD}/2 – 1.214$	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2 + 1.198$	$V_{DD}/2 + 1.292$	$V_{DD}/2 + 1.368$	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.041$	$V_{DD}/2$	$V_{DD}/2 + 0.04$	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2 – 1.362$	$V_{DD}/2 – 1.295$	$V_{DD}/2 – 1.220$	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2 + 1.202$	$V_{DD}/2 + 1.292$	$V_{DD}/2 + 1.364$	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.033$	$V_{DD}/2$	$V_{DD}/2 + 0.030$	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2 – 1.364$	$V_{DD}/2 – 1.297$	$V_{DD}/2 – 1.222$	V
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.072	P2[4] + P2[6] – 0.017	P2[4] + P2[6] + 0.041	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.029	P2[4] – P2[6] + 0.010	P2[4] – P2[6] + 0.048	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.066	P2[4] + P2[6] – 0.010	P2[4] + P2[6] + 0.043	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.024	P2[4] – P2[6] + 0.004	P2[4] – P2[6] + 0.034	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.007	P2[4] + P2[6] + 0.053	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.028	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.033	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.006	P2[4] + P2[6] + 0.056	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.030	P2[4] – P2[6]	P2[4] – P2[6] + 0.032	V
0b010	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	$V_{DD} – 0.102$	$V_{DD} – 0.003$	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.040$	$V_{DD}/2 + 0.001$	$V_{DD}/2 + 0.039$	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	$V_{SS} + 0.005$	$V_{SS} + 0.020$	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	$V_{DD} – 0.082$	$V_{DD} – 0.002$	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.031$	$V_{DD}/2$	$V_{DD}/2 + 0.028$	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	$V_{SS} + 0.003$	$V_{SS} + 0.015$	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	$V_{DD} – 0.083$	$V_{DD} – 0.002$	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.032$	$V_{DD}/2 – 0.001$	$V_{DD}/2 + 0.029$	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	$V_{SS} + 0.002$	$V_{SS} + 0.014$	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	$V_{DD} – 0.081$	$V_{DD} – 0.002$	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.033$	$V_{DD}/2 – 0.001$	$V_{DD}/2 + 0.029$	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	$V_{SS} + 0.002$	$V_{SS} + 0.013$	V
0b011	All power settings Not allowed at 3.3 V	–	–	–	–	–	–	–

AC Electrical Characteristics

AC Chip-Level Specifications

These tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 29. 5-V and 3.3-V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}[19]	Internal main oscillator (IMO) frequency for 24 MHz	22.8	24	25.2[20,21]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 8 on page 18. SLIMO mode = 0.
F_{IMO6}	IMO frequency for 6 MHz	5.5	6	6.5[20,21]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 8 on page 18. SLIMO mode = 1.
F_{CPU1}	CPU frequency (5 V nominal)	0.937	24	24.6[20]	MHz	SLIMO mode = 0.
F_{CPU2}	CPU frequency (3.3 V nominal)	0.937	12	12.3[21]	MHz	SLIMO mode = 0.
F_{48M}	Digital PSoC block frequency	0	48	49.2[20,22]	MHz	Refer to the AC Digital Block Specifications.
F_{24M}	Digital PSoC block frequency	0	24	24.6[22]	MHz	
F_{32K1}	ILO frequency	15	32	64	kHz	
F_{32K2}	External crystal oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on timing this
F_{PLL}	PLL frequency	–	23.986	–	MHz	Is a multiple (x732) of crystal frequency.
$T_{PLLSLEW}$	PLL lock time	0.5	–	10	ms	
$T_{PLLSLEWSLOW}$	PLL lock time for low gain setting	0.5	–	50	ms	
T_{OS}	External crystal oscillator startup to 1%	–	1700	2620	ms	
T_{OSACC}	External crystal oscillator startup to 100 ppm	–	2800	3800	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{osacc} period. Correct operation assumes a properly loaded 1 µW maximum drive level 32.768 kHz crystal. 3.0 V ≤ V_{DD} ≤ 5.5 V, –40 °C ≤ T_A ≤ 85 °C.
t_{XRST}	External reset pulse width	10	–	–	µs	

Notes
19. Errata: When the device is operated within 0 °C to 70 °C, the frequency tolerance is reduced to ±2.5%, but if operated at extreme temperature (below 0°C or above 70 °C), frequency tolerance deviates from ±2.5% to ±5%. For more information, see "Errata" on page 67.
20. 4.75 V < V_{DD} < 5.25 V.
21. 3.0 V < V_{DD} < 3.6 V. See application note Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 for information on trimming for operation at 3.3 V.
22. See the individual user module datasheets for information on maximum frequencies for user modules.
23. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

Table 30. 2.7-V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO12}	IMO frequency for 12 MHz	11.5	12	12.7[27, 28]	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 8 on page 18. SLIMO mode = 1.
F_{IMO6}	IMO frequency for 6 MHz	5.5	6	6.5[27, 28]	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 8 on page 18. SLIMO mode = 1.
F_{CPU1}	CPU frequency (2.7 V nominal)	0.937	3	3.15[27]	MHz	SLIMO mode = 0.
F_{BLK27}	Digital PSoC block frequency (2.7 V nominal)	0	12	12.7[27, 28]	MHz	Refer to the AC Digital Block Specifications.
F_{32K1}	ILO frequency	8	32	96	kHz	
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on timing this
t_{XRST}	External reset pulse width	10	–	–	µs	
DC12M	12 MHz duty cycle	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.7	MHz	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power-up.
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the System Resets section of the PSoC Technical Reference Manual.
t_{jit_IMO}[29]	12 MHz IMO cycle-to-cycle jitter (RMS)	–	400	1000	ps	N = 32
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	600	1300	ps	
	12 MHz IMO period jitter (RMS)	–	100	500	ps	
t_{jit_PLL}[29]	12 MHz IMO cycle-to-cycle jitter (RMS)	–	400	1000	ps	N = 32
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	700	1300		
	12 MHz IMO period jitter (RMS)	–	300	500		

Notes
27. 2.4 V < V_{DD} < 3.0 V.
28. Refer to application note Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 for information on trimming for operation at 3.3 V.
29. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

AC GPIO Specifications

These tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

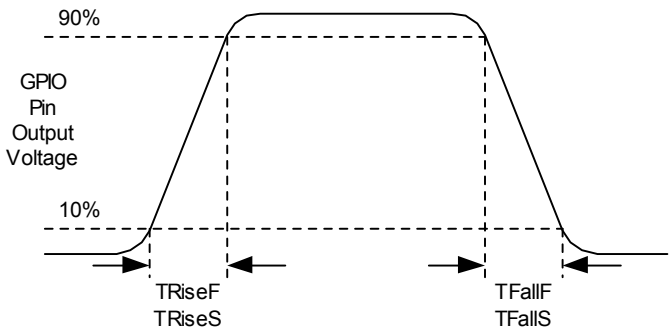
Table 31. 5-V and 3.3-V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12	MHz	Normal Strong Mode
tRiseF	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10% to 90%
tFallF	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10% to 90%
tRiseS	Rise time, slow strong mode, Cload = 50 pF	10	27	–	ns	V_{DD} = 3 to 5.25 V, 10% to 90%
tFallS	Fall time, slow strong mode, Cload = 50 pF	10	22	–	ns	V_{DD} = 3 to 5.25 V, 10% to 90%

Table 32. 2.7-V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	3	MHz	Normal strong mode
tRiseF	Rise time, normal strong mode, Cload = 50 pF	6	–	50	ns	V_{DD} = 2.4 to 3.0 V, 10% to 90%
tFallF	Fall time, normal strong mode, Cload = 50 pF	6	–	50	ns	V_{DD} = 2.4 to 3.0 V, 10% to 90%
tRiseS	Rise time, slow strong mode, Cload = 50 pF	18	40	120	ns	V_{DD} = 2.4 to 3.0 V, 10% to 90%
tFallS	Fall time, slow strong mode, Cload = 50 pF	18	40	120	ns	V_{DD} = 2.4 to 3.0 V, 10% to 90%

Figure 0-1. GPIO Timing Diagram



AC Operational Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the analog continuous time PSoC block.

Power = high and Opamp bias = high is not supported at 3.3 V and 2.7 V.

Table 33. 5-V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
t_{ROA}	Rising settling time from 80% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs
t_{SOA}	Falling settling time from 20% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs
SR_{ROA}	Rising slew rate (20% to 80%) (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 0.15 1.7 6.5	 – – –	 – – –	 V/µs V/µs V/µs
SR_{FOA}	Falling slew rate (20% to 80%) (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 0.01 0.5 4.0	 – – –	 – – –	 V/µs V/µs V/µs
BW_{OA}	Gain bandwidth product Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz
E_{NOA}	Noise at 1 kHz (Power = medium, Opamp bias = high)	–	100	–	nV/rt-Hz

Table 34. 3.3-V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
t_{ROA}	Rising settling time from 80% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 – –	 – –	 3.92 0.72	 µs µs
t_{SOA}	Falling settling time from 20% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 – –	 – –	 5.41 0.72	 µs µs
SR_{ROA}	Rising slew rate (20% to 80%) (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 0.31 2.7	 – –	 – –	 V/µs V/µs
SR_{FOA}	Falling slew rate (20% to 80%) (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 0.24 1.8	 – –	 – –	 V/µs V/µs
BW_{OA}	Gain bandwidth product Power = low, Opamp bias = low Power = medium, Opamp bias = high	 0.67 2.8	 – –	 – –	 MHz MHz
E_{NOA}	Noise at 1 kHz (Power = medium, Opamp bias = high)	–	100	–	nV/rt-Hz

AC Analog Output Buffer Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 39. 5-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
t_{ROB}	Rising settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high	 – –	 – –	 2.5 2.5	 µs µs
t_{SOB}	Falling settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high	 – –	 – –	 2.2 2.2	 µs µs
SR_{ROB}	Rising slew rate (20% to 80%), 1 V Step, 100 pF load Power = low Power = high	 0.65 0.65	 – –	 – –	 V/µs V/µs
SR_{FOB}	Falling slew rate (80% to 20%), 1 V Step, 100 pF load Power = low Power = high	 0.65 0.65	 – –	 – –	 V/µs V/µs
BW_{OB}	Small signal bandwidth, 20mV_{pp}, 3dB BW, 100 pF load Power = low Power = high	 0.8 0.8	 – –	 – –	 MHz MHz
BW_{OB}	Large signal bandwidth, 1V_{pp}, 3dB BW, 100 pF load Power = low Power = high	 300 300	 – –	 – –	 kHz kHz

Table 40. 3.3-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
t_{ROB}	Rising settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high	 – –	 – –	 3.8 3.8	 µs µs
t_{SOB}	Falling settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high	 – –	 – –	 2.6 2.6	 µs µs
SR_{ROB}	Rising slew rate (20% to 80%), 1 V Step, 100 pF load Power = low Power = high	 0.5 0.5	 – –	 – –	 V/µs V/µs
SR_{FOB}	Falling slew rate (80% to 20%), 1 V Step, 100 pF load Power = low Power = high	 0.5 0.5	 – –	 – –	 V/µs V/µs
BW_{OB}	Small signal bandwidth, 20mV_{pp}, 3dB BW, 100 pF load Power = low Power = high	 0.7 0.7	 – –	 – –	 MHz MHz
BW_{OB}	Large signal bandwidth, 1V_{pp}, 3dB BW, 100 pF load Power = low Power = high	 200 200	 – –	 – –	 kHz kHz

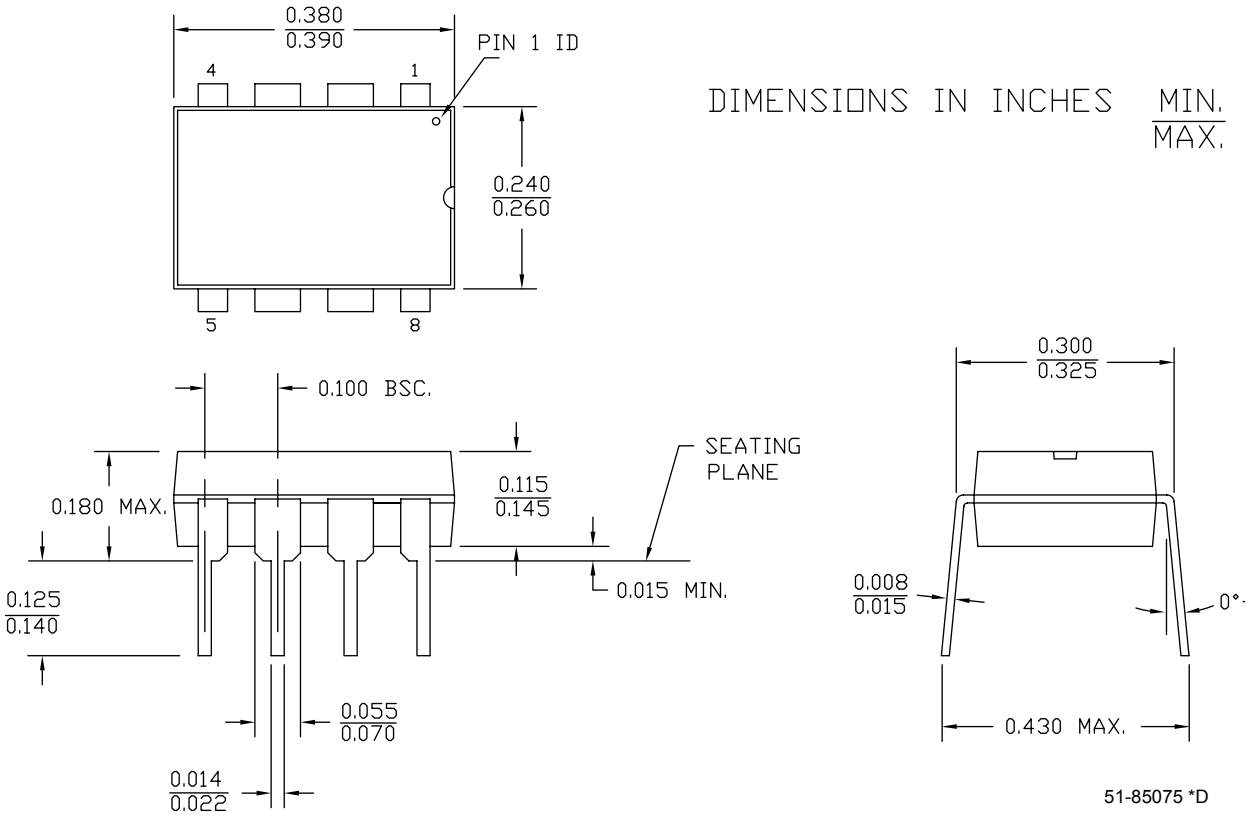
Packaging Information

This section illustrates the packaging specifications for the CY8C24x23A PSoC device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, see the emulator pod drawings at http://www.cypress.com/design/MR10161.

Packaging Dimensions

Figure 17. 8-Pin (300-Mil) PDIP



Glossary (continued)

duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
external reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
flash	An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5 V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device.***

Glossary (continued)

shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Errata

This section describes the errata for the CY8C24xxxA device family. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Ordering Information
CY8C24123A	CY8C24123A-24PXI
	CY8C24123A-24SXI
	CY8C24123A-24SXIT
	CY8C24223A-24PXI
	CY8C24223A-24PVXI
	CY8C24223A-24PVXIT
	CY8C24223A-24SXI
	CY8C24223A-24SXIT
	CY8C24423A-24PXI
	CY8C24423A-24PVXI
	CY8C24423A-24PVXIT
	CY8C24423A-24SXI
	CY8C24423A-24SXIT
	CY8C24423A-24LFXI
	CY8C24423A-24LTXI
	CY8C24423A-24LTXIT
	CY8C24000A-24PVXI

CY8C24123A Qualification Status

Product Status: Production

CY8C24123A Errata Summary

The following table defines the errata applicability to available CY8C24123A family devices.

Items	Part Number	Silicon Revision	Fix Status
[1.]. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes	CY8C24123A	*A	No silicon fix planned. Workaround is required.

1. **Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes**
   - **Problem Definition**
     Asynchronous Digital Communications Interfaces may fail framing beyond 0 to 70 °C. This problem does not affect end-product usage between 0 and 70 °C.
   - **Parameters Affected**
     The IMO frequency tolerance. The worst case deviation when operated below 0°C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.
   - **Trigger Condition(S)**
     The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the data sheet limit of ±2.5% when operated beyond the temperature range of 0 to +70 °C.
   - **Scope of Impact**
     This problem may affect UART, IrDA, and FSK implementations.
   - **Workaround**
     Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.
   - **Fix Status**
     Silicon fix is not planned. The workaround mentioned above should be used.

Document History Page (continued)

Document Title: CY8C24123A/CY8C24223A/CY8C24423A, PSoC® Programmable System-on-Chip Document Number: 38-12028				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*L	2897881	MAXK / NJF	03/23/2010	Add "More Information" on page 2. Update unit in Table 10-28 and Table 38 of SPIS Maximum Input Clock Frequency from ns to MHz. Update revision of package diagrams for 8 PDIP, 8 SOIC, 20 PDIP, 20 SSOP, 20 SOIC, 28 PDIP, 28 SSOP, 28 SOIC, 32 QFN. Updated Cypress website links. Removed reference to PSoC Designer 4.4. Updated 56-Pin SSOP definitions and diagram. Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings. Updated 5-V DC Analog Reference Specifications table. Updated Note in Packaging Information. Added Note 29. Updated Solder Reflow Specifications table. Removed Third Party Tools and Build a PSoC Emulator into your Board. Removed inactive parts from Ordering Information. Update trademark info. and Sales, Solutions, and Legal Information.
*M	2942375	VMAD	06/02/2010	Updated content to match current style guide and datasheet template. No technical updates.
*N	3032514	NJF	09/17/10	Added PSoC Device Characteristics table. Added DC I^2C Specifications table. Added F_{32K_U} max limit. Added Tjit_IMO specification, removed existing jitter specifications. Updated Analog reference tables. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changes were made to AC Digital Block Specifications table and I^2C Timing Diagram. They were updated for clearer understanding. Updated Figure 13 since the labelling for y-axis was incorrect. Template and styles update.
*O	3098766	YJI	12/01/2010	Sunset review; no content update
*P	3351721	YJI	08/31/2011	Full annual review of document. No changes are required.
*Q	3367463	BTK / GIR	09/22/2011	Updated text under DC Analog Reference Specifications on page 28. Removed package diagram spec 51-85188 as there is no active MPN using this outline drawing. The text "Pin must be left floating" is included under Description of NC pin in Table 5 on page 13 and Table 6 on page 14. Updated Table 50 on page 57 to give more clarity. Removed Footnote #35.
*R	3598291	LURE / XZNG	04/24/2012	Changed the PWM description string from "8- to 32-bit" to "8- and 16-bit".
*S	3991993	PMAD	05/08/2013	Updated Packaging Information: spec 51-85066 – Changed revision from *E to *F. spec 51-85014 – Changed revision from *F to *G. spec 51-85026 – Changed revision from *F to *G. spec 001-30999 – Changed revision from *C to *D. spec 51-85062 – Changed revision from *E to *F. Updated Reference Documents (Removed 001-17397 spec, 001-14503 spec related information). Added Errata.

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