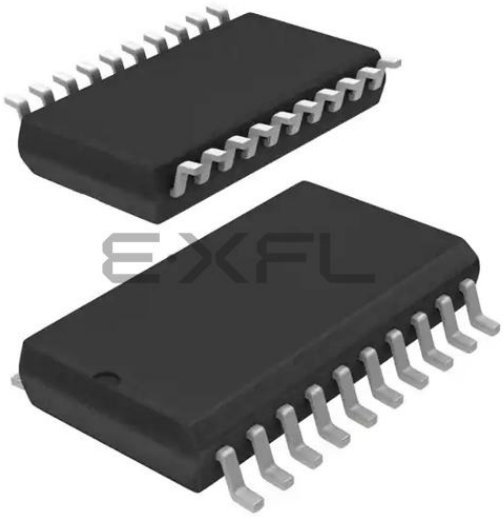

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | M8C |
| Core Size | 8-Bit |
| Speed | 24MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 16 |
| Program Memory Size | 4KB (4K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.4V ~ 5.25V |
| Data Converters | A/D 8x14b; D/A 2x9b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | 20-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24223a-24sxit |

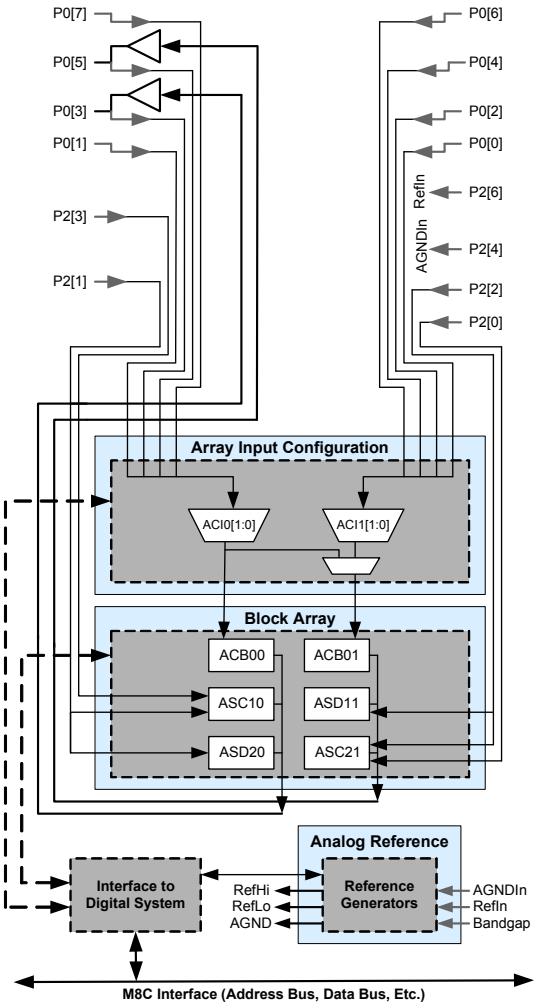
## Analog System

The analog system consists of six configurable blocks, each consisting of an opamp circuit that allows the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- ADCs (up to two, with 6- to 14-bit resolution, selectable as incremental, delta sigma, and SAR)
- Filters (two and four pole band-pass, low-pass, and notch)
- Amplifiers (up to two, with selectable gain to 48x)
- Instrumentation amplifiers (one with selectable gain to 93x)
- Comparators (up to two, with 16 selectable thresholds)
- DACs (up to two, with 6 to 9-bit resolution)
- Multiplying DACs (up to two, with 6 to 9-bit resolution)
- High current output drivers (two with 30 mA drive as a PSoC Core resource)
- 1.3 V reference (as a system resource)
- DTMF dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are arranged in a column of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks, as shown in Figure 3

**Figure 3. Analog System Block Diagram**



# Register Reference

This section lists the registers of the CY8C24x23A PSoC device. For detailed register information, see the PSoC Programmable Sytem-on-Chip Reference Manual.

## Register Conventions

*Abbreviations Used*

The register conventions specific to this section are listed in the following table.

**Table 7. Abbreviations**

| Convention | Description |
|---|---|
| R | Read register or bit(s) |
| W | Write register or bit(s) |
| L | Logical register or bit(s) |
| C | Clearable register or bit(s) |
| # | Access is bit specific |

## Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, Bank 0 and Bank 1. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set, the user is in Bank 1.

**Note** In the following register mapping tables, blank fields are reserved and must not be accessed.

**Table 8. Register Map Bank 0 Table: User Space**

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PRT0DR | 00 | RW | | 40 | | ASC10CR0 | 80 | RW | | C0 | |
| PRT0IE | 01 | RW | | 41 | | ASC10CR1 | 81 | RW | | C1 | |
| PRT0GS | 02 | RW | | 42 | | ASC10CR2 | 82 | RW | | C2 | |
| PRT0DM2 | 03 | RW | | 43 | | ASC10CR3 | 83 | RW | | C3 | |
| PRT1DR | 04 | RW | | 44 | | ASD11CR0 | 84 | RW | | C4 | |
| PRT1IE | 05 | RW | | 45 | | ASD11CR1 | 85 | RW | | C5 | |
| PRT1GS | 06 | RW | | 46 | | ASD11CR2 | 86 | RW | | C6 | |
| PRT1DM2 | 07 | RW | | 47 | | ASD11CR3 | 87 | RW | | C7 | |
| PRT2DR | 08 | RW | | 48 | | | 88 | | | C8 | |
| PRT2IE | 09 | RW | | 49 | | | 89 | | | C9 | |
| PRT2GS | 0A | RW | | 4A | | | 8A | | | CA | |
| PRT2DM2 | 0B | RW | | 4B | | | 8B | | | CB | |
| | 0C | | | 4C | | | 8C | | | CC | |
| | 0D | | | 4D | | | 8D | | | CD | |
| | 0E | | | 4E | | | 8E | | | CE | |
| | 0F | | | 4F | | | 8F | | | CF | |
| | 10 | | | 50 | | ASD20CR0 | 90 | RW | | D0 | |
| | 11 | | | 51 | | ASD20CR1 | 91 | RW | | D1 | |
| | 12 | | | 52 | | ASD20CR2 | 92 | RW | | D2 | |
| | 13 | | | 53 | | ASD20CR3 | 93 | RW | | D3 | |
| | 14 | | | 54 | | ASC21CR0 | 94 | RW | | D4 | |
| | 15 | | | 55 | | ASC21CR1 | 95 | RW | | D5 | |
| | 16 | | | 56 | | ASC21CR2 | 96 | RW | I2C_CFG | D6 | RW |
| | 17 | | | 57 | | ASC21CR3 | 97 | RW | I2C_SCR | D7 | # |
| | 18 | | | 58 | | | 98 | | I2C_DR | D8 | RW |
| | 19 | | | 59 | | | 99 | | I2C_MSCR | D9 | # |
| | 1A | | | 5A | | | 9A | | INT_CLR0 | DA | RW |
| | 1B | | | 5B | | | 9B | | INT_CLR1 | DB | RW |
| | 1C | | | 5C | | | 9C | | | DC | |
| | 1D | | | 5D | | | 9D | | INT_CLR3 | DD | RW |
| | 1E | | | 5E | | | 9E | | INT_MSK3 | DE | RW |
| | 1F | | | 5F | | | 9F | | | DF | |
| DBB00DR0 | 20 | # | AMX_IN | 60 | RW | | A0 | | INT_MSK0 | E0 | RW |
| DBB00DR1 | 21 | W | | 61 | | | A1 | | INT_MSK1 | E1 | RW |
| DBB00DR2 | 22 | RW | | 62 | | | A2 | | INT_VC | E2 | RC |
| DBB00CR0 | 23 | # | ARF_CR | 63 | RW | | A3 | | RES_WDT | E3 | W |
| DBB01DR0 | 24 | # | CMP_CR0 | 64 | # | | A4 | | DEC_DH | E4 | RC |
| DBB01DR1 | 25 | W | ASY_CR | 65 | # | | A5 | | DEC_DL | E5 | RC |
| DBB01DR2 | 26 | RW | CMP_CR1 | 66 | RW | | A6 | | DEC_CR0 | E6 | RW |
| DBB01CR0 | 27 | # | | 67 | | | A7 | | DEC_CR1 | E7 | RW |
| DCB02DR0 | 28 | # | | 68 | | | A8 | | MUL_X | E8 | W |
| DCB02DR1 | 29 | W | | 69 | | | A9 | | MUL_Y | E9 | W |
| DCB02DR2 | 2A | RW | | 6A | | | AA | | MUL_DH | EA | R |
| DCB02CR0 | 2B | # | | 6B | | | AB | | MUL_DL | EB | R |
| DCB03DR0 | 2C | # | | 6C | | | AC | | ACC_DR1 | EC | RW |
| DCB03DR1 | 2D | W | | 6D | | | AD | | ACC_DR0 | ED | RW |
| DCB03DR2 | 2E | RW | | 6E | | | AE | | ACC_DR3 | EE | RW |
| DCB03CR0 | 2F | # | | 6F | | | AF | | ACC_DR2 | EF | RW |
| | 30 | | ACB00CR3 | 70 | RW | RDI0RI | B0 | RW | | F0 | |
| | 31 | | ACB00CR0 | 71 | RW | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | ACB00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACB00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | ACB01CR3 | 74 | RW | RDI0LT1 | B4 | RW | | F4 | |
| | 35 | | ACB01CR0 | 75 | RW | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | ACB01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACB01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | | FA | |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | | FD | |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

**Blank fields are Reserved and must not be accessed.** **# Access is bit specific.**

**Table 15. 3.3-V DC Operational Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{OSOA}$ | Input offset voltage (absolute value)<br>Power = low, Opamp bias = high<br>Power = medium, Opamp bias = high<br>Power = high, Opamp bias = high | <br>–<br>–<br>– | <br>1.65<br>1.32<br>– | <br>10<br>8<br>– | <br>mV<br>mV<br>mV | Power = high, Opamp bias = high setting is not allowed for 3.3 V $V_{DD}$ operation. |
| $TCV_{OSOA}$ | Average input offset voltage drift | – | 7.0 | 35.0 | µV/°C | |
| $I_{EBOA}$ | Input leakage current (port 0 analog pins) | – | 20 | – | pA | Gross tested to 1 µA |
| $C_{INOA}$ | Input capacitance (port 0 analog pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25 °C |
| $V_{CMOA}$ | Common mode voltage range | 0.2 | – | $V_{DD}$ – 0.2 | V | The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer. |
| $G_{OLOA}$ | Open loop gain<br>Power = low, ppamp Opamp bias = low<br>Power = medium, Opamp bias = low<br>Power = high, Opamp bias = low | <br>60<br>60<br>80 | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>dB<br>dB<br>dB | Specification is applicable at low Opamp bias. For high Opamp bias mode (except high power, high Opamp bias), minimum is 60 dB. |
| $V_{OHIGHOA}$ | High output voltage swing (internal signals)<br>Power = low, Opamp bias = low<br>Power = medium, Opamp bias = low<br>Power = high, Opamp bias = low | <br>$V_{DD}$ – 0.2<br>$V_{DD}$ – 0.2<br>$V_{DD}$ – 0.2 | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>V<br>V<br>V | Power = high, Opamp bias = high setting is not allowed for 3.3 V $V_{DD}$ operation. |
| $V_{OLOWOA}$ | Low output voltage swing (internal signals)<br>Power = low, ppamp Opamp bias = low<br>Power = medium, Opamp bias = low<br>Power = high, Opamp bias = low | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>0.2<br>0.2<br>0.2 | <br>V<br>V<br>V | Power = high, Opamp bias = high setting is not allowed for 3.3 V $V_{DD}$ operation. |
| $I_{SOA}$ | Supply current (including associated AGND buffer)<br>Power = low, Opamp bias = low<br>Power = low, Opamp bias = high<br>Power = medium, Opamp bias = low<br>Power = medium, Opamp bias = high<br>Power = high, Opamp bias = low<br>Power = high, Opamp bias = high | <br>–<br>–<br>–<br>–<br>–<br>– | <br>150<br>300<br>600<br>1200<br>2400<br>– | <br>200<br>400<br>800<br>1600<br>3200<br>– | <br>µA<br>µA<br>µA<br>µA<br>µA<br>µA | Power = high, Opamp bias = high setting is not allowed for 3.3 V $V_{DD}$ operation. |
| $PSRR_{OA}$ | Supply voltage rejection ratio | 64 | 80 | – | dB | $V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$ |

*DC Switch Mode Pump Specifications*

Table 21 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ $T_A$ ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

**Table 21. DC Switch Mode Pump (SMP) Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{PUMP}$ 5 V | 5 V output voltage from pump | 4.75 | 5.0 | 5.25 | V | Configuration listed in footnote.[11] Average, neglecting ripple. SMP trip voltage is set to 5.0 V. |
| $V_{PUMP}$ 3 V | 3.3 V output voltage from pump | 3.00 | 3.25 | 3.60 | V | Configuration listed in footnote.[11] Average, neglecting ripple. SMP trip voltage is set to 3.25 V. |
| $V_{PUMP}$ 2 V | 2.6 V output voltage from pump | 2.45 | 2.55 | 2.80 | V | Configuration listed in footnote.[11] Average, neglecting ripple. SMP trip voltage is set to 2.55 V. |
| $I_{PUMP}$ | Available output current<br>$V_{BAT}$ = 1.8 V, $V_{PUMP}$ = 5.0 V<br>$V_{BAT}$ = 1.5 V, $V_{PUMP}$ = 3.25 V<br>$V_{BAT}$ = 1.3 V, $V_{PUMP}$ = 2.55 V | <br>5<br>8<br>8 | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>mA<br>mA<br>mA | Configuration listed in footnote.[11]<br>SMP trip voltage is set to 5.0 V.<br>SMP trip voltage is set to 3.25 V.<br>SMP trip voltage is set to 2.55 V. |
| $V_{BAT}$5 V | Input voltage range from battery | 1.8 | – | 5.0 | V | Configuration listed in footnote.[11] SMP trip voltage is set to 5.0 V. |
| $V_{BAT}$3 V | Input voltage range from battery | 1.0 | – | 3.3 | V | Configuration listed in footnote.[11] SMP trip voltage is set to 3.25 V. |
| $V_{BAT}$2 V | Input voltage range from battery | 1.0 | – | 3.0 | V | Configuration listed in footnote.[11] SMP trip voltage is set to 2.55 V. |
| $V_{BATSTART}$ | Minimum input voltage from battery to start pump | 1.2 | – | – | V | Configuration listed in footnote.[11] 0 °C ≤ $T_A$ ≤ 100. 1.25 V at $T_A$ = –40 °C |
| $\Delta V_{PUMP_Line}$ | Line regulation (over $V_{BAT}$ range) | – | 5 | – | $\%V_O$ | Configuration listed in footnote.[11] $V_O$ is the $V_{DD}$ Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 26 on page 35. |
| $\Delta V_{PUMP_Load}$ | Load regulation | – | 5 | – | $\%V_O$ | Configuration listed in footnote.[11] $V_O$ is the "$V_{DD}$ value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 26 on page 35. |
| $\Delta V_{PUMP_Ripple}$ | Output voltage ripple (depends on capacitor/load) | – | 100 | – | mVpp | Configuration listed in footnote.[11] Load is 5 mA. |
| $E_3$ | Efficiency | 35 | 50 | – | % | Configuration listed in footnote.[11] Load is 5 mA. SMP trip voltage is set to 3.25 V. |
| $E_2$ | Efficiency | – | – | – | | |
| $F_{PUMP}$ | Switching frequency | – | 1.3 | – | MHz | |
| $DC_{PUMP}$ | Switching duty cycle | – | 50 | – | % | |

**Note**
11. $L_1$ = 2 mH inductor, $C_1$ = 10 mF capacitor, $D_1$ = Schottky diode. See Figure 10

**Figure 10. Basic Switch Mode Pump Circuit**

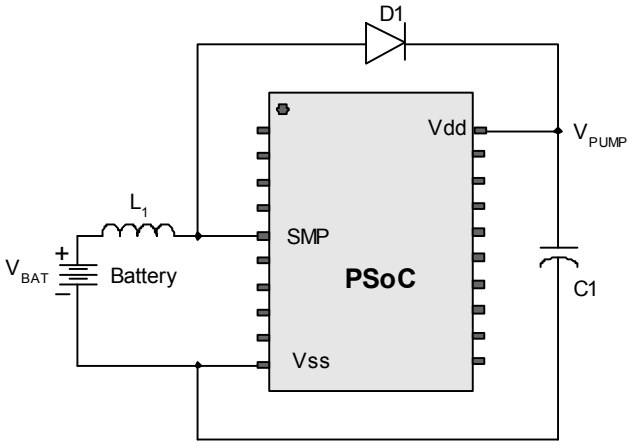


**Table 22. 5-V DC Analog Reference Specifications** (continued)

| Reference ARF_CR [5:3] | Reference Power Settings | Symbol | Reference | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| 0b010 | RefPower = high Opamp bias = high | $V_{REFHI}$ | Ref High | $V_{DD}$ | $V_{DD}$ – 0.121 | $V_{DD}$ – 0.003 | $V_{DD}$ | V |
| | | $V_{AGND}$ | AGND | $V_{DD}/2$ | $V_{DD}/2$ – 0.040 | $V_{DD}/2$ | $V_{DD}/2$ + 0.034 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.006 | $V_{SS}$ + 0.019 | V |
| | RefPower = high Opamp bias = low | $V_{REFHI}$ | Ref High | $V_{DD}$ | $V_{DD}$ – 0.083 | $V_{DD}$ – 0.002 | $V_{DD}$ | V |
| | | $V_{AGND}$ | AGND | $V_{DD}/2$ | $V_{DD}/2$ – 0.040 | $V_{DD}/2$ – 0.001 | $V_{DD}/2$ + 0.033 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.004 | $V_{SS}$ + 0.016 | V |
| | RefPower = medium Opamp bias = high | $V_{REFHI}$ | Ref High | $V_{DD}$ | $V_{DD}$ – 0.075 | $V_{DD}$ – 0.002 | $V_{DD}$ | V |
| | | $V_{AGND}$ | AGND | $V_{DD}/2$ | $V_{DD}/2$ – 0.040 | $V_{DD}/2$ – 0.001 | $V_{DD}/2$ + 0.032 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.003 | $V_{SS}$ + 0.015 | V |
| | RefPower = medium Opamp bias = low | $V_{REFHI}$ | Ref High | $V_{DD}$ | $V_{DD}$ – 0.074 | $V_{DD}$ – 0.002 | $V_{DD}$ | V |
| | | $V_{AGND}$ | AGND | $V_{DD}/2$ | $V_{DD}/2$ – 0.040 | $V_{DD}/2$ – 0.001 | $V_{DD}/2$ + 0.032 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.002 | $V_{SS}$ + 0.014 | V |
| 0b011 | RefPower = high Opamp bias = high | $V_{REFHI}$ | Ref High | 3 × Bandgap | 3.753 | 3.874 | 3.979 | V |
| | | $V_{AGND}$ | AGND | 2 × Bandgap | 2.511 | 2.590 | 2.657 | V |
| | | $V_{REFLO}$ | Ref Low | Bandgap | 1.243 | 1.297 | 1.333 | V |
| | RefPower = high Opamp bias = low | $V_{REFHI}$ | Ref High | 3 × Bandgap | 3.767 | 3.881 | 3.974 | V |
| | | $V_{AGND}$ | AGND | 2 × Bandgap | 2.518 | 2.592 | 2.652 | V |
| | | $V_{REFLO}$ | Ref Low | Bandgap | 1.241 | 1.295 | 1.330 | V |
| | RefPower = medium Opamp bias = high | $V_{REFHI}$ | Ref High | 3 × Bandgap | 2.771 | 3.885 | 3.979 | V |
| | | $V_{AGND}$ | AGND | 2 × Bandgap | 2.521 | 2.593 | 2.649 | V |
| | | $V_{REFLO}$ | Ref Low | Bandgap | 1.240 | 1.295 | 1.331 | V |
| | RefPower = medium Opamp bias = low | $V_{REFHI}$ | Ref High | 3 × Bandgap | 3.771 | 3.887 | 3.977 | V |
| | | $V_{AGND}$ | AGND | 2 × Bandgap | 2.522 | 2.594 | 2.648 | V |
| | | $V_{REFLO}$ | Ref Low | Bandgap | 1.239 | 1.295 | 1.332 | V |
| 0b100 | RefPower = high Opamp bias = high | $V_{REFHI}$ | Ref High | 2 × Bandgap + P2[6] (P2[6] = 1.3 V) | 2.481 + P2[6] | 2.569 + P2[6] | 2.639 + P2[6] | V |
| | | $V_{AGND}$ | AGND | 2 × Bandgap | 2.511 | 2.590 | 2.658 | V |
| | | $V_{REFLO}$ | Ref Low | 2 × Bandgap – P2[6] (P2[6] = 1.3 V) | 2.515 – P2[6] | 2.602 – P2[6] | 2.654 – P2[6] | V |
| | RefPower = high Opamp bias = low | $V_{REFHI}$ | Ref High | 2 × Bandgap + P2[6] (P2[6] = 1.3 V) | 2.498 + P2[6] | 2.579 + P2[6] | 2.642 + P2[6] | V |
| | | $V_{AGND}$ | AGND | 2 × Bandgap | 2.518 | 2.592 | 2.652 | V |
| | | $V_{REFLO}$ | Ref Low | 2 × Bandgap – P2[6] (P2[6] = 1.3 V) | 2.513 – P2[6] | 2.598 – P2[6] | 2.650 – P2[6] | V |
| | RefPower = medium Opamp bias = high | $V_{REFHI}$ | Ref High | 2 × Bandgap + P2[6] (P2[6] = 1.3 V) | 2.504 + P2[6] | 2.583 + P2[6] | 2.646 + P2[6] | V |
| | | $V_{AGND}$ | AGND | 2 × Bandgap | 2.521 | 2.592 | 2.650 | V |
| | | $V_{REFLO}$ | Ref Low | 2 × Bandgap – P2[6] (P2[6] = 1.3 V) | 2.513 – P2[6] | 2.596 – P2[6] | 2.649 – P2[6] | V |
| | RefPower = medium Opamp bias = low | $V_{REFHI}$ | Ref High | 2 × Bandgap + P2[6] (P2[6] = 1.3 V) | 2.505 + P2[6] | 2.586 + P2[6] | 2.648 + P2[6] | V |
| | | $V_{AGND}$ | AGND | 2 × Bandgap | 2.521 | 2.594 | 2.648 | V |
| | | $V_{REFLO}$ | Ref Low | 2 × Bandgap – P2[6] (P2[6] = 1.3 V) | 2.513 – P2[6] | 2.595 – P2[6] | 2.648 – P2[6] | V |

**Table 22. 5-V DC Analog Reference Specifications** (continued)

| Reference ARF_CR [5:3] | Reference Power Settings | Symbol | Reference | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| 0b101 | RefPower = high Opamp bias = high | $V_{REFHI}$ | Ref High | P2[4] + Bandgap ($P2[4] = V_{DD}/2$) | P2[4] + 1.228 | P2[4] + 1.284 | P2[4] + 1.332 | V |
| | | $V_{AGND}$ | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | $V_{REFLO}$ | Ref Low | P2[4] – Bandgap ($P2[4] = V_{DD}/2$) | P2[4] – 1.358 | P2[4] – 1.293 | P2[4] – 1.226 | V |
| | RefPower = high Opamp bias = low | $V_{REFHI}$ | Ref High | P2[4] + Bandgap ($P2[4] = V_{DD}/2$) | P2[4] + 1.236 | P2[4] + 1.289 | P2[4] + 1.332 | V |
| | | $V_{AGND}$ | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | $V_{REFLO}$ | Ref Low | P2[4] – Bandgap ($P2[4] = V_{DD}/2$) | P2[4] – 1.357 | P2[4] – 1.297 | P2[4] – 1.229 | V |
| | RefPower = medium Opamp bias = high | $V_{REFHI}$ | Ref High | P2[4] + Bandgap ($P2[4] = V_{DD}/2$) | P2[4] + 1.237 | P2[4] + 1.291 | P2[4] + 1.337 | V |
| | | $V_{AGND}$ | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | $V_{REFLO}$ | Ref Low | P2[4] – Bandgap ($P2[4] = V_{DD}/2$) | P2[4] – 1.356 | P2[4] – 1.299 | P2[4] – 1.232 | V |
| | RefPower = medium Opamp bias = low | $V_{REFHI}$ | Ref High | P2[4] + Bandgap ($P2[4] = V_{DD}/2$) | P2[4] + 1.237 | P2[4] + 1.292 | P2[4] + 1.337 | V |
| | | $V_{AGND}$ | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | $V_{REFLO}$ | Ref Low | P2[4] – Bandgap ($P2[4] = V_{DD}/2$) | P2[4] – 1.357 | P2[4] – 1.300 | P2[4] – 1.233 | V |
| 0b110 | RefPower = high Opamp bias = high | $V_{REFHI}$ | Ref High | 2 × Bandgap | 2.512 | 2.594 | 2.654 | V |
| | | $V_{AGND}$ | AGND | Bandgap | 1.250 | 1.303 | 1.346 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.011 | $V_{SS}$ + 0.027 | V |
| | RefPower = high Opamp bias = low | $V_{REFHI}$ | Ref High | 2 × Bandgap | 2.515 | 2.592 | 2.654 | V |
| | | $V_{AGND}$ | AGND | Bandgap | 1.253 | 1.301 | 1.340 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.006 | $V_{SS}$ + 0.02 | V |
| | RefPower = medium Opamp bias = high | $V_{REFHI}$ | Ref High | 2 × Bandgap | 2.518 | 2.593 | 2.651 | V |
| | | $V_{AGND}$ | AGND | Bandgap | 1.254 | 1.301 | 1.338 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.004 | $V_{SS}$ + 0.017 | V |
| | RefPower = medium Opamp bias = low | $V_{REFHI}$ | Ref High | 2 × Bandgap | 2.517 | 2.594 | 2.650 | V |
| | | $V_{AGND}$ | AGND | Bandgap | 1.255 | 1.300 | 1.337 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.003 | $V_{SS}$ + 0.015 | V |
| 0b111 | RefPower = high Opamp bias = high | $V_{REFHI}$ | Ref High | 3.2 × Bandgap | 4.011 | 4.143 | 4.203 | V |
| | | $V_{AGND}$ | AGND | 1.6 × Bandgap | 2.020 | 2.075 | 2.118 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.011 | $V_{SS}$ + 0.026 | V |
| | RefPower = high Opamp bias = low | $V_{REFHI}$ | Ref High | 3.2 × Bandgap | 4.022 | 4.138 | 4.203 | V |
| | | $V_{AGND}$ | AGND | 1.6 × Bandgap | 2.023 | 2.075 | 2.114 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.006 | $V_{SS}$ + 0.017 | V |
| | RefPower = medium Opamp bias = high | $V_{REFHI}$ | Ref High | 3.2 × Bandgap | 4.026 | 4.141 | 4.207 | V |
| | | $V_{AGND}$ | AGND | 1.6 × Bandgap | 2.024 | 2.075 | 2.114 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.004 | $V_{SS}$ + 0.015 | V |
| | RefPower = medium Opamp bias = low | $V_{REFHI}$ | Ref High | 3.2 × Bandgap | 4.030 | 4.143 | 4.206 | V |
| | | $V_{AGND}$ | AGND | 1.6 × Bandgap | 2.024 | 2.076 | 2.112 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.003 | $V_{SS}$ + 0.013 | V |

**Table 23. 3.3-V DC Analog Reference Specifications**

| Reference ARF_CR [5:3] | Reference Power Settings | Symbol | Reference | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| 0b000 | RefPower = high Opamp bias = high | $V_{REFHI}$ | Ref High | $V_{DD}/2$ + Bandgap | $V_{DD}/2$ + 1.170 | $V_{DD}/2$ + 1.288 | $V_{DD}/2$ + 1.376 | V |
| | | $V_{AGND}$ | AGND | $V_{DD}/2$ | $V_{DD}/2$ – 0.098 | $V_{DD}/2$ + 0.003 | $V_{DD}/2$ + 0.097 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{DD}/2$ – Bandgap | $V_{DD}/2$ – 1.386 | $V_{DD}/2$ – 1.287 | $V_{DD}/2$ – 1.169 | V |
| | RefPower = high Opamp bias = low | $V_{REFHI}$ | Ref High | $V_{DD}/2$ + Bandgap | $V_{DD}/2$ + 1.210 | $V_{DD}/2$ + 1.290 | $V_{DD}/2$ + 1.355 | V |
| | | $V_{AGND}$ | AGND | $V_{DD}/2$ | $V_{DD}/2$ – 0.055 | $V_{DD}/2$ + 0.001 | $V_{DD}/2$ + 0.054 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{DD}/2$ – Bandgap | $V_{DD}/2$ – 1.359 | $V_{DD}/2$ – 1.292 | $V_{DD}/2$ – 1.214 | V |
| | RefPower = medium Opamp bias = high | $V_{REFHI}$ | Ref High | $V_{DD}/2$ + Bandgap | $V_{DD}/2$ + 1.198 | $V_{DD}/2$ + 1.292 | $V_{DD}/2$ + 1.368 | V |
| | | $V_{AGND}$ | AGND | $V_{DD}/2$ | $V_{DD}/2$ – 0.041 | $V_{DD}/2$ | $V_{DD}/2$ + 0.04 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{DD}/2$ – Bandgap | $V_{DD}/2$ – 1.362 | $V_{DD}/2$ – 1.295 | $V_{DD}/2$ – 1.220 | V |
| | RefPower = medium Opamp bias = low | $V_{REFHI}$ | Ref High | $V_{DD}/2$ + Bandgap | $V_{DD}/2$ + 1.202 | $V_{DD}/2$ + 1.292 | $V_{DD}/2$ + 1.364 | V |
| | | $V_{AGND}$ | AGND | $V_{DD}/2$ | $V_{DD}/2$ – 0.033 | $V_{DD}/2$ | $V_{DD}/2$ + 0.030 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{DD}/2$ – Bandgap | $V_{DD}/2$ – 1.364 | $V_{DD}/2$ – 1.297 | $V_{DD}/2$ – 1.222 | V |
| 0b001 | RefPower = high Opamp bias = high | $V_{REFHI}$ | Ref High | P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V) | P2[4] + P2[6] – 0.072 | P2[4] + P2[6] – 0.017 | P2[4] + P2[6] + 0.041 | V |
| | | $V_{AGND}$ | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | $V_{REFLO}$ | Ref Low | P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V) | P2[4] – P2[6] – 0.029 | P2[4] – P2[6] + 0.010 | P2[4] – P2[6] + 0.048 | V |
| | RefPower = high Opamp bias = low | $V_{REFHI}$ | Ref High | P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V) | P2[4] + P2[6] – 0.066 | P2[4] + P2[6] – 0.010 | P2[4] + P2[6] + 0.043 | V |
| | | $V_{AGND}$ | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | $V_{REFLO}$ | Ref Low | P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V) | P2[4] – P2[6] – 0.024 | P2[4] – P2[6] + 0.004 | P2[4] – P2[6] + 0.034 | V |
| | RefPower = medium Opamp bias = high | $V_{REFHI}$ | Ref High | P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V) | P2[4] + P2[6] – 0.073 | P2[4] + P2[6] – 0.007 | P2[4] + P2[6] + 0.053 | V |
| | | $V_{AGND}$ | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | $V_{REFLO}$ | Ref Low | P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V) | P2[4] – P2[6] – 0.028 | P2[4] – P2[6] + 0.002 | P2[4] – P2[6] + 0.033 | V |
| | RefPower = medium Opamp bias = low | $V_{REFHI}$ | Ref High | P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V) | P2[4] + P2[6] – 0.073 | P2[4] + P2[6] – 0.006 | P2[4] + P2[6] + 0.056 | V |
| | | $V_{AGND}$ | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | $V_{REFLO}$ | Ref Low | P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V) | P2[4] – P2[6] – 0.030 | P2[4] – P2[6] | P2[4] – P2[6] + 0.032 | V |
| 0b010 | RefPower = high Opamp bias = high | $V_{REFHI}$ | Ref High | $V_{DD}$ | $V_{DD}$ – 0.102 | $V_{DD}$ – 0.003 | $V_{DD}$ | V |
| | | $V_{AGND}$ | AGND | $V_{DD}/2$ | $V_{DD}/2$ – 0.040 | $V_{DD}/2$ + 0.001 | $V_{DD}/2$ + 0.039 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.005 | $V_{SS}$ + 0.020 | V |
| | RefPower = high Opamp bias = low | $V_{REFHI}$ | Ref High | $V_{DD}$ | $V_{DD}$ – 0.082 | $V_{DD}$ – 0.002 | $V_{DD}$ | V |
| | | $V_{AGND}$ | AGND | $V_{DD}/2$ | $V_{DD}/2$ – 0.031 | $V_{DD}/2$ | $V_{DD}/2$ + 0.028 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.003 | $V_{SS}$ + 0.015 | V |
| | RefPower = medium Opamp bias = high | $V_{REFHI}$ | Ref High | $V_{DD}$ | $V_{DD}$ – 0.083 | $V_{DD}$ – 0.002 | $V_{DD}$ | V |
| | | $V_{AGND}$ | AGND | $V_{DD}/2$ | $V_{DD}/2$ – 0.032 | $V_{DD}/2$ – 0.001 | $V_{DD}/2$ + 0.029 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.002 | $V_{SS}$ + 0.014 | V |
| | RefPower = medium Opamp bias = low | $V_{REFHI}$ | Ref High | $V_{DD}$ | $V_{DD}$ – 0.081 | $V_{DD}$ – 0.002 | $V_{DD}$ | V |
| | | $V_{AGND}$ | AGND | $V_{DD}/2$ | $V_{DD}/2$ – 0.033 | $V_{DD}/2$ – 0.001 | $V_{DD}/2$ + 0.029 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.002 | $V_{SS}$ + 0.013 | V |
| 0b011 | All power settings Not allowed at 3.3 V | – | – | – | – | – | – | – |

**Table 23. 3.3-V DC Analog Reference Specifications** (continued)

| Reference ARF_CR [5:3] | Reference Power Settings | Symbol | Reference | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| 0b100 | All power settings Not allowed at 3.3 V | – | – | – | – | – | – | – |
| 0b101 | RefPower = high Opamp bias = high | $V_{REFHI}$ | Ref High | P2[4] + Bandgap ($P2[4] = V_{DD}/2$) | P2[4] + 1.211 | P2[4] + 1.285 | P2[4] + 1.348 | V |
| | | $V_{AGND}$ | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | $V_{REFLO}$ | Ref Low | P2[4] – Bandgap ($P2[4] = V_{DD}/2$) | P2[4] – 1.354 | P2[4] – 1.290 | P2[4] – 1.197 | V |
| | RefPower = high Opamp bias = low | $V_{REFHI}$ | Ref High | P2[4] + Bandgap ($P2[4] = V_{DD}/2$) | P2[4] + 1.209 | P2[4] + 1.289 | P2[4] + 1.353 | V |
| | | $V_{AGND}$ | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | $V_{REFLO}$ | Ref Low | P2[4] – Bandgap ($P2[4] = V_{DD}/2$) | P2[4] – 1.352 | P2[4] – 1.294 | P2[4] – 1.222 | V |
| | RefPower = medium Opamp bias = high | $V_{REFHI}$ | Ref High | P2[4] + Bandgap ($P2[4] = V_{DD}/2$) | P2[4] + 1.218 | P2[4] + 1.291 | P2[4] + 1.351 | V |
| | | $V_{AGND}$ | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | $V_{REFLO}$ | Ref Low | P2[4] – Bandgap ($P2[4] = V_{DD}/2$) | P2[4] – 1.351 | P2[4] – 1.296 | P2[4] – 1.224 | V |
| | RefPower = medium Opamp bias = low | $V_{REFHI}$ | Ref High | P2[4] + Bandgap ($P2[4] = V_{DD}/2$) | P2[4] + 1.215 | P2[4] + 1.292 | P2[4] + 1.354 | V |
| | | $V_{AGND}$ | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | $V_{REFLO}$ | Ref Low | P2[4] – Bandgap ($P2[4] = V_{DD}/2$) | P2[4] – 1.352 | P2[4] – 1.297 | P2[4] – 1.227 | V |
| 0b110 | RefPower = high Opamp bias = high | $V_{REFHI}$ | Ref High | 2 × Bandgap | 2.460 | 2.594 | 2.695 | V |
| | | $V_{AGND}$ | AGND | Bandgap | 1.257 | 1.302 | 1.335 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.01 | $V_{SS}$ + 0.029 | V |
| | RefPower = high Opamp bias = low | $V_{REFHI}$ | Ref High | 2 × Bandgap | 2.462 | 2.592 | 2.692 | V |
| | | $V_{AGND}$ | AGND | Bandgap | 1.256 | 1.301 | 1.332 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.005 | $V_{SS}$ + 0.017 | V |
| | RefPower = medium Opamp bias = high | $V_{REFHI}$ | Ref High | 2 × Bandgap | 2.473 | 2.593 | 2.682 | V |
| | | $V_{AGND}$ | AGND | Bandgap | 1.257 | 1.301 | 1.330 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.003 | $V_{SS}$ + 0.014 | V |
| | RefPower = medium Opamp bias = low | $V_{REFHI}$ | Ref High | 2 × Bandgap | 2.470 | 2.594 | 2.685 | V |
| | | $V_{AGND}$ | AGND | Bandgap | 1.256 | 1.300 | 1.332 | V |
| | | $V_{REFLO}$ | Ref Low | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ + 0.002 | $V_{SS}$ + 0.012 | V |
| 0b111 | All power settings Not allowed at 3.3 V | – | – | – | – | – | – | – |

*AC Operational Amplifier Specifications*

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ $T_A$ ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the analog continuous time PSoC block.

Power = high and Opamp bias = high is not supported at 3.3 V and 2.7 V.

**Table 33. 5-V AC Operational Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $t_{ROA}$ | Rising settling time from 80% of ΔV to 0.1% of ΔV (10 pF load, unity gain)<br>Power = low, Opamp bias = low<br>Power = medium, Opamp bias = high<br>Power = high, Opamp bias = high | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>3.9<br>0.72<br>0.62 | <br>µs<br>µs<br>µs |
| $t_{SOA}$ | Falling settling time from 20% of ΔV to 0.1% of ΔV (10 pF load, unity gain)<br>Power = low, Opamp bias = low<br>Power = medium, Opamp bias = high<br>Power = high, Opamp bias = high | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>5.9<br>0.92<br>0.72 | <br>µs<br>µs<br>µs |
| $SR_{ROA}$ | Rising slew rate (20% to 80%) (10 pF load, unity gain)<br>Power = low, Opamp bias = low<br>Power = medium, Opamp bias = high<br>Power = high, Opamp bias = high | <br>0.15<br>1.7<br>6.5 | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>V/µs<br>V/µs<br>V/µs |
| $SR_{FOA}$ | Falling slew rate (20% to 80%) (10 pF load, unity gain)<br>Power = low, Opamp bias = low<br>Power = medium, Opamp bias = high<br>Power = high, Opamp bias = high | <br>0.01<br>0.5<br>4.0 | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>V/µs<br>V/µs<br>V/µs |
| $BW_{OA}$ | Gain bandwidth product<br>Power = low, Opamp bias = low<br>Power = medium, Opamp bias = high<br>Power = high, Opamp bias = high | <br>0.75<br>3.1<br>5.4 | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>MHz<br>MHz<br>MHz |
| $E_{NOA}$ | Noise at 1 kHz (Power = medium, Opamp bias = high) | – | 100 | – | nV/rt-Hz |

**Table 34. 3.3-V AC Operational Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $t_{ROA}$ | Rising settling time from 80% of ΔV to 0.1% of ΔV (10 pF load, unity gain)<br>Power = low, Opamp bias = low<br>Power = medium, Opamp bias = high | <br>–<br>– | <br>–<br>– | <br>3.92<br>0.72 | <br>µs<br>µs |
| $t_{SOA}$ | Falling settling time from 20% of ΔV to 0.1% of ΔV (10 pF load, unity gain)<br>Power = low, Opamp bias = low<br>Power = medium, Opamp bias = high | <br>–<br>– | <br>–<br>– | <br>5.41<br>0.72 | <br>µs<br>µs |
| $SR_{ROA}$ | Rising slew rate (20% to 80%) (10 pF load, unity gain)<br>Power = low, Opamp bias = low<br>Power = medium, Opamp bias = high | <br>0.31<br>2.7 | <br>–<br>– | <br>–<br>– | <br>V/µs<br>V/µs |
| $SR_{FOA}$ | Falling slew rate (20% to 80%) (10 pF load, unity gain)<br>Power = low, Opamp bias = low<br>Power = medium, Opamp bias = high | <br>0.24<br>1.8 | <br>–<br>– | <br>–<br>– | <br>V/µs<br>V/µs |
| $BW_{OA}$ | Gain bandwidth product<br>Power = low, Opamp bias = low<br>Power = medium, Opamp bias = high | <br>0.67<br>2.8 | <br>–<br>– | <br>–<br>– | <br>MHz<br>MHz |
| $E_{NOA}$ | Noise at 1 kHz (Power = medium, Opamp bias = high) | – | 100 | – | nV/rt-Hz |

**Table 41. 2.7-V AC Analog Output Buffer Specifications**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $t_{ROB}$ | Rising settling time to 0.1%, 1 V Step, 100 pF load<br>Power = low<br>Power = high | <br>–<br>– | <br>–<br>– | <br>4<br>4 | <br>µs<br>µs |
| $t_{SOB}$ | Falling settling time to 0.1%, 1 V Step, 100 pF load<br>Power = low<br>Power = high | <br>–<br>– | <br>–<br>– | <br>3<br>3 | <br>µs<br>µs |
| $SR_{ROB}$ | Rising slew rate (20% to 80%), 1 V Step, 100 pF load<br>Power = low<br>Power = high | <br>0.4<br>0.4 | <br>–<br>– | <br>–<br>– | <br>V/µs<br>V/µs |
| $SR_{FOB}$ | Falling slew rate (80% to 20%), 1 V Step, 100 pF load<br>Power = low<br>Power = high | <br>0.4<br>0.4 | <br>–<br>– | <br>–<br>– | <br>V/µs<br>V/µs |
| $BW_{OB}$ | Small signal bandwidth, 20 $mV_{pp}$, 3dB BW, 100 pF load<br>Power = low<br>Power = high | <br>0.6<br>0.6 | <br>–<br>– | <br>–<br>– | <br>MHz<br>MHz |
| $BW_{OB}$ | Large signal bandwidth, 1 $V_{pp}$, 3dB BW, 100 pF load<br>Power = low<br>Power = high | <br>180<br>180 | <br>–<br>– | <br>–<br>– | <br>kHz<br>kHz |

*AC External Clock Specifications*

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ $T_A$ ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

**Table 42. 5-V AC External Clock Specifications**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $F_{OSCEXT}$ | Frequency | 0.093 | – | 24.6 | MHz |
| – | High period | 20.6 | – | 5300 | ns |
| – | Low period | 20.6 | – | – | ns |
| – | Power-up IMO to switch | 150 | – | – | µs |

**Table 43. 3.3-V AC External Clock Specifications**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $F_{OSCEXT}$ | Frequency with CPU clock divide by 1[32] | 0.093 | – | 12.3 | MHz |
| $F_{OSCEXT}$ | Frequency with CPU clock divide by 2 or greater[33] | 0.186 | – | 24.6 | MHz |
| – | High period with CPU clock divide by 1 | 41.7 | – | 5300 | ns |
| – | Low period with CPU clock divide by 1 | 41.7 | – | – | ns |
| – | Power-up IMO to switch | 150 | – | – | µs |

**Notes**
32. Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
33. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met

**Table 44. 2.7-V AC External Clock Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{OSCEXT}$ | Frequency with CPU clock divide by 1[34] | 0.093 | – | 12.3 | MHz | |
| $F_{OSCEXT}$ | Frequency with CPU clock divide by 2 or greater[35] | 0.186 | – | 12.3 | MHz | |
| – | High period with CPU clock divide by 1 | 41.7 | – | 5300 | ns | |
| – | Low period with CPU clock divide by 1 | 41.7 | – | – | ns | |
| – | Power-up IMO to switch | 150 | – | – | µs | |

*AC Programming Specifications*

Table 45 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ $T_A$ ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

**Table 45. AC Programming Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $t_{RSCLK}$ | Rise time of SCLK | 1 | – | 20 | ns | |
| $t_{FSCLK}$ | Fall time of SCLK | 1 | – | 20 | ns | |
| $t_{SSCLK}$ | Data setup time to falling edge of SCLK | 40 | – | – | ns | |
| $t_{HSCLK}$ | Data hold time from falling edge of SCLK | 40 | – | – | ns | |
| $F_{SCLK}$ | Frequency of SCLK | 0 | – | 8 | MHz | |
| $t_{ERASEB}$ | Flash erase time (block) | – | 20 | – | ms | |
| $t_{WRITE}$ | Flash block write time | – | 80 | – | ms | |
| $t_{DSCLK}$ | Data out delay from falling edge of SCLK | – | – | 45 | ns | $V_{DD} > 3.6$ |
| $t_{DSCLK3}$ | Data out delay from falling edge of SCLK | – | – | 50 | ns | $3.0 \le V_{DD} \le 3.6$ |
| $t_{DSCLK2}$ | Data out delay from falling edge of SCLK | – | – | 70 | ns | $2.4 \le V_{DD} \le 3.0$ |
| $t_{ERASEALL}$ | Flash erase time (Bulk) | – | 20 | – | ms | Erase all blocks and protection fields at once |
| $t_{PROGRAM_HOT}$ | Flash block erase + flash block write time | – | – | 200[36] | ms | 0 °C ≤ Tj ≤ 100 °C |
| $t_{PROGRAM_COLD}$ | Flash block erase + flash block write time | – | – | 400[36] | ms | –40 °C ≤ Tj ≤ 0 °C |

**Notes**
34. Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
35. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
36. For the full industrial range, you must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs application note Design Aids – Reading and Writing PSoC® Flash – AN2015 for more information.

**Figure 20. 20-Pin (210-Mil) SSOP**

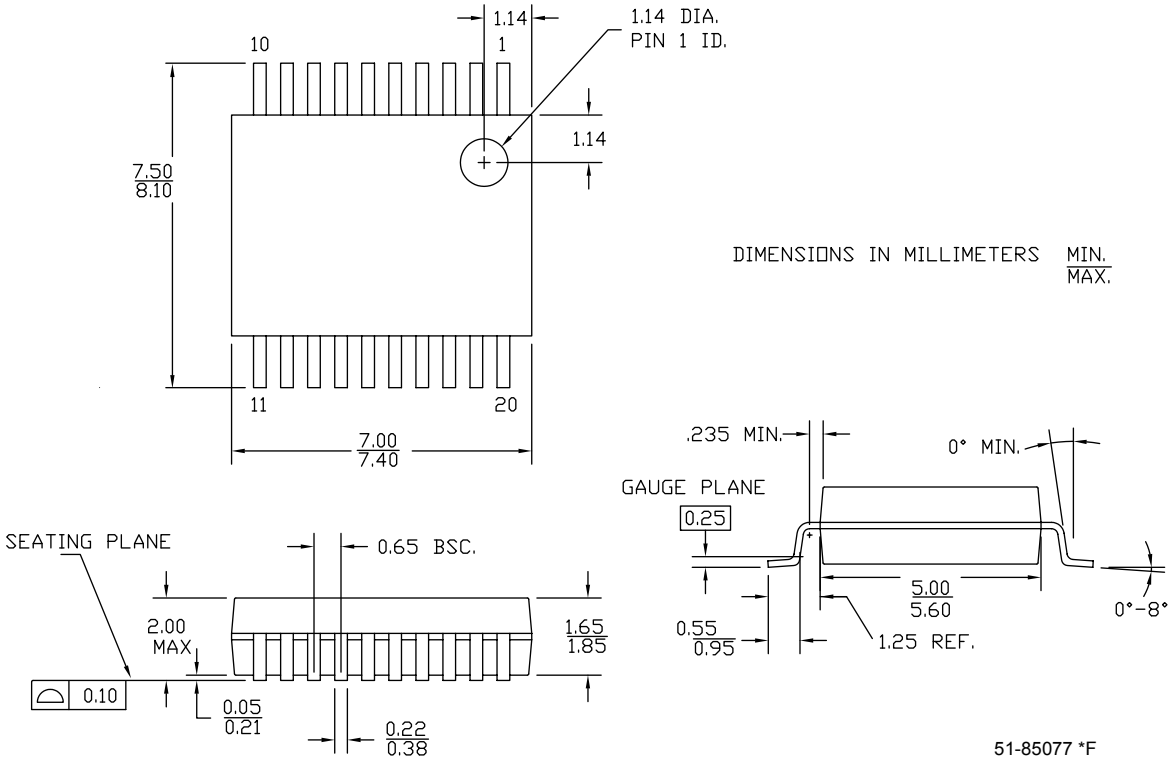



**Figure 21. 20-Pin (300-Mil) Molded SOIC**

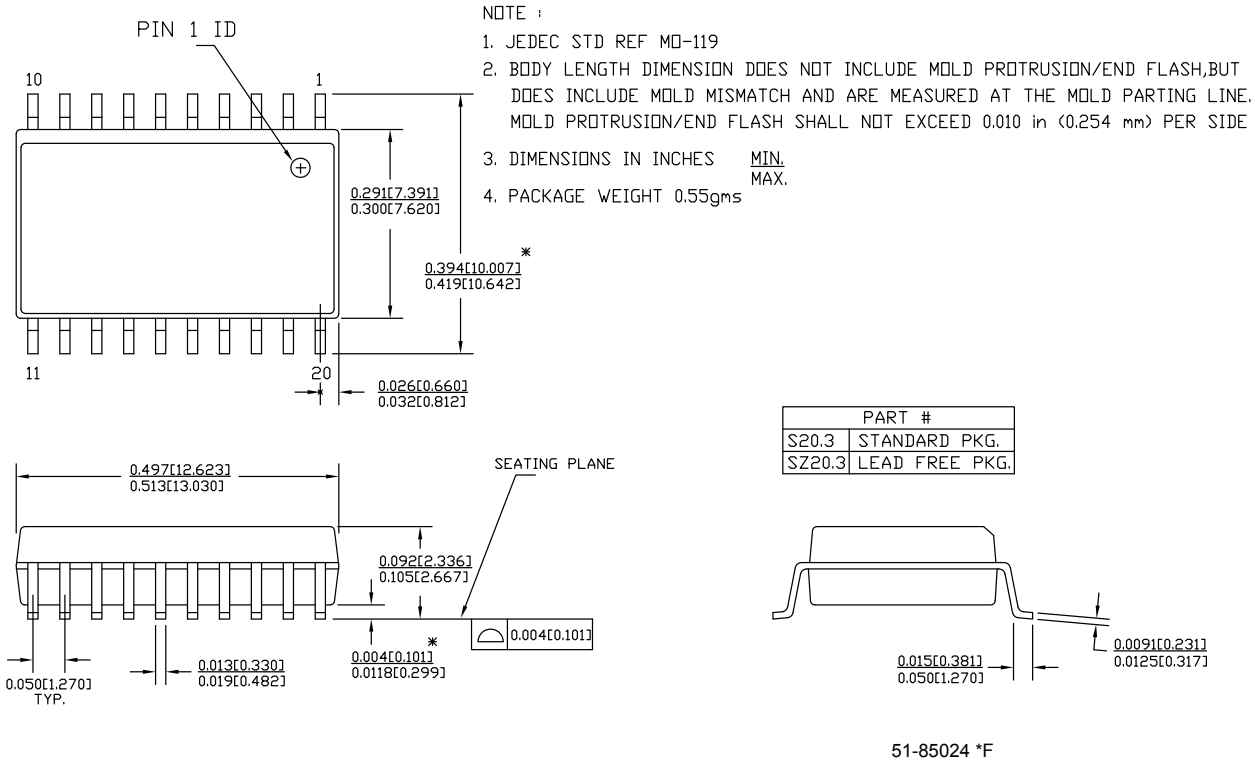


**Figure 22. 28-Pin (300-Mil) Molded DIP**

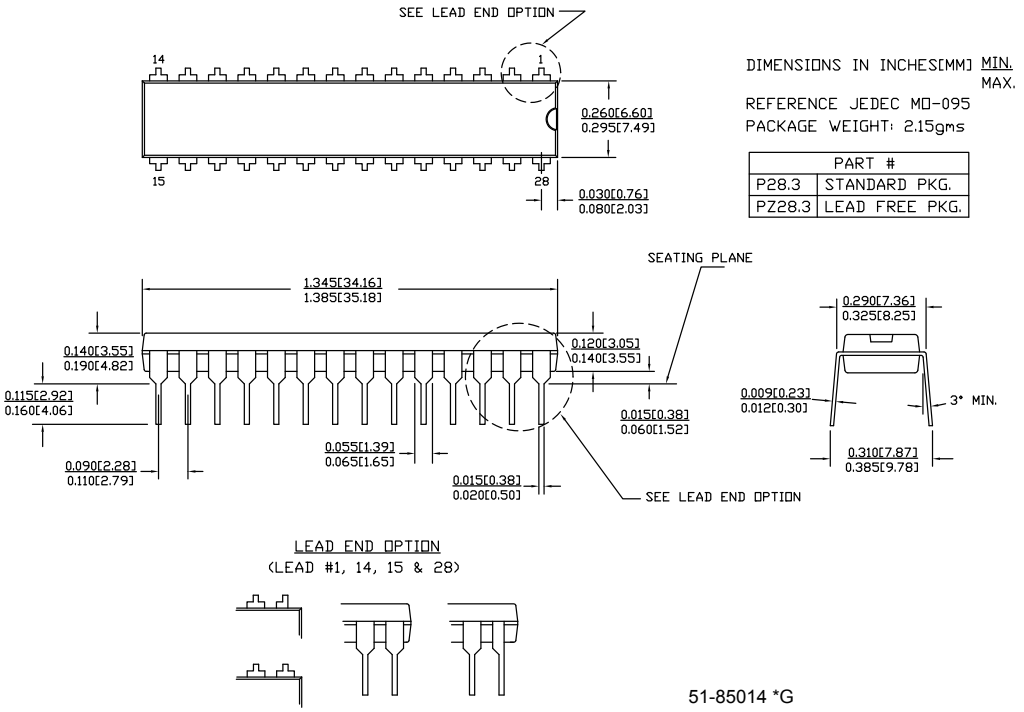



**Figure 23. 28-Pin (210-Mil) SSOP**

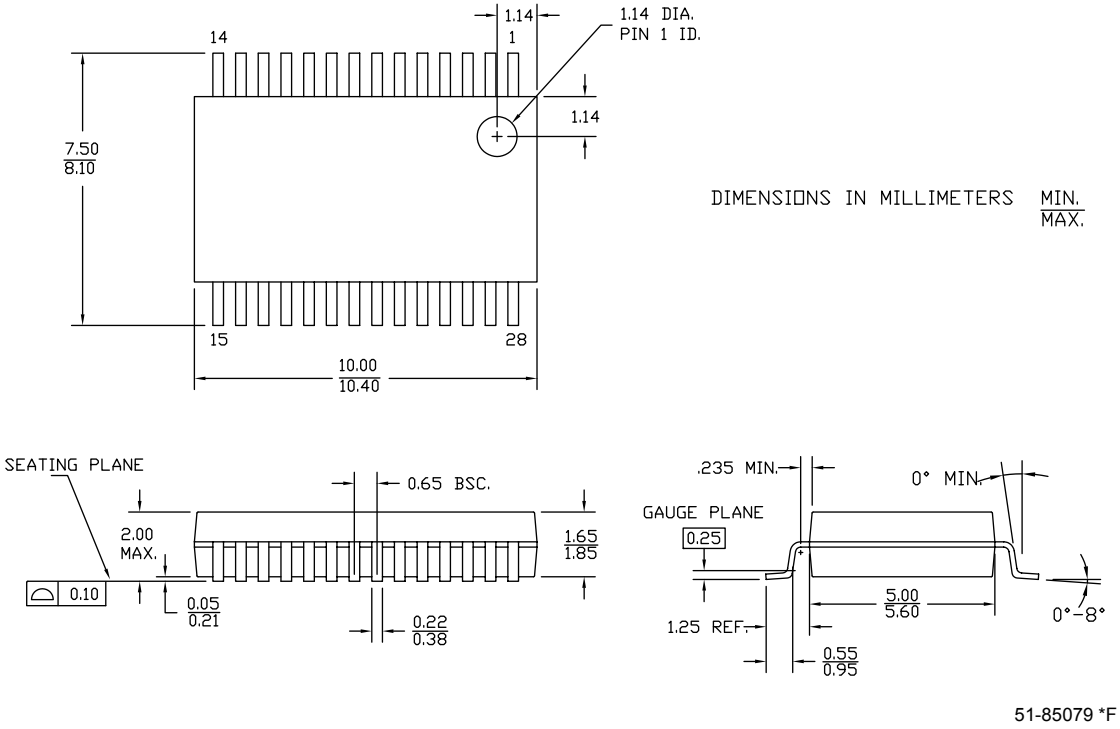
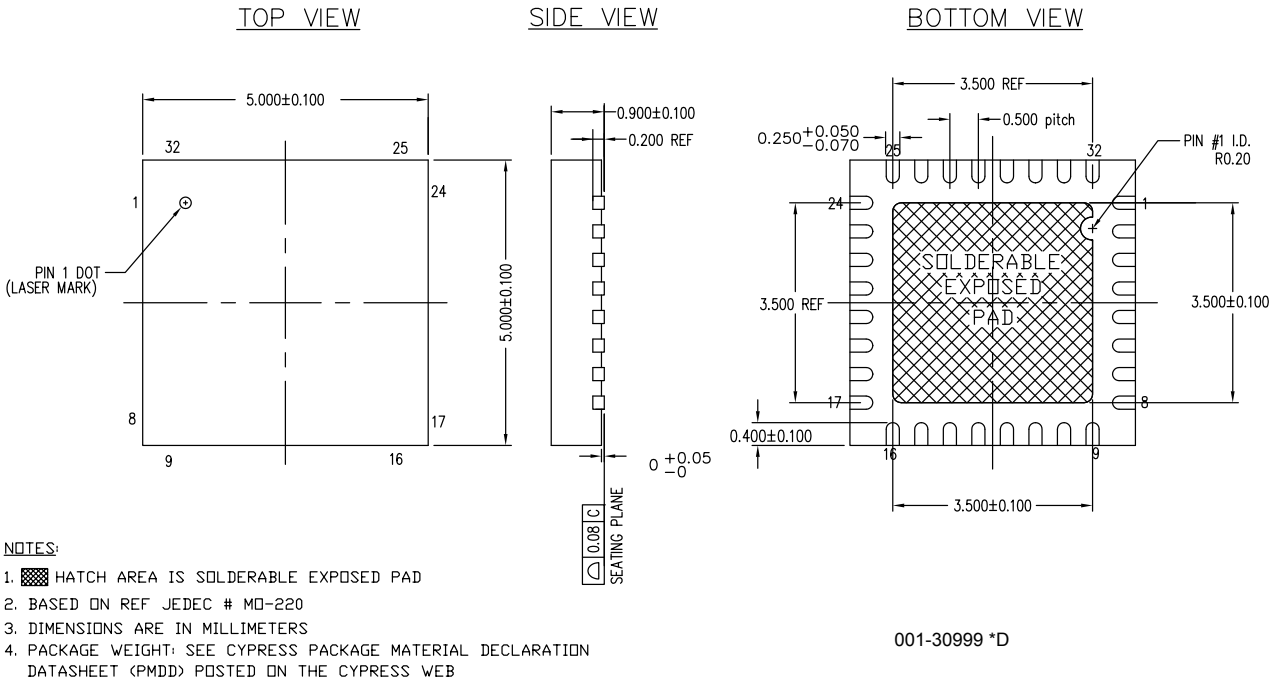
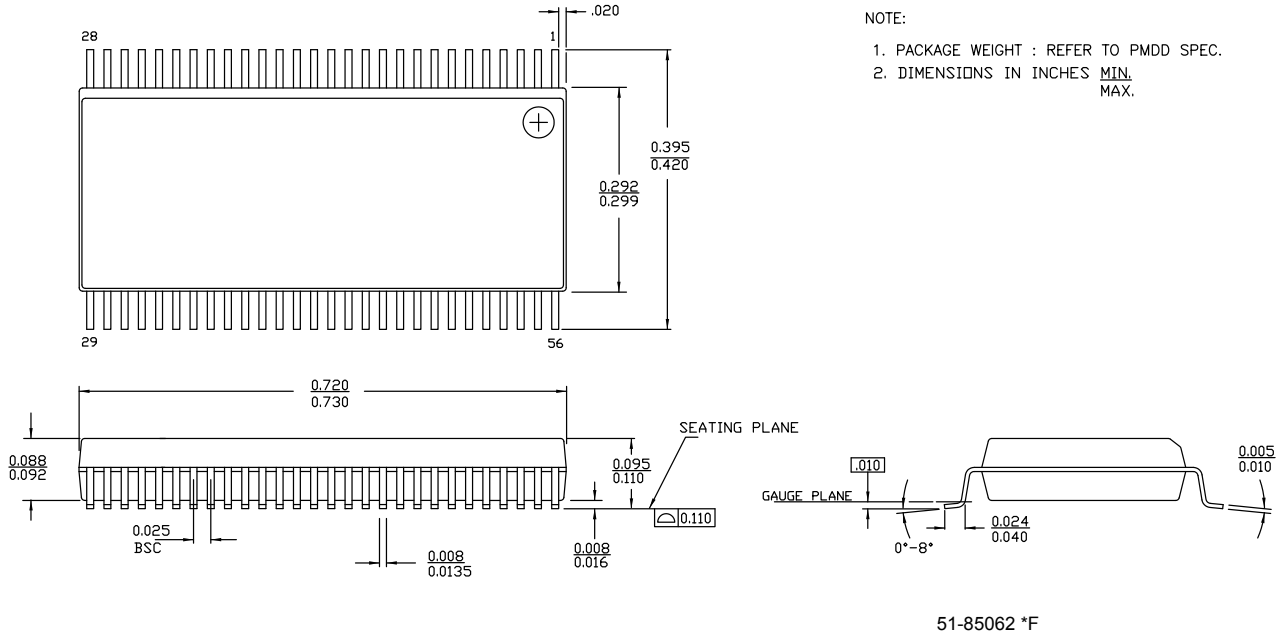


**Figure 25. 32-Pin Sawn QFN Package**




**Important Note** For information on the preferred dimensions for mounting QFN packages, see the application note, *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages* available at http://www.amkor.com.

**Figure 26. 56-Pin (300-Mil) SSOP**



## Glossary (continued)

| | |
|---|---|
| microcontroller | An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor. |
| mixed-signal | The reference to a circuit containing both analog and digital techniques and components. |
| modulator | A device that imposes a signal on a carrier. |
| noise | 1. A disturbance that affects a signal and that may distort the information carried by the signal.<br>2. The random variations of one or more characteristics of any entity such as voltage, current, or data. |
| oscillator | A circuit that may be crystal controlled and is used to generate a clock frequency. |
| parity | A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity). |
| phase-locked loop (PLL) | An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal. |
| pinouts | The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names. |
| port | A group of pins, usually eight. |
| power on reset (POR) | A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is one type of hardware reset. |
| PSoC® | Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress. |
| PSoC Designer™ | The software for Cypress' Programmable System-on-Chip technology. |
| pulse width modulator (PWM) | An output in the form of duty cycle which varies as a function of the applied measurand |
| RAM | An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in. |
| register | A storage device with a specific capacity, such as a bit or byte. |
| reset | A means of bringing a system back to a know state. See hardware reset and software reset. |
| ROM | An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in. |
| serial | 1. Pertaining to a process in which all events occur one after the other.<br>2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel. |
| settling time | The time it takes for an output signal or value to stabilize after the input has changed from one value to another. |

# Errata

This section describes the errata for the CY8C24xxxA device family. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

## Part Numbers Affected

| Part Number | Ordering Information |
|---|---|
| CY8C24123A | CY8C24123A-24PXI |
| | CY8C24123A-24SXI |
| | CY8C24123A-24SXIT |
| | CY8C24223A-24PXI |
| | CY8C24223A-24PVXI |
| | CY8C24223A-24PVXIT |
| | CY8C24223A-24SXI |
| | CY8C24223A-24SXIT |
| | CY8C24423A-24PXI |
| | CY8C24423A-24PVXI |
| | CY8C24423A-24PVXIT |
| | CY8C24423A-24SXI |
| | CY8C24423A-24SXIT |
| | CY8C24423A-24LFXI |
| | CY8C24423A-24LTXI |
| | CY8C24423A-24LTXIT |
| | CY8C24000A-24PVXI |

## CY8C24123A Qualification Status

Product Status: Production

## CY8C24123A Errata Summary

The following table defines the errata applicability to available CY8C24123A family devices.

| Items | Part Number | Silicon Revision | Fix Status |
|---|---|---|---|
| [1.]. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes | CY8C24123A | *A | No silicon fix planned. Workaround is required. |

1. **Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes**
   - **Problem Definition**
     Asynchronous Digital Communications Interfaces may fail framing beyond 0 to 70 °C. This problem does not affect end-product usage between 0 and 70 °C.
   - **Parameters Affected**
     The IMO frequency tolerance. The worst case deviation when operated below 0°C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.
   - **Trigger Condition(S)**
     The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the data sheet limit of ±2.5% when operated beyond the temperature range of 0 to +70 °C.
   - **Scope of Impact**
     This problem may affect UART, IrDA, and FSK implementations.
   - **Workaround**
     Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.
   - **Fix Status**
     Silicon fix is not planned. The workaround mentioned above should be used.

## Document History Page (continued)

| Document Title: CY8C24123A/CY8C24223A/CY8C24423A, PSoC® Programmable System-on-Chip<br>Document Number: 38-12028 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *T | 4066332 | PMAD | 07/17/2013 | Added Errata Footnotes (Note 1, 19).<br><br>Updated PSoC Functional Overview:<br>Updated PSoC Core:<br>Added Note 1 and referred the same note in 4th paragraph in PSoC Core.<br><br>Updated Electrical Specifications:<br>Updated AC Electrical Characteristics:<br>Updated AC Chip-Level Specifications:<br>Added Note 19 and referred the same note in $F_{IMO24}$ parameter.<br>Updated minimum and maximum values of $F_{IMO24}$ parameter.<br>Updated AC Digital Block Specifications:<br>Replaced all instances of maximum value “49.2” with “50.4” and “24.6” with “25.2” in Table 37.<br><br>Updated in new template. |
| *U | 4479672 | RJVB | 08/20/2014 | Updated Packaging Information:<br>Updated Packaging Dimensions:<br>spec 51-85011 – Changed revision from *C to *D.<br>spec 51-85024 – Changed revision from *E to *F.<br>spec 51-85026 – Changed revision from *G to *H.<br><br>Updated Errata:<br>Updated CY8C24123A Errata Summary:<br>Updated details in “Fix Status” column in the table.<br>Updated details in “Fix Status” bulleted point below the table.<br><br>Completing Sunset Review. |
| *V | 4622083 | RKRM | 01/13/2015 | Added More Information section. |

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