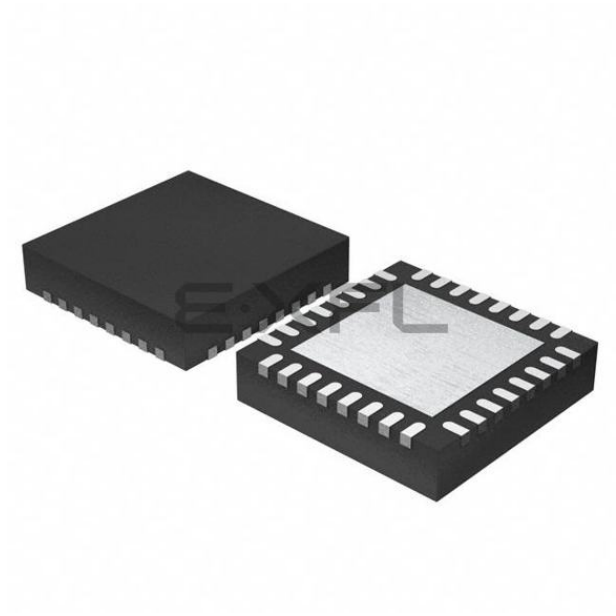

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	A/D 10x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24423a-24ltxit

Contents

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

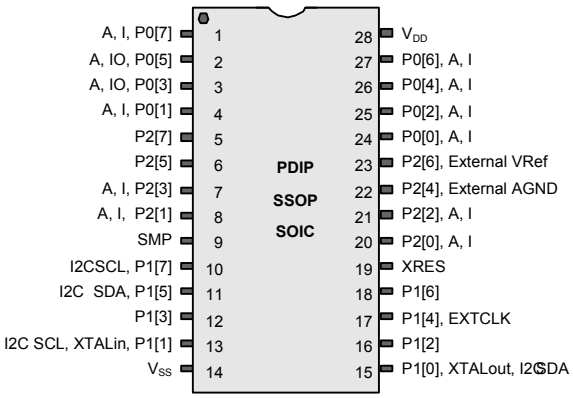
28-Pin Part Pinout

Table 4. 28-Pin PDIP, SSOP, and SOIC

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I/O	P0[5]	Analog column mux input and column output
3	I/O	I/O	P0[3]	Analog column mux input and column output
4	I/O	I	P0[1]	Analog column mux input
5	I/O		P2[7]	
6	I/O		P2[5]	
7	I/O	I	P2[3]	Direct switched capacitor block input
8	I/O	I	P2[1]	Direct switched capacitor block input
9	Power		SMP	SMP connection to external components required
10	I/O		P1[7]	I^2C SCL
11	I/O		P1[5]	I^2C SDA
12	I/O		P1[3]	
13	I/O		P1[1]	XTALin, I^2C SCL, ISSP-SCLK[6]
14	Power		V_{SS}	Ground connection.
15	I/O		P1[0]	XTALout, I^2C SDA, ISSP-SDATA[6]
16	I/O		P1[2]	
17	I/O		P1[4]	Optional EXTCLK
18	I/O		P1[6]	
19	Input		XRES	Active high external reset with internal pull-down
20	I/O	I	P2[0]	Direct switched capacitor block input
21	I/O	I	P2[2]	Direct switched capacitor block input
22	I/O		P2[4]	External analog ground (AGND)
23	I/O		P2[6]	External voltage reference (V_{REF})
24	I/O	I	P0[0]	Analog column mux input
25	I/O	I	P0[2]	Analog column mux input
26	I/O	I	P0[4]	Analog column mux input
27	I/O	I	P0[6]	Analog column mux input
28	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 6. CY8C24423A 28-Pin PSoC Device



Not for Production

Note
6. These are the ISSP pins, which are not high Z at POR. See the PSoC Technical Reference Manual for details.

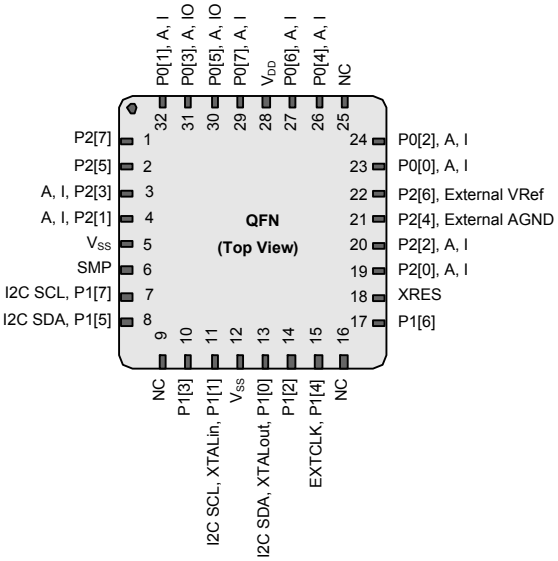
32-Pin Part Pinout

Table 5. 32-Pin QFN[7]

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O		P2[7]	
2	I/O		P2[5]	
3	I/O	I	P2[3]	Direct switched capacitor block input
4	I/O	I	P2[1]	Direct switched capacitor block input
5	Power		V_{SS}	Ground connection
6	Power		SMP	SMP connection to external components required
7	I/O		P1[7]	I^2C SCL
8	I/O		P1[5]	I^2C SDA
9			NC	No connection. Pin must be left floating
10	I/O		P1[3]	
11	I/O		P1[1]	XTALin, I^2C SCL, ISSP-SCLK[8]
12	Power		V_{SS}	Ground Connection
13	I/O		P1[0]	XTALout, I^2C SDA, ISSP-SDATA[8]
14	I/O		P1[2]	
15	I/O		P1[4]	Optional EXTCLK
16			NC	No connection. Pin must be left floating
17	I/O		P1[6]	
18	Input		XRES	Active high external reset with internal pull-down
19	I/O	I	P2[0]	Direct switched capacitor block input
20	I/O	I	P2[2]	Direct switched capacitor block input
21	I/O		P2[4]	External AGND
22	I/O		P2[6]	External V_{REF}
23	I/O	I	P0[0]	Analog column mux input
24	I/O	I	P0[2]	Analog column mux input
25			NC	No connection. Pin must be left floating
26	I/O	I	P0[4]	Analog column mux input
27	I/O	I	P0[6]	Analog column mux input
28	Power		V_{DD}	Supply voltage
29	I/O	I	P0[7]	Analog column mux input
30	I/O	I/O	P0[5]	Analog column mux input and column output
31	I/O	I/O	P0[3]	Analog column mux input and column output
32	I/O	I	P0[1]	Analog column mux input

LEGEND: A = Analog, I = Input, and O = Output.

Figure 7. CY8C24423A 32-Pin PSoC Device



Notes
7. The center pad on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
8. These are the ISSP pins, which are not high Z at POR. See the PSoC Technical Reference Manual for details.

56-Pin Part Pinout

The 56-pin SSOP part is for the CY8C24000A On-Chip Debug (OCD) PSoC device.

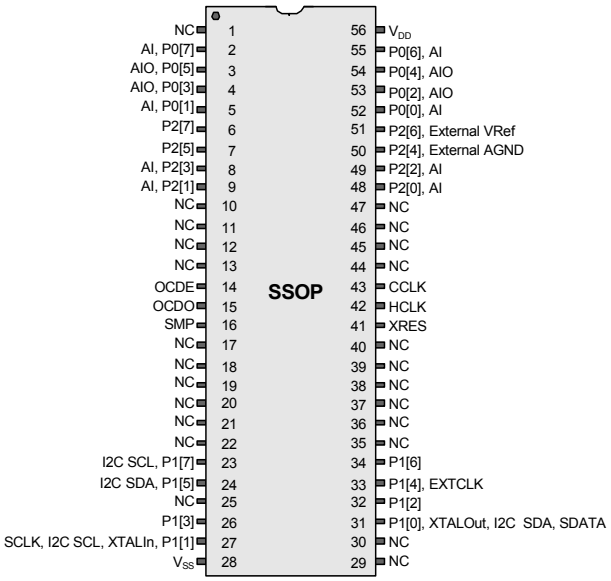
Note This part is only used for in-circuit debugging. It is NOT available for production.

Table 6. 56-Pin SSOP OCD

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1			NC	No connection. Pin must be left floating
2	I/O	I	P0[7]	Analog column mux input
3	I/O	I	P0[5]	Analog column mux input and column output
4	I/O	I	P0[3]	Analog column mux input and column output
5	I/O	I	P0[1]	Analog column mux input
6	I/O		P2[7]	
7	I/O		P2[5]	
8	I/O	I	P2[3]	Direct switched capacitor block input
9	I/O	I	P2[1]	Direct switched capacitor block input
10			NC	No connection. Pin must be left floating
11			NC	No connection. Pin must be left floating
12			NC	No connection. Pin must be left floating
13			NC	No connection. Pin must be left floating
14	OCD		OCDE	OCD even data I/O
15	OCD		OCDO	OCD odd data output
16	Power		SMP	SMP connection to required external components
17			NC	No connection. Pin must be left floating
18			NC	No connection. Pin must be left floating
19			NC	No connection. Pin must be left floating
20			NC	No connection. Pin must be left floating
21			NC	No connection. Pin must be left floating
22			NC	No connection. Pin must be left floating
23	I/O		P1[7]	I^2C SCL
24	I/O		P1[5]	I^2C SDA
25			NC	No connection. Pin must be left floating
26	I/O		P1[3]	
27	I/O		P1[1]	XTALin, I^2C SCL, ISSP-SCLK[9]
28	Power		V_{DD}	Supply voltage
29			NC	No connection. Pin must be left floating
30			NC	No connection. Pin must be left floating
31	I/O		P1[0]	XTALout, I^2C SDA, ISSP-SDATA[9]
32	I/O		P1[2]	
33	I/O		P1[4]	Optional EXTCLK
34	I/O		P1[6]	
35			NC	No connection. Pin must be left floating
36			NC	No connection. Pin must be left floating
37			NC	No connection. Pin must be left floating
38			NC	No connection. Pin must be left floating
39			NC	No connection. Pin must be left floating
40			NC	No connection. Pin must be left floating
41	Input		XRES	Active high external reset with internal pull-down.
42	OCD		HCLK	OCD high speed clock output.
43	OCD		CCLK	OCD CPU clock output.
44			NC	No connection. Pin must be left floating
45			NC	No connection. Pin must be left floating
46			NC	No connection. Pin must be left floating
47			NC	No connection. Pin must be left floating
48	I/O	I	P2[0]	Direct switched capacitor block input.
49	I/O	I	P2[2]	Direct switched capacitor block input.
50	I/O		P2[4]	External AGND.
51	I/O		P2[6]	External V_{REF}.
52	I/O	I	P0[0]	Analog column mux input.
53	I/O	I	P0[2]	Analog column mux input and column output.
54	I/O	I	P0[4]	Analog column mux input and column output.
55	I/O	I	P0[6]	Analog column mux input.
56	Power		V_{DD}	Supply voltage.

LEGEND: A = Analog, I = Input, O = Output, and OCD = On-Chip Debug.

Figure 8. CY8C24000A 56-Pin PSoC Device



Note

9. These are the ISSP pins, which are not high Z at POR. See the PSoC Technical Reference Manual for details.

Table 0-1. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASC10CR0	80	RW		C0	
PRT0DM1	01	RW		41		ASC10CR1	81	RW		C1	
PRT0IC0	02	RW		42		ASC10CR2	82	RW		C2	
PRT0IC1	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DM0	04	RW		44		ASD11CR0	84	RW		C4	
PRT1DM1	05	RW		45		ASD11CR1	85	RW		C5	
PRT1IC0	06	RW		46		ASD11CR2	86	RW		C6	
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50		ASD20CR0	90	RW	GDI_O_IN	D0	RW
	11			51		ASD20CR1	91	RW	GDI_E_IN	D1	RW
	12			52		ASD20CR2	92	RW	GDI_O_OU	D2	RW
	13			53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW		D6	
	17			57		ASC21CR3	97	RW		D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW		6C			AC			EC	
DCB03IN	2D	RW		6D			AD			ED	
DCB03OU	2E	RW		6E			AE			EE	
	2F			6F			AF			EF	
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 16. 2.7-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 1.65 1.32 –	 10 8 –	 mV mV mV	Power = high, Opamp bias = high setting is not allowed for 2.7 V V_{DD} operation.
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	20	–	pA	Gross tested to 1 µA
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0.2	–	V_{DD} – 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain Power = low, Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 60 60 80	 – – –	 – – –	 dB dB dB	Specification is applicable at low Opamp bias. For high Opamp bias mode, (except high power, high Opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.2	 – – –	 – – –	 V V V	Power = high, Opamp bias = high setting is not allowed for 2.7 V V_{DD} operation.
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 – – –	 – – –	 0.2 0.2 0.2	 V V V	Power = high, Opamp bias = high setting is not allowed for 2.7 V V_{DD} operation.
I_{SOA}	Supply current (including associated AGND buffer) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – – – –	 150 300 600 1200 2400 –	 200 400 800 1600 3200 –	 µA µA µA µA µA µA	Power = high, Opamp bias = high setting is not allowed for 2.7 V V_{DD} operation.
$PSRR_{OA}$	Supply voltage rejection ratio	64	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$

DC Low Power Comparator Specifications

Table 17 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V at 25 °C and are for design guidance only.

Table 17. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	V_{DD} – 1	V	
I_{SLPC}	LPC supply current	–	10	40	µA	
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV	

Table 24. 2.7-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	All power settings Not allowed at 2.7 V	–	–	–	–	–	–	–
0b001	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.739	P2[4] + P2[6] – 0.016	P2[4] + P2[6] + 0.759	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 1.675	P2[4] – P2[6] + 0.013	P2[4] – P2[6] + 1.825	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.098	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.067	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.308	P2[4] – P2[6] + 0.004	P2[4] – P2[6] + 0.362	V
	RefPower = low Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.042	P2[4] + P2[6] – 0.005	P2[4] + P2[6] + 0.035	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.030	P2[4] – P2[6]	P2[4] – P2[6] + 0.030	V
	RefPower = low Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.367	P2[4] + P2[6] – 0.005	P2[4] + P2[6] + 0.308	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = V_{DD}/2, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.345	P2[4] – P2[6]	P2[4] – P2[6] + 0.301	V
0b010	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.100	V_{DD} – 0.003	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.038	V_{DD}/2	V_{DD}/2 + 0.036	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.016	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.065	V_{DD} – 0.002	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.025	V_{DD}/2	V_{DD}/2 + 0.023	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.012	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.054	V_{DD} – 0.002	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.024	V_{DD}/2 – 0.001	V_{DD}/2 + 0.020	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.012	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.042	V_{DD} – 0.002	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.027	V_{DD}/2 – 0.001	V_{DD}/2 + 0.022	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.001	V_{SS} + 0.010	V
	RefPower = low Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.042	V_{DD} – 0.002	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.028	V_{DD}/2 – 0.001	V_{DD}/2 + 0.023	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.001	V_{SS} + 0.010	V
	RefPower = low Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.036	V_{DD} – 0.002	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.184	V_{DD}/2 – 0.001	V_{DD}/2 + 0.159	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.001	V_{SS} + 0.009	V

DC POR, SMP, and LVD Specifications

Table 24 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the PSoC Programmable Sytem-on-Chip Technical Reference Manual for more information on the VLT_CR register.

Table 26. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip					V_{DD} must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b		2.82	2.95	V	
V_{PPOR2}	PORLEV[1:0] = 10b		4.55	4.70	V	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.40	2.45	2.51[12]	V	
V_{LVD1}	VM[2:0] = 001b	2.85	2.92	2.99[13]	V	
V_{LVD2}	VM[2:0] = 010b	2.95	3.02	3.09	V	
V_{LVD3}	VM[2:0] = 011b	3.06	3.13	3.20	V	
V_{LVD4}	VM[2:0] = 100b	4.37	4.48	4.55	V	
V_{LVD5}	VM[2:0] = 101b	4.50	4.64	4.75	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	
	V_{DD} value for SMP trip					
V_{PUMP0}	VM[2:0] = 000b	2.50	2.55	2.62[14]	V	
V_{PUMP1}	VM[2:0] = 001b	2.96	3.02	3.09	V	
V_{PUMP2}	VM[2:0] = 010b	3.03	3.10	3.16	V	
V_{PUMP3}	VM[2:0] = 011b	3.18	3.25	3.32[15]	V	
V_{PUMP4}	VM[2:0] = 100b	4.54	4.64	4.74	V	
V_{PUMP5}	VM[2:0] = 101b	4.62	4.73	4.83	V	
V_{PUMP6}	VM[2:0] = 110b	4.71	4.82	4.92	V	
V_{PUMP7}	VM[2:0] = 111b	4.89	5.00	5.12	V	

Notes
12. Always greater than 50 mV above V_{PPOR} (PORLEV=00) for falling supply.
13. Always greater than 50 mV above V_{PPOR} (PORLEV=01) for falling supply.
14. Always greater than 50 mV above V_{LVD0}.
15. Always greater than 50 mV above V_{LVD3}.

AC Electrical Characteristics

AC Chip-Level Specifications

These tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 29. 5-V and 3.3-V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}[19]	Internal main oscillator (IMO) frequency for 24 MHz	22.8	24	25.2[20,21]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 8 on page 18. SLIMO mode = 0.
F_{IMO6}	IMO frequency for 6 MHz	5.5	6	6.5[20,21]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 8 on page 18. SLIMO mode = 1.
F_{CPU1}	CPU frequency (5 V nominal)	0.937	24	24.6[20]	MHz	SLIMO mode = 0.
F_{CPU2}	CPU frequency (3.3 V nominal)	0.937	12	12.3[21]	MHz	SLIMO mode = 0.
F_{48M}	Digital PSoC block frequency	0	48	49.2[20,22]	MHz	Refer to the AC Digital Block Specifications.
F_{24M}	Digital PSoC block frequency	0	24	24.6[22]	MHz	
F_{32K1}	ILO frequency	15	32	64	kHz	
F_{32K2}	External crystal oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on timing this
F_{PLL}	PLL frequency	–	23.986	–	MHz	Is a multiple (x732) of crystal frequency.
$T_{PLLSLEW}$	PLL lock time	0.5	–	10	ms	
$T_{PLLSLEWSLOW}$	PLL lock time for low gain setting	0.5	–	50	ms	
T_{OS}	External crystal oscillator startup to 1%	–	1700	2620	ms	
T_{OSACC}	External crystal oscillator startup to 100 ppm	–	2800	3800	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{osacc} period. Correct operation assumes a properly loaded 1 µW maximum drive level 32.768 kHz crystal. 3.0 V ≤ V_{DD} ≤ 5.5 V, –40 °C ≤ T_A ≤ 85 °C.
t_{XRST}	External reset pulse width	10	–	–	µs	

Notes
19. Errata: When the device is operated within 0 °C to 70 °C, the frequency tolerance is reduced to ±2.5%, but if operated at extreme temperature (below 0°C or above 70 °C), frequency tolerance deviates from ±2.5% to ±5%. For more information, see "Errata" on page 67.
20. 4.75 V < V_{DD} < 5.25 V.
21. 3.0 V < V_{DD} < 3.6 V. See application note Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 for information on trimming for operation at 3.3 V.
22. See the individual user module datasheets for information on maximum frequencies for user modules.
23. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

Figure 11. PLL Lock Timing Diagram

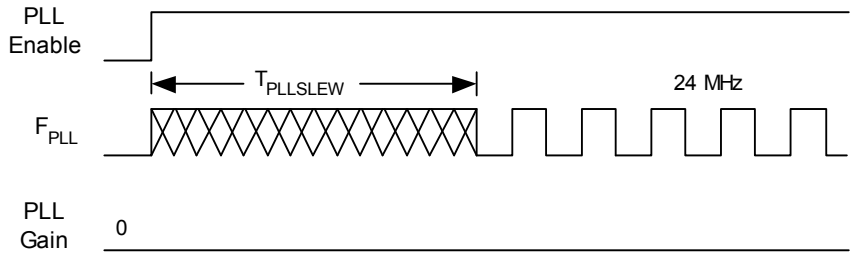


Figure 12. PLL Lock for Low Gain Setting Timing Diagram

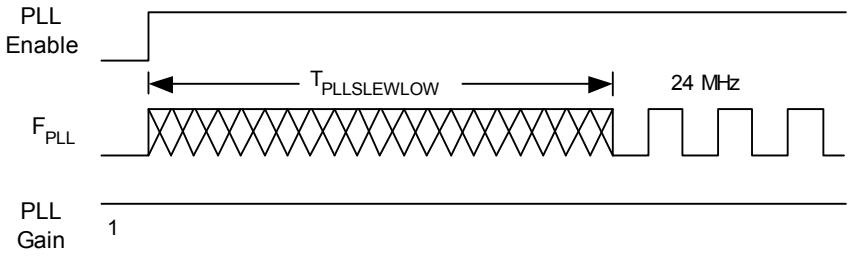
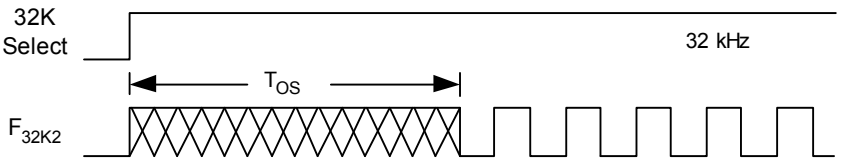


Figure 13. External Crystal Oscillator Startup Timing Diagram



AC Operational Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the analog continuous time PSoC block.

Power = high and Opamp bias = high is not supported at 3.3 V and 2.7 V.

Table 33. 5-V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
t_{ROA}	Rising settling time from 80% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs
t_{SOA}	Falling settling time from 20% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs
SR_{ROA}	Rising slew rate (20% to 80%) (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 0.15 1.7 6.5	 – – –	 – – –	 V/µs V/µs V/µs
SR_{FOA}	Falling slew rate (20% to 80%) (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 0.01 0.5 4.0	 – – –	 – – –	 V/µs V/µs V/µs
BW_{OA}	Gain bandwidth product Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz
E_{NOA}	Noise at 1 kHz (Power = medium, Opamp bias = high)	–	100	–	nV/rt-Hz

Table 34. 3.3-V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
t_{ROA}	Rising settling time from 80% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 – –	 – –	 3.92 0.72	 µs µs
t_{SOA}	Falling settling time from 20% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 – –	 – –	 5.41 0.72	 µs µs
SR_{ROA}	Rising slew rate (20% to 80%) (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 0.31 2.7	 – –	 – –	 V/µs V/µs
SR_{FOA}	Falling slew rate (20% to 80%) (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 0.24 1.8	 – –	 – –	 V/µs V/µs
BW_{OA}	Gain bandwidth product Power = low, Opamp bias = low Power = medium, Opamp bias = high	 0.67 2.8	 – –	 – –	 MHz MHz
E_{NOA}	Noise at 1 kHz (Power = medium, Opamp bias = high)	–	100	–	nV/rt-Hz

AC Digital Block Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 37. 5-V and 3.3-V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All functions	Block input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	50.4	MHz	
	V_{DD} < 4.75 V	–	–	25.2	MHz	
Timer	Input clock frequency					
	No capture, V_{DD} ≥ 4.75 V	–	–	50.4	MHz	
	No capture, V_{DD} < 4.75 V	–	–	25.2	MHz	
	With capture	–	–	25.2	MHz	
	Capture pulse width	50[30]	–	–	ns	
Counter	Input clock frequency					
	No enable input, V_{DD} ≥ 4.75 V	–	–	50.4	MHz	
	No enable input, V_{DD} < 4.75 V	–	–	25.2	MHz	
	With enable input	–	–	25.2	MHz	
	Enable input pulse width	50[30]	–	–	ns	
Dead Band	Kill pulse width					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50[30]	–	–	ns	
	Disable mode	50[30]	–	–	ns	
	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	50.4	MHz	
	V_{DD} < 4.75 V	–	–	25.2	MHz	
CRCPRS (PRS Mode)	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	50.4	MHz	
	V_{DD} < 4.75 V	–	–	25.2	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	25.2	MHz	
SPIM	Input clock frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	4.1	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_negated between transmissions	50[30]	–	–	ns	
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	50.4	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	25.2	MHz	
	V_{DD} < 4.75 V	–	–	25.2	MHz	
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	50.4	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	25.2	MHz	
	V_{DD} < 4.75 V	–	–	25.2	MHz	

Note
30. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

Table 41. 2.7-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
t_{ROB}	Rising settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high	 – –	 – –	 4 4	 µs µs
t_{SOB}	Falling settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high	 – –	 – –	 3 3	 µs µs
SR_{ROB}	Rising slew rate (20% to 80%), 1 V Step, 100 pF load Power = low Power = high	 0.4 0.4	 – –	 – –	 V/µs V/µs
SR_{FOB}	Falling slew rate (80% to 20%), 1 V Step, 100 pF load Power = low Power = high	 0.4 0.4	 – –	 – –	 V/µs V/µs
BW_{OB}	Small signal bandwidth, 20 mV_{pp}, 3dB BW, 100 pF load Power = low Power = high	 0.6 0.6	 – –	 – –	 MHz MHz
BW_{OB}	Large signal bandwidth, 1 V_{pp}, 3dB BW, 100 pF load Power = low Power = high	 180 180	 – –	 – –	 kHz kHz

AC External Clock Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 42. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz
–	High period	20.6	–	5300	ns
–	Low period	20.6	–	–	ns
–	Power-up IMO to switch	150	–	–	µs

Table 43. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency with CPU clock divide by 1[32]	0.093	–	12.3	MHz
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater[33]	0.186	–	24.6	MHz
–	High period with CPU clock divide by 1	41.7	–	5300	ns
–	Low period with CPU clock divide by 1	41.7	–	–	ns
–	Power-up IMO to switch	150	–	–	µs

Notes
32. Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
33. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met

AC I²C Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

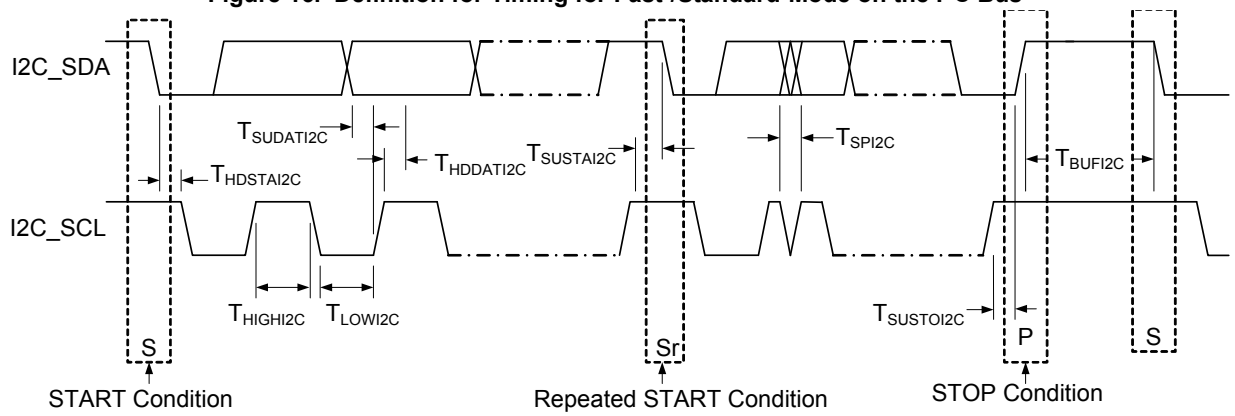
Table 46. AC Characteristics of the I²C SDA and SCL Pins for V_{DD} > 3.0 V

Symbol	Description	Standard-Mode		Fast-Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz
$t_{HDSTAI2C}$	Hold time (repeated) start condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs
t_{LOWI2C}	Low period of the SCL clock	4.7	–	1.3	–	µs
$t_{HIGHI2C}$	High period of the SCL clock	4.0	–	0.6	–	µs
$t_{SUSTAI2C}$	Setup time for a repeated start condition	4.7	–	0.6	–	µs
$t_{HDDATI2C}$	Data hold time	0	–	0	–	µs
$t_{SUDATI2C}$	Data setup time	250	–	100[37]	–	ns
$t_{SUSTOI2C}$	Setup time for stop condition	4.0	–	0.6	–	µs
t_{BUFI2C}	Bus free time between a stop and start condition	4.7	–	1.3	–	µs
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

Table 47. AC Characteristics of the I²C SDA and SCL Pins for V_{DD} < 3.0 V (Fast Mode Not Supported)

Symbol	Description	Standard-Mode		Fast-Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100	–	–	kHz
$t_{HDSTAI2C}$	Hold time (repeated) start condition. After this period, the first clock pulse is generated	4.0	–	–	–	µs
t_{LOWI2C}	Low period of the SCL clock	4.7	–	–	–	µs
$t_{HIGHI2C}$	High period of the SCL clock	4.0	–	–	–	µs
$t_{SUSTAI2C}$	Setup time for a repeated start condition	4.7	–	–	–	µs
$t_{HDDATI2C}$	Data hold time	0	–	–	–	µs
$t_{SUDATI2C}$	Data setup time	250	–	–	–	ns
$t_{SUSTOI2C}$	Setup time for stop condition	4.0	–	–	–	µs
t_{BUFI2C}	Bus free time between a stop and start condition	4.7	–	–	–	µs
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter	–	–	–	–	ns

Figure 16. Definition for Timing for Fast-/Standard-Mode on the I²C Bus



Note

37. A fast-mode I²C-bus device can be used in a Standard-Mode I²C-bus system, but the requirement t_{SUDAT} ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + t_{SUDAT} = 1000 + 250 = 1250 ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

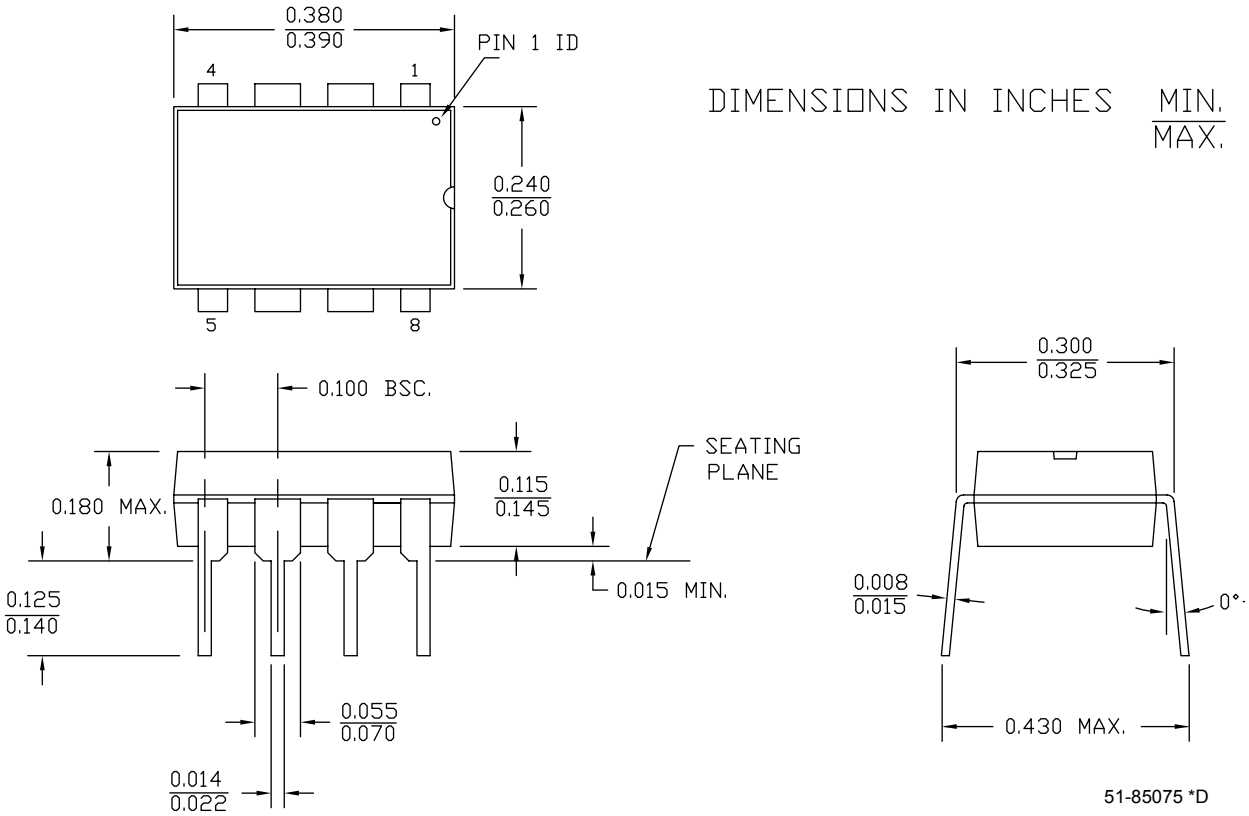
Packaging Information

This section illustrates the packaging specifications for the CY8C24x23A PSoC device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, see the emulator pod drawings at http://www.cypress.com/design/MR10161.

Packaging Dimensions

Figure 17. 8-Pin (300-Mil) PDIP



Ordering Information

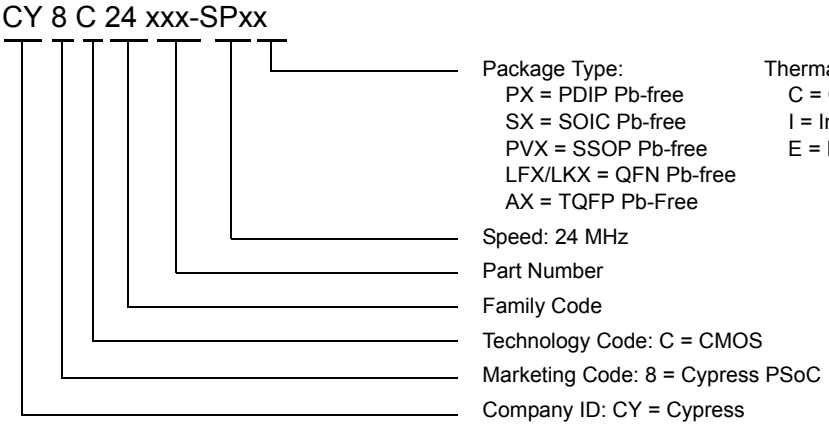
The following table lists the CY8C24x23A PSoC device's key package features and ordering codes.

Table 52. CY8C24x23A PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Switch Mode Pump	Temperature Range	Digital Blocks	Analog Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
8-pin (300-mil) DIP	CY8C24123A-24PXI	4 K	256	No	–40 °C to +85 °C	4	6	6	4	2	No
8-pin (150-mil) SOIC	CY8C24123A-24SXI	4 K	256	No	–40 °C to +85 °C	4	6	6	4	2	No
8-pin (150-mil) SOIC (Tape and Reel)	CY8C24123A-24SXIT	4 K	256	No	–40 °C to +85 °C	4	6	6	4	2	No
20-pin (300-mil) DIP	CY8C24223A-24PXI	4 K	256	Yes	–40 °C to +85 °C	4	6	16	8	2	Yes
20-pin (210-mil) SSOP	CY8C24223A-24PVXI	4 K	256	Yes	–40 °C to +85 °C	4	6	16	8	2	Yes
20-pin (210-mil) SSOP (Tape and Reel)	CY8C24223A-24PVXIT	4 K	256	Yes	–40 °C to +85 °C	4	6	16	8	2	Yes
20-pin (300-mil) SOIC	CY8C24223A-24SXI	4 K	256	Yes	–40 °C to +85 °C	4	6	16	8	2	Yes
20-pin (300-mil) SOIC (Tape and Reel)	CY8C24223A-24SXIT	4 K	256	Yes	–40 °C to +85 °C	4	6	16	8	2	Yes
28-pin (300-mil) DIP	CY8C24423A-24PXI	4 K	256	Yes	–40 °C to +85 °C	4	6	24	10	2	Yes
28-pin (210-mil) SSOP	CY8C24423A-24PVXI	4 K	256	Yes	–40 °C to +85 °C	4	6	24	10	2	Yes
28-pin (210-mil) SSOP (Tape and Reel)	CY8C24423A-24PVXIT	4 K	256	Yes	–40 °C to +85 °C	4	6	24	10	2	Yes
28-pin (300-mil) SOIC	CY8C24423A-24SXI	4 K	256	Yes	–40 °C to +85 °C	4	6	24	10	2	Yes
28-pin (300-mil) SOIC (Tape and Reel)	CY8C24423A-24SXIT	4 K	256	Yes	–40 °C to +85 °C	4	6	24	10	2	Yes
32-pin (5 × 5 mm 1.00 max) Sawn QFN	CY8C24423A-24LTXI	4 K	256	Yes	–40 °C to +85 °C	4	6	24	10	2	Yes
32-pin (5 × 5 mm 1.00 max) Sawn QFN (Tape and Reel)	CY8C24423A-24LTXIT	4 K	256	Yes	–40 °C to +85 °C	4	6	24	10	2	Yes
56-pin OCD SSOP	CY8C24000A-24PVXI[43]	4 K	256	Yes	–40 °C to +85 °C	4	6	24	10	2	Yes

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions



Note
43. This part may be used for in-circuit debugging. It is NOT available for production.

Glossary (continued)

shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Document History Page (continued)

Document Title: CY8C24123A/CY8C24223A/CY8C24423A, PSoC® Programmable System-on-Chip Document Number: 38-12028				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*L	2897881	MAXK / NJF	03/23/2010	Add "More Information" on page 2. Update unit in Table 10-28 and Table 38 of SPIS Maximum Input Clock Frequency from ns to MHz. Update revision of package diagrams for 8 PDIP, 8 SOIC, 20 PDIP, 20 SSOP, 20 SOIC, 28 PDIP, 28 SSOP, 28 SOIC, 32 QFN. Updated Cypress website links. Removed reference to PSoC Designer 4.4. Updated 56-Pin SSOP definitions and diagram. Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings. Updated 5-V DC Analog Reference Specifications table. Updated Note in Packaging Information. Added Note 29. Updated Solder Reflow Specifications table. Removed Third Party Tools and Build a PSoC Emulator into your Board. Removed inactive parts from Ordering Information. Update trademark info. and Sales, Solutions, and Legal Information.
*M	2942375	VMAD	06/02/2010	Updated content to match current style guide and datasheet template. No technical updates.
*N	3032514	NJF	09/17/10	Added PSoC Device Characteristics table. Added DC I^2C Specifications table. Added F_{32K_U} max limit. Added Tjit_IMO specification, removed existing jitter specifications. Updated Analog reference tables. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changes were made to AC Digital Block Specifications table and I^2C Timing Diagram. They were updated for clearer understanding. Updated Figure 13 since the labelling for y-axis was incorrect. Template and styles update.
*O	3098766	YJI	12/01/2010	Sunset review; no content update
*P	3351721	YJI	08/31/2011	Full annual review of document. No changes are required.
*Q	3367463	BTK / GIR	09/22/2011	Updated text under DC Analog Reference Specifications on page 28. Removed package diagram spec 51-85188 as there is no active MPN using this outline drawing. The text "Pin must be left floating" is included under Description of NC pin in Table 5 on page 13 and Table 6 on page 14. Updated Table 50 on page 57 to give more clarity. Removed Footnote #35.
*R	3598291	LURE / XZNG	04/24/2012	Changed the PWM description string from "8- to 32-bit" to "8- and 16-bit".
*S	3991993	PMAD	05/08/2013	Updated Packaging Information: spec 51-85066 – Changed revision from *E to *F. spec 51-85014 – Changed revision from *F to *G. spec 51-85026 – Changed revision from *F to *G. spec 001-30999 – Changed revision from *C to *D. spec 51-85062 – Changed revision from *E to *F. Updated Reference Documents (Removed 001-17397 spec, 001-14503 spec related information). Added Errata.

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