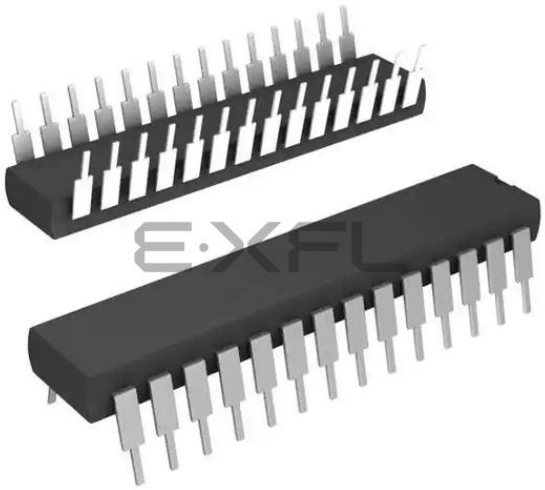

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	A/D 10x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24423a-24pxi

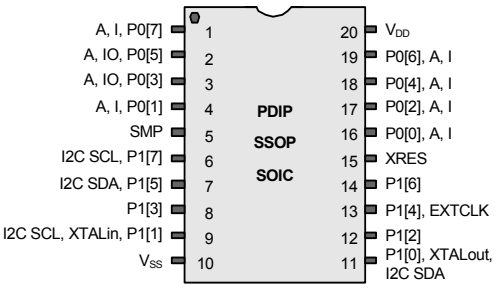
20-Pin Part Pinout

Table 3. 20-Pin PDIP, SSOP, and SOIC

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I/O	P0[5]	Analog column mux input and column output
3	I/O	I/O	P0[3]	Analog column mux input and column output
4	I/O	I	P0[1]	Analog column mux input
5	Power		SMP	SMP connection to external components required
6	I/O		P1[7]	I^2C SCL
7	I/O		P1[5]	I^2C SDA
8	I/O		P1[3]	
9	I/O		P1[1]	XTALin, I^2C SCL, ISSP-SCLK[5]
10	Power		V_{SS}	Ground connection.
11	I/O		P1[0]	XTALout, I^2C SDA, ISSP-SDATA[5]
12	I/O		P1[2]	
13	I/O		P1[4]	Optional external clock input (EXTCLK)
14	I/O		P1[6]	
15	Input		XRES	Active high external reset with internal pull-down
16	I/O	I	P0[0]	Analog column mux input
17	I/O	I	P0[2]	Analog column mux input
18	I/O	I	P0[4]	Analog column mux input
19	I/O	I	P0[6]	Analog column mux input
20	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 5. CY8C24223A 20-Pin PSoC Device



Note
5. These are the ISSP pins, which are not high Z at POR. See the PSoC Technical Reference Manual for details.

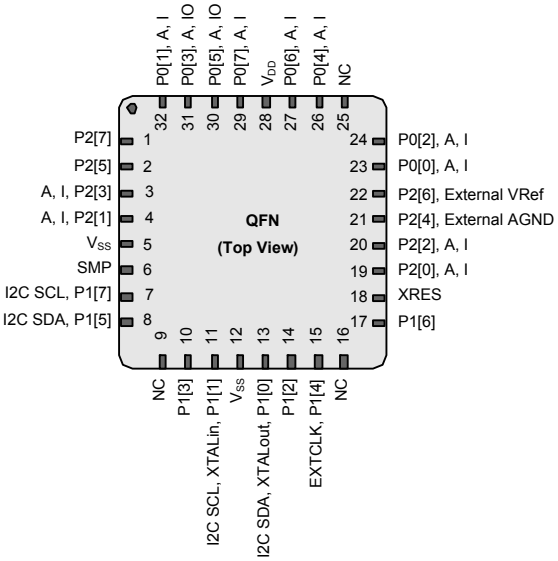
32-Pin Part Pinout

Table 5. 32-Pin QFN[7]

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O		P2[7]	
2	I/O		P2[5]	
3	I/O	I	P2[3]	Direct switched capacitor block input
4	I/O	I	P2[1]	Direct switched capacitor block input
5	Power		V_{SS}	Ground connection
6	Power		SMP	SMP connection to external components required
7	I/O		P1[7]	I^2C SCL
8	I/O		P1[5]	I^2C SDA
9			NC	No connection. Pin must be left floating
10	I/O		P1[3]	
11	I/O		P1[1]	XTALin, I^2C SCL, ISSP-SCLK[8]
12	Power		V_{SS}	Ground Connection
13	I/O		P1[0]	XTALout, I^2C SDA, ISSP-SDATA[8]
14	I/O		P1[2]	
15	I/O		P1[4]	Optional EXTCLK
16			NC	No connection. Pin must be left floating
17	I/O		P1[6]	
18	Input		XRES	Active high external reset with internal pull-down
19	I/O	I	P2[0]	Direct switched capacitor block input
20	I/O	I	P2[2]	Direct switched capacitor block input
21	I/O		P2[4]	External AGND
22	I/O		P2[6]	External V_{REF}
23	I/O	I	P0[0]	Analog column mux input
24	I/O	I	P0[2]	Analog column mux input
25			NC	No connection. Pin must be left floating
26	I/O	I	P0[4]	Analog column mux input
27	I/O	I	P0[6]	Analog column mux input
28	Power		V_{DD}	Supply voltage
29	I/O	I	P0[7]	Analog column mux input
30	I/O	I/O	P0[5]	Analog column mux input and column output
31	I/O	I/O	P0[3]	Analog column mux input and column output
32	I/O	I	P0[1]	Analog column mux input

LEGEND: A = Analog, I = Input, and O = Output.

Figure 7. CY8C24423A 32-Pin PSoC Device



Notes
7. The center pad on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
8. These are the ISSP pins, which are not high Z at POR. See the PSoC Technical Reference Manual for details.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C24x23A PSoC device. For the latest electrical specifications, check if you have the most recent datasheet by visiting the website at http://www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted.

Refer to Table 29 on page 37 for the electrical specifications for the IMO using SLIMO mode.

Figure 9. Voltage versus CPU Frequency

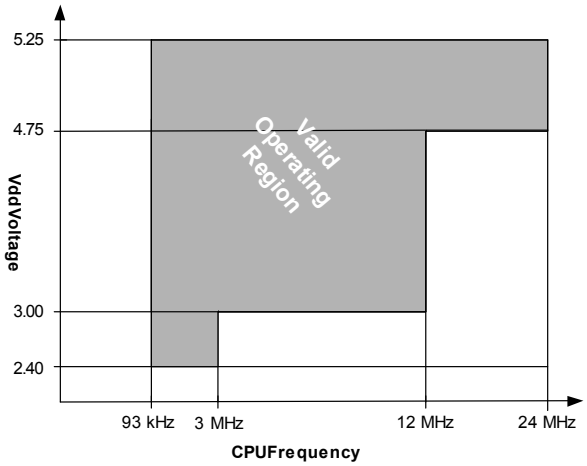
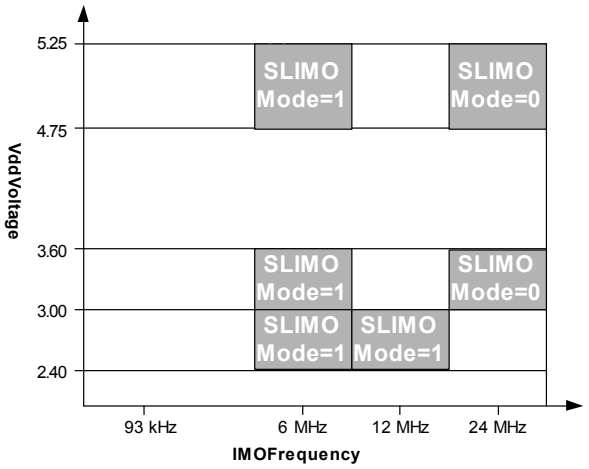


Figure 8. IMO Frequency Trim Options



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 9. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 65 °C degrades reliability.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	
$t_{BAKETIME}$	Bake time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied	–40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tri-state	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
ESD	Electrostatic discharge voltage	2000	–	–	V	Human body model ESD.
LU	Latch up current	–	–	200	mA	

Operating Temperature

Table 10. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_J	Junction temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Table 48 on page 57. You must limit the power consumption to comply with this requirement

DC Electrical Characteristics

DC Chip-Level Specifications

Table 11 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 11. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	2.4	–	5.25	V	See DC POR and LVD specifications, Table 26 on page 35
I_{DD}	Supply current	–	5	8	mA	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off SLIMO mode = 0. IMO = 24 MHz
I_{DD3}	Supply current	–	3.3	6.0	mA	Conditions are V_{DD} = 3.3 V, T_A= 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off. SLIMO mode = 0. IMO = 24 MHz
I_{DD27}	Supply current	–	2	4	mA	Conditions are V_{DD} = 2.7 V, T_A = 25 °C, CPU = 0.75 MHz, SYSCLK doubler disabled, VC1 = 0.375 MHz, VC2 = 23.44 kHz, VC3 = 0.09 kHz, analog power = off. SLIMO mode = 1. IMO = 6 MHz
I_{SB}	Sleep (mode) current with POR, LVD, sleep timer, and WDT.[10]	–	3	6.5	µA	Conditions are with internal slow speed oscillator, V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 55 °C, analog power = off
I_{SBH}	Sleep (mode) current with POR, LVD, sleep timer, and WDT at high temperature.[10]	–	4	25	µA	Conditions are with internal slow speed oscillator, V_{DD} = 3.3 V, 55 °C < T_A ≤ 85 °C, analog power = off
I_{SBXTL}	Sleep (mode) current with POR, LVD, sleep timer, WDT, and external crystal.[10]	–	4	7.5	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 55 °C, analog power = off
I_{SBXTLH}	Sleep (Mode) current with POR, LVD, sleep timer, WDT, and external crystal at high temperature.[10]	–	5	26	µA	Conditions are with properly loaded, 1µW max, 32.768 kHz crystal. V_{DD} = 3.3 V, 55 °C < T_A ≤ 85 °C, analog power = off
V_{REF}	Reference voltage (Bandgap)	1.28	1.30	1.32	V	Trimmed for appropriate V_{DD}. V_{DD} > 3.0 V
V_{REF27}	Reference voltage (Bandgap)	1.16	1.30	1.32	V	Trimmed for appropriate V_{DD}. V_{DD} = 2.4 V to 3.0 V

Note
10. Standby current includes all functions (POR, LVD, WDT, sleep time) needed for reliable system operation. This must be compared with devices that have similar functions enabled.

DC Operational Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

The operational amplifier is a component of both the analog continuous time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the analog continuous time PSoC block. Typical parameters are measured at 5 V at 25 °C and are for design guidance only.

Table 14. 5-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 1.6 1.3 1.2	 10 8 7.5	 mV mV mV	
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	20	–	pA	Gross tested to 1 µA
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range Common mode voltage range (high power or high Opamp bias)	0.0 0.5	– –	V_{DD} V_{DD} – 0.5	V	The common mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 60 60 80	 – – –	 – – –	 dB dB dB	Specification is applicable at high Opamp bias. For low Opamp bias mode, minimum is 60 dB.
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.5	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 0.2 0.2 0.5	 V V V	
I_{SOA}	Supply current (including associated AGND buffer) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – – – –	 150 300 600 1200 2400 4600	 200 400 800 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply voltage rejection ratio	64	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$

Table 16. 2.7-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 1.65 1.32 –	 10 8 –	 mV mV mV	Power = high, Opamp bias = high setting is not allowed for 2.7 V V_{DD} operation.
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	20	–	pA	Gross tested to 1 µA
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0.2	–	V_{DD} – 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain Power = low, Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 60 60 80	 – – –	 – – –	 dB dB dB	Specification is applicable at low Opamp bias. For high Opamp bias mode, (except high power, high Opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.2	 – – –	 – – –	 V V V	Power = high, Opamp bias = high setting is not allowed for 2.7 V V_{DD} operation.
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 – – –	 – – –	 0.2 0.2 0.2	 V V V	Power = high, Opamp bias = high setting is not allowed for 2.7 V V_{DD} operation.
I_{SOA}	Supply current (including associated AGND buffer) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – – – –	 150 300 600 1200 2400 –	 200 400 800 1600 3200 –	 µA µA µA µA µA µA	Power = high, Opamp bias = high setting is not allowed for 2.7 V V_{DD} operation.
$PSRR_{OA}$	Supply voltage rejection ratio	64	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$

DC Low Power Comparator Specifications

Table 17 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V at 25 °C and are for design guidance only.

Table 17. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	V_{DD} – 1	V	
I_{SLPC}	LPC supply current	–	10	40	µA	
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV	

DC Analog Output Buffer Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 18. 5-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (absolute value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	µV/°C	
V_{CMOB}	Common mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 1 1	 – –	 W W	
$V_{OHIGHOB}$	High output voltage swing (Load = 32 ohms to $V_{DD/2}$) Power = low Power = high	 0.5 × V_{DD} + 1.1 0.5 × V_{DD} + 1.1	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 32 ohms to $V_{DD/2}$) Power = low Power = high	 – –	 – –	 .5 × V_{DD} – 1.3 0.5 × V_{DD} – 1.3	 V V	
I_{SOB}	Supply current including Opamp bias cell (No Load) Power = low Power = high	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	52	64	–	dB	V_{OUT} > (V_{DD} – 1.25)

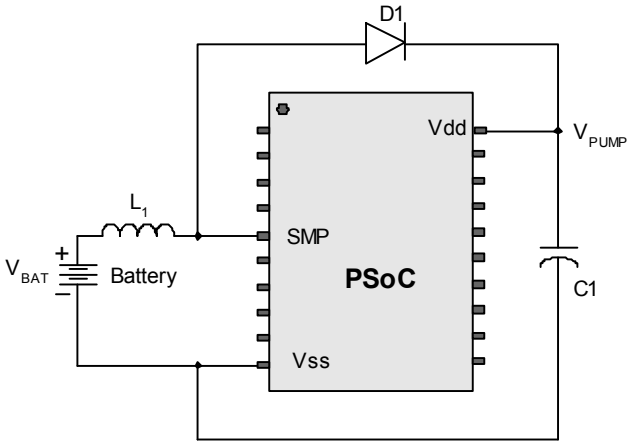
Table 19. 3.3-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (absolute value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	µV/°C	
V_{CMOB}	Common mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (Load = 1 K ohms to $V_{DD/2}$) Power = low Power = high	 0.5 × V_{DD} + 1.0 0.5 × V_{DD} + 1.0	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 1 K ohms to $V_{DD/2}$) Power = low Power = high	 – –	 – –	 0.5 × V_{DD} – 1.0 0.5 × V_{DD} – 1.0	 V V	
I_{SOB}	Supply current including Opamp bias cell (no load) Power = low Power = high	 – –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	52	64	–	dB	V_{OUT} > (V_{DD} – 1.25)

Table 20. 2.7-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (absolute value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	µV/°C	
V_{CMOB}	Common mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (Load = 1 K ohms to $V_{DD/2}$) Power = low Power = high	 0.5 × V_{DD} + 0.2 0.5 × V_{DD} + 0.2	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 1 K ohms to $V_{DD/2}$) Power = low Power = high	 – –	 – –	 0.5 × V_{DD} – 0.7 0.5 × V_{DD} – 0.7	 V V	
I_{SOB}	Supply current including Opamp bias cell (No Load) Power = low Power = high	 –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	52	64	–	dB	V_{OUT} > (V_{DD} – 1.25).

Figure 10. Basic Switch Mode Pump Circuit



DC Analog Reference Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

The guaranteed specifications for RefHI and RefLo are measured through the Analog Continuous Time PSoC blocks. The power levels for RefHi and RefLo refer to the Analog Reference Control register. AGND is measured at P2[4] in AGND bypass mode. Each Analog Continuous Time PSoC block adds a maximum of 10 mV additional offset error to guaranteed AGND specifications from the local AGND buffer. Reference control power can be set to medium or high unless otherwise noted.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the analog reference. Some coupling of the digital signal may appear on the AGND.

Table 22. 5-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.136	$V_{DD}/2$ + 1.288	$V_{DD}/2$ + 1.409	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.138	$V_{DD}/2$ + 0.003	$V_{DD}/2$ + 0.132	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.417	$V_{DD}/2$ – 1.289	$V_{DD}/2$ – 1.154	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.202	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.358	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.055	$V_{DD}/2$ + 0.001	$V_{DD}/2$ + 0.055	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.369	$V_{DD}/2$ – 1.295	$V_{DD}/2$ – 1.218	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.211	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.357	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.055	$V_{DD}/2$	$V_{DD}/2$ + 0.052	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.368	$V_{DD}/2$ – 1.298	$V_{DD}/2$ – 1.224	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.215	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.353	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.040	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.033	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.368	$V_{DD}/2$ – 1.299	$V_{DD}/2$ – 1.225	V
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.076	P2[4] + P2[6] – 0.021	P2[4] + P2[6] + 0.041	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.025	P2[4] – P2[6] + 0.011	P2[4] – P2[6] + 0.085	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.069	P2[4] + P2[6] – 0.014	P2[4] + P2[6] + 0.043	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.029	P2[4] – P2[6] + 0.005	P2[4] – P2[6] + 0.052	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.072	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.048	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.031	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.057	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.070	P2[4] + P2[6] – 0.009	P2[4] + P2[6] + 0.047	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.033	P2[4] – P2[6] + 0.001	P2[4] – P2[6] + 0.039	V

Table 22. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b101	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.228	P2[4] + 1.284	P2[4] + 1.332	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.358	P2[4] – 1.293	P2[4] – 1.226	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.236	P2[4] + 1.289	P2[4] + 1.332	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.357	P2[4] – 1.297	P2[4] – 1.229	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.237	P2[4] + 1.291	P2[4] + 1.337	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.356	P2[4] – 1.299	P2[4] – 1.232	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.237	P2[4] + 1.292	P2[4] + 1.337	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.357	P2[4] – 1.300	P2[4] – 1.233	V
0b110	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.512	2.594	2.654	V
		V_{AGND}	AGND	Bandgap	1.250	1.303	1.346	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.011	V_{SS} + 0.027	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.515	2.592	2.654	V
		V_{AGND}	AGND	Bandgap	1.253	1.301	1.340	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.02	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.518	2.593	2.651	V
		V_{AGND}	AGND	Bandgap	1.254	1.301	1.338	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.017	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.517	2.594	2.650	V
		V_{AGND}	AGND	Bandgap	1.255	1.300	1.337	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.015	V
0b111	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	3.2 × Bandgap	4.011	4.143	4.203	V
		V_{AGND}	AGND	1.6 × Bandgap	2.020	2.075	2.118	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.011	V_{SS} + 0.026	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	3.2 × Bandgap	4.022	4.138	4.203	V
		V_{AGND}	AGND	1.6 × Bandgap	2.023	2.075	2.114	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.017	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	3.2 × Bandgap	4.026	4.141	4.207	V
		V_{AGND}	AGND	1.6 × Bandgap	2.024	2.075	2.114	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.015	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	3.2 × Bandgap	4.030	4.143	4.206	V
		V_{AGND}	AGND	1.6 × Bandgap	2.024	2.076	2.112	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.013	V

DC POR, SMP, and LVD Specifications

Table 24 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the PSoC Programmable Sytem-on-Chip Technical Reference Manual for more information on the VLT_CR register.

Table 26. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip					V_{DD} must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b		2.82	2.95	V	
V_{PPOR2}	PORLEV[1:0] = 10b		4.55	4.70	V	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.40	2.45	2.51[12]	V	
V_{LVD1}	VM[2:0] = 001b	2.85	2.92	2.99[13]	V	
V_{LVD2}	VM[2:0] = 010b	2.95	3.02	3.09	V	
V_{LVD3}	VM[2:0] = 011b	3.06	3.13	3.20	V	
V_{LVD4}	VM[2:0] = 100b	4.37	4.48	4.55	V	
V_{LVD5}	VM[2:0] = 101b	4.50	4.64	4.75	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	
	V_{DD} value for SMP trip					
V_{PUMP0}	VM[2:0] = 000b	2.50	2.55	2.62[14]	V	
V_{PUMP1}	VM[2:0] = 001b	2.96	3.02	3.09	V	
V_{PUMP2}	VM[2:0] = 010b	3.03	3.10	3.16	V	
V_{PUMP3}	VM[2:0] = 011b	3.18	3.25	3.32[15]	V	
V_{PUMP4}	VM[2:0] = 100b	4.54	4.64	4.74	V	
V_{PUMP5}	VM[2:0] = 101b	4.62	4.73	4.83	V	
V_{PUMP6}	VM[2:0] = 110b	4.71	4.82	4.92	V	
V_{PUMP7}	VM[2:0] = 111b	4.89	5.00	5.12	V	

Notes
12. Always greater than 50 mV above V_{PPOR} (PORLEV=00) for falling supply.
13. Always greater than 50 mV above V_{PPOR} (PORLEV=01) for falling supply.
14. Always greater than 50 mV above V_{LVD0}.
15. Always greater than 50 mV above V_{LVD3}.

Table 30. 2.7-V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO12}	IMO frequency for 12 MHz	11.5	12	12.7[27, 28]	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 8 on page 18. SLIMO mode = 1.
F_{IMO6}	IMO frequency for 6 MHz	5.5	6	6.5[27, 28]	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 8 on page 18. SLIMO mode = 1.
F_{CPU1}	CPU frequency (2.7 V nominal)	0.937	3	3.15[27]	MHz	SLIMO mode = 0.
F_{BLK27}	Digital PSoC block frequency (2.7 V nominal)	0	12	12.7[27, 28]	MHz	Refer to the AC Digital Block Specifications.
F_{32K1}	ILO frequency	8	32	96	kHz	
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on timing this
t_{XRST}	External reset pulse width	10	–	–	µs	
DC12M	12 MHz duty cycle	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.7	MHz	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power-up.
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the System Resets section of the PSoC Technical Reference Manual.
t_{jit_IMO}[29]	12 MHz IMO cycle-to-cycle jitter (RMS)	–	400	1000	ps	N = 32
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	600	1300	ps	
	12 MHz IMO period jitter (RMS)	–	100	500	ps	
t_{jit_PLL}[29]	12 MHz IMO cycle-to-cycle jitter (RMS)	–	400	1000	ps	N = 32
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	700	1300		
	12 MHz IMO period jitter (RMS)	–	300	500		

Notes
27. 2.4 V < V_{DD} < 3.0 V.
28. Refer to application note Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 for information on trimming for operation at 3.3 V.
29. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

AC Analog Output Buffer Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 39. 5-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
t_{ROB}	Rising settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high	 – –	 – –	 2.5 2.5	 µs µs
t_{SOB}	Falling settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high	 – –	 – –	 2.2 2.2	 µs µs
SR_{ROB}	Rising slew rate (20% to 80%), 1 V Step, 100 pF load Power = low Power = high	 0.65 0.65	 – –	 – –	 V/µs V/µs
SR_{FOB}	Falling slew rate (80% to 20%), 1 V Step, 100 pF load Power = low Power = high	 0.65 0.65	 – –	 – –	 V/µs V/µs
BW_{OB}	Small signal bandwidth, 20mV_{pp}, 3dB BW, 100 pF load Power = low Power = high	 0.8 0.8	 – –	 – –	 MHz MHz
BW_{OB}	Large signal bandwidth, 1V_{pp}, 3dB BW, 100 pF load Power = low Power = high	 300 300	 – –	 – –	 kHz kHz

Table 40. 3.3-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
t_{ROB}	Rising settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high	 – –	 – –	 3.8 3.8	 µs µs
t_{SOB}	Falling settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high	 – –	 – –	 2.6 2.6	 µs µs
SR_{ROB}	Rising slew rate (20% to 80%), 1 V Step, 100 pF load Power = low Power = high	 0.5 0.5	 – –	 – –	 V/µs V/µs
SR_{FOB}	Falling slew rate (80% to 20%), 1 V Step, 100 pF load Power = low Power = high	 0.5 0.5	 – –	 – –	 V/µs V/µs
BW_{OB}	Small signal bandwidth, 20mV_{pp}, 3dB BW, 100 pF load Power = low Power = high	 0.7 0.7	 – –	 – –	 MHz MHz
BW_{OB}	Large signal bandwidth, 1V_{pp}, 3dB BW, 100 pF load Power = low Power = high	 200 200	 – –	 – –	 kHz kHz

Table 41. 2.7-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
t_{ROB}	Rising settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high	 – –	 – –	 4 4	 µs µs
t_{SOB}	Falling settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high	 – –	 – –	 3 3	 µs µs
SR_{ROB}	Rising slew rate (20% to 80%), 1 V Step, 100 pF load Power = low Power = high	 0.4 0.4	 – –	 – –	 V/µs V/µs
SR_{FOB}	Falling slew rate (80% to 20%), 1 V Step, 100 pF load Power = low Power = high	 0.4 0.4	 – –	 – –	 V/µs V/µs
BW_{OB}	Small signal bandwidth, 20 mV_{pp}, 3dB BW, 100 pF load Power = low Power = high	 0.6 0.6	 – –	 – –	 MHz MHz
BW_{OB}	Large signal bandwidth, 1 V_{pp}, 3dB BW, 100 pF load Power = low Power = high	 180 180	 – –	 – –	 kHz kHz

AC External Clock Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 42. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz
–	High period	20.6	–	5300	ns
–	Low period	20.6	–	–	ns
–	Power-up IMO to switch	150	–	–	µs

Table 43. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency with CPU clock divide by 1[32]	0.093	–	12.3	MHz
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater[33]	0.186	–	24.6	MHz
–	High period with CPU clock divide by 1	41.7	–	5300	ns
–	Low period with CPU clock divide by 1	41.7	–	–	ns
–	Power-up IMO to switch	150	–	–	µs

Notes
32. Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
33. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met

Table 44. 2.7-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1[34]	0.093	–	12.3	MHz	
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater[35]	0.186	–	12.3	MHz	
–	High period with CPU clock divide by 1	41.7	–	5300	ns	
–	Low period with CPU clock divide by 1	41.7	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

AC Programming Specifications

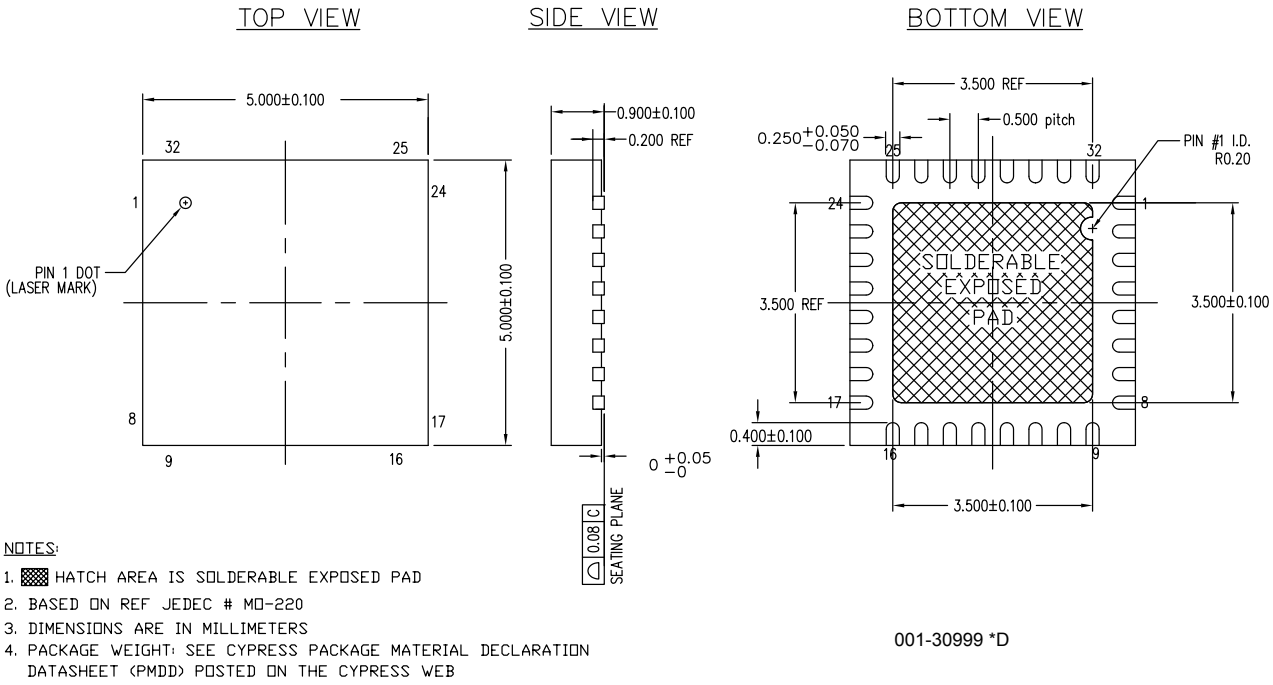
Table 45 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 45. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RSCLK}	Rise time of SCLK	1	–	20	ns	
t_{FSCLK}	Fall time of SCLK	1	–	20	ns	
t_{SSCLK}	Data setup time to falling edge of SCLK	40	–	–	ns	
t_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
t_{ERASEB}	Flash erase time (block)	–	20	–	ms	
t_{WRITE}	Flash block write time	–	80	–	ms	
t_{DSCLK}	Data out delay from falling edge of SCLK	–	–	45	ns	$V_{DD} > 3.6$
t_{DSCLK3}	Data out delay from falling edge of SCLK	–	–	50	ns	$3.0 \le V_{DD} \le 3.6$
t_{DSCLK2}	Data out delay from falling edge of SCLK	–	–	70	ns	$2.4 \le V_{DD} \le 3.0$
$t_{ERASEALL}$	Flash erase time (Bulk)	–	20	–	ms	Erase all blocks and protection fields at once
$t_{PROGRAM\_HOT}$	Flash block erase + flash block write time	–	–	200[36]	ms	0 °C ≤ Tj ≤ 100 °C
$t_{PROGRAM\_COLD}$	Flash block erase + flash block write time	–	–	400[36]	ms	–40 °C ≤ Tj ≤ 0 °C

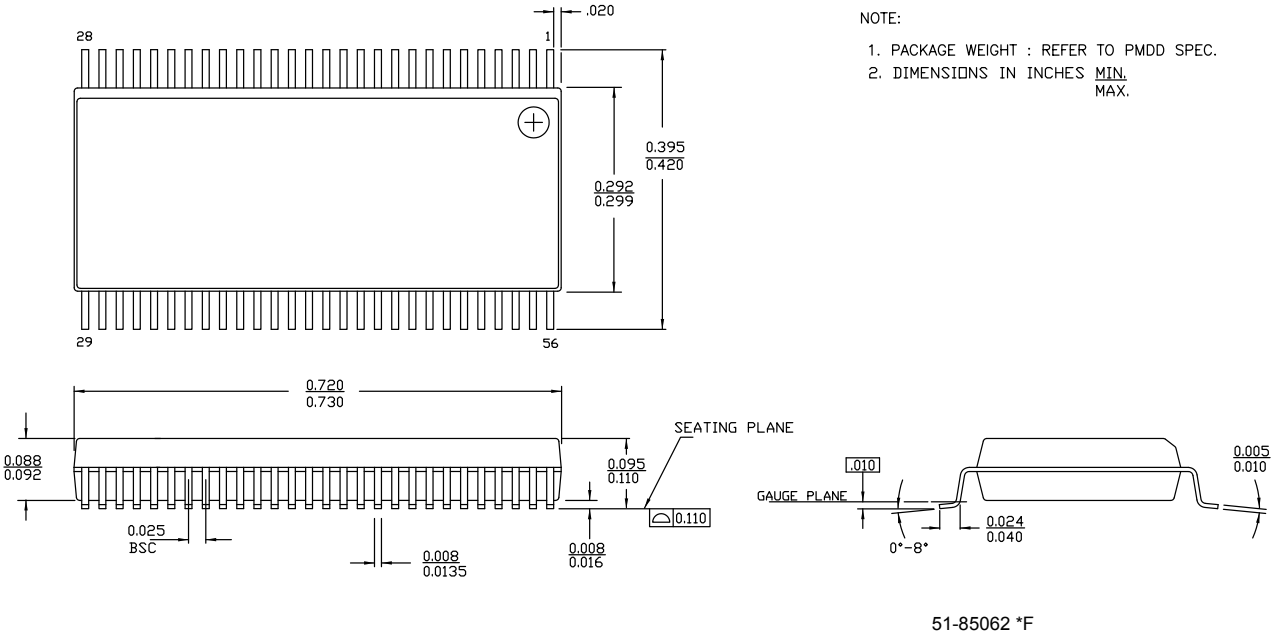
Notes
34. Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
35. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
36. For the full industrial range, you must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs application note Design Aids – Reading and Writing PSoC® Flash – AN2015 for more information.

Figure 25. 32-Pin Sawn QFN Package



Important Note For information on the preferred dimensions for mounting QFN packages, see the application note, *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages* available at http://www.amkor.com.

Figure 26. 56-Pin (300-Mil) SSOP



Thermal Impedances

Table 48. Thermal Impedances per Package

Package	Typical θ_{JA}[38]
8-pin PDIP	123 °C/W
8-pin SOIC	185 °C/W
20-pin PDIP	109 °C/W
20-pin SSOP	117 °C/W
20-pin SOIC	81 °C/W
28-pin PDIP	69 °C/W
28-pin SSOP	101 °C/W
28-pin SOIC	74 °C/W
32-pin QFN[39]	22 °C/W

Capacitance on Crystal Pins

Table 49. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
8-pin PDIP	2.8 pF
8-pin SOIC	2.0 pF
20-pin PDIP	3.0 pF
20-pin SSOP	2.6 pF
20-pin SOIC	2.5 pF
28-pin PDIP	3.5 pF
28-pin SSOP	2.8 pF
28-pin SOIC	2.7 pF
32-pin QFN	2.0 pF

Solder Reflow Specifications

Table 50 shows the solder reflow temperature limits that must not be exceeded.

Table 50. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
8-pin PDIP	260 °C	30 seconds
8-pin SOIC	260 °C	30 seconds
20-pin PDIP	260 °C	30 seconds
20-pin SSOP	260 °C	30 seconds
20-pin SOIC	260 °C	30 seconds
28-pin PDIP	260 °C	30 seconds
28-pin SSOP	260 °C	30 seconds
28-pin SOIC	260 °C	30 seconds
32-pin QFN	260 °C	30 seconds

Notes
38. $T_J = T_A + \text{Power} \times \theta_{JA}$
39. To achieve the thermal impedance specified for the QFN package, refer to *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages* available at www.amkor.com.

Errata

This section describes the errata for the CY8C24xxxA device family. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Ordering Information
CY8C24123A	CY8C24123A-24PXI
	CY8C24123A-24SXI
	CY8C24123A-24SXIT
	CY8C24223A-24PXI
	CY8C24223A-24PVXI
	CY8C24223A-24PVXIT
	CY8C24223A-24SXI
	CY8C24223A-24SXIT
	CY8C24423A-24PXI
	CY8C24423A-24PVXI
	CY8C24423A-24PVXIT
	CY8C24423A-24SXI
	CY8C24423A-24SXIT
	CY8C24423A-24LFXI
	CY8C24423A-24LTXI
	CY8C24423A-24LTXIT
	CY8C24000A-24PVXI

CY8C24123A Qualification Status

Product Status: Production

CY8C24123A Errata Summary

The following table defines the errata applicability to available CY8C24123A family devices.

Items	Part Number	Silicon Revision	Fix Status
[1.]. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes	CY8C24123A	*A	No silicon fix planned. Workaround is required.

1. **Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes**
   - **Problem Definition**
     Asynchronous Digital Communications Interfaces may fail framing beyond 0 to 70 °C. This problem does not affect end-product usage between 0 and 70 °C.
   - **Parameters Affected**
     The IMO frequency tolerance. The worst case deviation when operated below 0°C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.
   - **Trigger Condition(S)**
     The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the data sheet limit of ±2.5% when operated beyond the temperature range of 0 to +70 °C.
   - **Scope of Impact**
     This problem may affect UART, IrDA, and FSK implementations.
   - **Workaround**
     Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.
   - **Fix Status**
     Silicon fix is not planned. The workaround mentioned above should be used.

Document History Page

Document Title: CY8C24123A/CY8C24223A/CY8C24423A, PSoC® Programmable System-on-Chip Document Number: 38-12028				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	236409	SFV	See ECN	New silicon and new document – Preliminary datasheet.
*A	247589	SFV	See ECN	Changed the title to read “Final” datasheet. Updated Electrical Specifications chapter.
*B	261711	HMT	See ECN	Input all SFV memo changes. Updated Electrical Specifications chapter.
*C	279731	HMT	See ECN	Update Electrical Specifications chapter, including 2.7 VIL DC GPIO spec. Add Solder Reflow Peak Temperature table. Clean up pinouts and fine tune wording and format throughout.
*D	352614	HMT	See ECN	Add new color and CY logo. Add URL to preferred dimensions for mounting MLF packages. Update Transmitter and Receiver AC Digital Block Electrical Specifications. Re-add ISSP pinout identifier. Delete Electrical Specification sentence re: devices running at greater than 12 MHz. Update Solder Reflow Peak Temperature table. Fix CY.com URLs. Update CY copyright.
*E	424036	HMT	See ECN	Fix SMP 8-pin SOIC error in Feature and Order table. Update 32-pin QFN E-Pad dimensions and rev. *A. Add ISSP note to pinout tables. Update typical and recommended Storage Temperature per industrial specs. Add OCD non-production pinout and package diagram. Update CY branding and QFN convention. Update package diagram revisions.
*F	521439	HMT	See ECN	Add Low Power Comparator (LPC) AC/DC electrical spec. tables. Add new Dev. Tool section. Add CY8C20x34 to PSoC Device Characteristics table.
*G	2256806	UVS / PYRS	See ECN	Added Sawn pin information.
*H	2425586	DSO / AESA	See ECN	Corrected Ordering Information to include CY8C24423A-24LTXI and CY8C24423A-24LTXIT
*I	2619935	OGNE / AESA	12/11/2008	Changed title to “CY8C24123A, CY8C24223A, CY8C24423A PSoC® Programmable System-on-Chip™” Updated package diagram 001-30999 to *A. Added note on digital signaling in DC Analog Reference Specifications on page 28. Added Die Sales information note to Ordering Information on page 60.
*J	2692871	DPT / PYRS	04/16/2009	Updated Max package thickness for 32-pin QFN package Formatted Notes Updated “Getting Started” on page 7 Updated “Development Tools” on page 8 and “Designing with PSoC Designer” on page 9
*K	2762168	JVY / AESA	06/25/2009	Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: Modified FIMO6 and TWRITE specifications. Replaced T_{RAMP} (time) specification with SR_{POWER_UP} (slew rate) specification. Added note [9] to Flash Endurance specification. Added IOH, IOL, DC_{ILO}, F_{32K_U}, $T_{POWERUP}$, $T_{ERASEALL}$, $T_{PROGRAM\_HOT}$, and $T_{PROGRAM\_COLD}$ specifications.