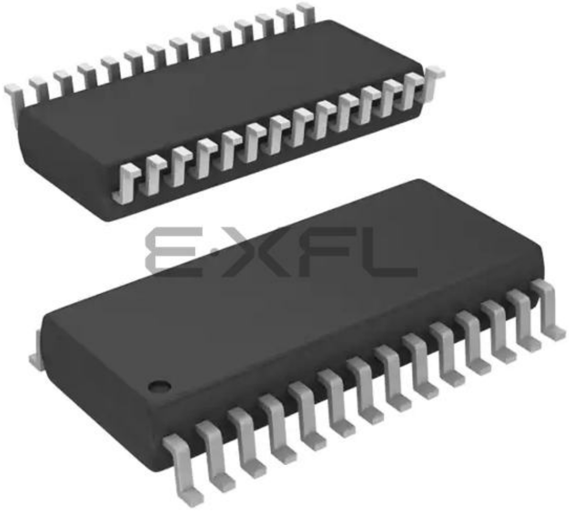
Infineon Technologies - CY8C24423A-24SXI Datasheet



What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	A/D 10x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24423a-24sxi

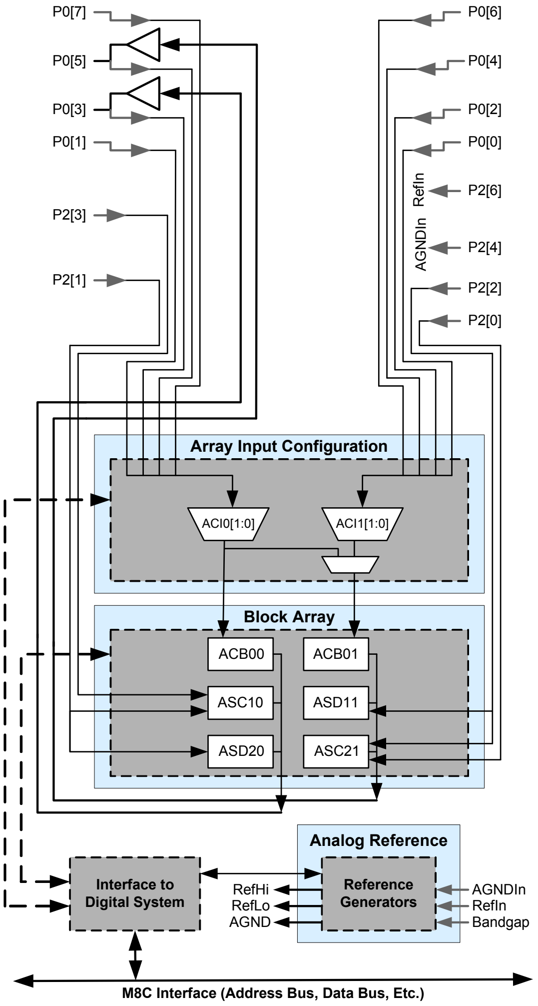
Analog System

The analog system consists of six configurable blocks, each consisting of an opamp circuit that allows the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- ADCs (up to two, with 6- to 14-bit resolution, selectable as incremental, delta sigma, and SAR)
- Filters (two and four pole band-pass, low-pass, and notch)
- Amplifiers (up to two, with selectable gain to 48x)
- Instrumentation amplifiers (one with selectable gain to 93x)
- Comparators (up to two, with 16 selectable thresholds)
- DACs (up to two, with 6 to 9-bit resolution)
- Multiplying DACs (up to two, with 6 to 9-bit resolution)
- High current output drivers (two with 30 mA drive as a PSoC Core resource)
- 1.3 V reference (as a system resource)
- DTMF dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are arranged in a column of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks, as shown in Figure 3

Figure 3. Analog System Block Diagram



Getting Started

For in depth information, along with detailed programming details, see the PSoC® Technical Reference Manual.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable knowledge base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

6. Select user modules.
7. Configure user modules.
8. Organize and connect.
9. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Pinouts

This section describes, lists, and illustrates the CY8C24x23A PSoC device pins and pinout configurations. Every port pin (labeled with a "P") is capable of digital I/O. However, V_{SS}, V_{DD}, SMP, and XRES are not capable of digital I/O.

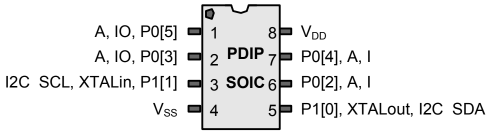
8-Pin Part Pinout

Table 2. 8-Pin PDIP and SOIC

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I/O	P0[5]	Analog column mux input and column output
2	I/O	I/O	P0[3]	Analog column mux input and column output
3	I/O		P1[1]	Crystal input (XTALin), I^2C serial clock (SCL), ISSP-SCLK[4]
4	Power		V_{SS}	Ground connection
5	I/O		P1[0]	Crystal output (XTALout), I^2C serial data (SDA), ISSP-SDATA[4]
6	I/O	I	P0[2]	Analog column mux input
7	I/O	I	P0[4]	Analog column mux input
8	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 4. CY8C24123A 8-Pin PSoC Device



Note

[4] These are the ISSP pins, which are not high Z at POR. See the PSoC Technical Reference Manual for details.

Register Reference

This section lists the registers of the CY8C24x23A PSoC device. For detailed register information, see the PSoC Programmable Sytem-on-Chip Reference Manual.

Register Conventions

Abbreviations Used

The register conventions specific to this section are listed in the following table.

Table 7. Abbreviations

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, Bank 0 and Bank 1. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set, the user is in Bank 1.

Note In the following register mapping tables, blank fields are reserved and must not be accessed.

Table 15. 3.3-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 1.65 1.32 –	 10 8 –	 mV mV mV	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	μV/°C	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	20	–	pA	Gross tested to 1 μA
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0.2	–	V_{DD} – 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain Power = low, ppamp Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 60 60 80	 – – –	 – – –	 dB dB dB	Specification is applicable at low Opamp bias. For high Opamp bias mode (except high power, high Opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.2	 – – –	 – – –	 V V V	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, ppamp Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 – – –	 – – –	 0.2 0.2 0.2	 V V V	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
I_{SOA}	Supply current (including associated AGND buffer) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – – – –	 150 300 600 1200 2400 –	 200 400 800 1600 3200 –	 μA μA μA μA μA μA	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
$PSRR_{OA}$	Supply voltage rejection ratio	64	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} - 2.25)$ or $(V_{DD} - 1.25\ V) \le V_{IN} \le V_{DD}$

DC Analog Output Buffer Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 18. 5-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (absolute value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	µV/°C	
V_{CMOB}	Common mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 1 1	 – –	 W W	
$V_{OHIGHOB}$	High output voltage swing (Load = 32 ohms to $V_{DD/2}$) Power = low Power = high	 0.5 × V_{DD} + 1.1 0.5 × V_{DD} + 1.1	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 32 ohms to $V_{DD/2}$) Power = low Power = high	 – –	 – –	 .5 × V_{DD} – 1.3 0.5 × V_{DD} – 1.3	 V V	
I_{SOB}	Supply current including Opamp bias cell (No Load) Power = low Power = high	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	52	64	–	dB	V_{OUT} > (V_{DD} – 1.25)

Table 19. 3.3-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (absolute value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	µV/°C	
V_{CMOB}	Common mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (Load = 1 K ohms to $V_{DD/2}$) Power = low Power = high	 0.5 × V_{DD} + 1.0 0.5 × V_{DD} + 1.0	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 1 K ohms to $V_{DD/2}$) Power = low Power = high	 – –	 – –	 0.5 × V_{DD} – 1.0 0.5 × V_{DD} – 1.0	 V V	
I_{SOB}	Supply current including Opamp bias cell (no load) Power = low Power = high	 – –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	52	64	–	dB	V_{OUT} > (V_{DD} – 1.25)

DC Switch Mode Pump Specifications

Table 21 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 21. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PUMP} 5 V	5 V output voltage from pump	4.75	5.0	5.25	V	Configuration listed in footnote.[11] Average, neglecting ripple. SMP trip voltage is set to 5.0 V.
V_{PUMP} 3 V	3.3 V output voltage from pump	3.00	3.25	3.60	V	Configuration listed in footnote.[11] Average, neglecting ripple. SMP trip voltage is set to 3.25 V.
V_{PUMP} 2 V	2.6 V output voltage from pump	2.45	2.55	2.80	V	Configuration listed in footnote.[11] Average, neglecting ripple. SMP trip voltage is set to 2.55 V.
I_{PUMP}	Available output current V_{BAT} = 1.8 V, V_{PUMP} = 5.0 V V_{BAT} = 1.5 V, V_{PUMP} = 3.25 V V_{BAT} = 1.3 V, V_{PUMP} = 2.55 V	 5 8 8	 – – –	 – – –	 mA mA mA	Configuration listed in footnote.[11] SMP trip voltage is set to 5.0 V. SMP trip voltage is set to 3.25 V. SMP trip voltage is set to 2.55 V.
V_{BAT}5 V	Input voltage range from battery	1.8	–	5.0	V	Configuration listed in footnote.[11] SMP trip voltage is set to 5.0 V.
V_{BAT}3 V	Input voltage range from battery	1.0	–	3.3	V	Configuration listed in footnote.[11] SMP trip voltage is set to 3.25 V.
V_{BAT}2 V	Input voltage range from battery	1.0	–	3.0	V	Configuration listed in footnote.[11] SMP trip voltage is set to 2.55 V.
$V_{BATSTART}$	Minimum input voltage from battery to start pump	1.2	–	–	V	Configuration listed in footnote.[11] 0 °C ≤ T_A ≤ 100. 1.25 V at T_A = –40 °C
ΔV_{PUMP_Line}	Line regulation (over V_{BAT} range)	–	5	–	%V_O	Configuration listed in footnote.[11] V_O is the V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 26 on page 35.
ΔV_{PUMP_Load}	Load regulation	–	5	–	%V_O	Configuration listed in footnote.[11] V_O is the "V_{DD} value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 26 on page 35.
ΔV_{PUMP_Ripple}	Output voltage ripple (depends on capacitor/load)	–	100	–	mVpp	Configuration listed in footnote.[11] Load is 5 mA.
E_3	Efficiency	35	50	–	%	Configuration listed in footnote.[11] Load is 5 mA. SMP trip voltage is set to 3.25 V.
E_2	Efficiency	–	–	–		
F_{PUMP}	Switching frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching duty cycle	–	50	–	%	

Note

[11] L_1 = 2 mH inductor, C_1 = 10 mF capacitor, D_1 = Schottky diode. See Figure 10

Table 22. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b010	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.121	V_{DD} – 0.003	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.040	V_{DD}/2	V_{DD}/2 + 0.034	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.019	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.083	V_{DD} – 0.002	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.040	V_{DD}/2 – 0.001	V_{DD}/2 + 0.033	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.016	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.075	V_{DD} – 0.002	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.040	V_{DD}/2 – 0.001	V_{DD}/2 + 0.032	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.015	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.074	V_{DD} – 0.002	V_{DD}	V
		V_{AGND}	AGND	V_{DD}/2	V_{DD}/2 – 0.040	V_{DD}/2 – 0.001	V_{DD}/2 + 0.032	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.014	V
0b011	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	3 × Bandgap	3.753	3.874	3.979	V
		V_{AGND}	AGND	2 × Bandgap	2.511	2.590	2.657	V
		V_{REFLO}	Ref Low	Bandgap	1.243	1.297	1.333	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	3 × Bandgap	3.767	3.881	3.974	V
		V_{AGND}	AGND	2 × Bandgap	2.518	2.592	2.652	V
		V_{REFLO}	Ref Low	Bandgap	1.241	1.295	1.330	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	3 × Bandgap	2.771	3.885	3.979	V
		V_{AGND}	AGND	2 × Bandgap	2.521	2.593	2.649	V
		V_{REFLO}	Ref Low	Bandgap	1.240	1.295	1.331	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	3 × Bandgap	3.771	3.887	3.977	V
		V_{AGND}	AGND	2 × Bandgap	2.522	2.594	2.648	V
		V_{REFLO}	Ref Low	Bandgap	1.239	1.295	1.332	V
0b100	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.481 + P2[6]	2.569 + P2[6]	2.639 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.511	2.590	2.658	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.515 – P2[6]	2.602 – P2[6]	2.654 – P2[6]	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.498 + P2[6]	2.579 + P2[6]	2.642 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.518	2.592	2.652	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.513 – P2[6]	2.598 – P2[6]	2.650 – P2[6]	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.504 + P2[6]	2.583 + P2[6]	2.646 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.521	2.592	2.650	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.513 – P2[6]	2.596 – P2[6]	2.649 – P2[6]	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.505 + P2[6]	2.586 + P2[6]	2.648 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.521	2.594	2.648	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.513 – P2[6]	2.595 – P2[6]	2.648 – P2[6]	V

Table 23. 3.3-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2 + 1.170$	$V_{DD}/2 + 1.288$	$V_{DD}/2 + 1.376$	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.098$	$V_{DD}/2 + 0.003$	$V_{DD}/2 + 0.097$	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2 – 1.386$	$V_{DD}/2 – 1.287$	$V_{DD}/2 – 1.169$	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2 + 1.210$	$V_{DD}/2 + 1.290$	$V_{DD}/2 + 1.355$	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.055$	$V_{DD}/2 + 0.001$	$V_{DD}/2 + 0.054$	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2 – 1.359$	$V_{DD}/2 – 1.292$	$V_{DD}/2 – 1.214$	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2 + 1.198$	$V_{DD}/2 + 1.292$	$V_{DD}/2 + 1.368$	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.041$	$V_{DD}/2$	$V_{DD}/2 + 0.04$	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2 – 1.362$	$V_{DD}/2 – 1.295$	$V_{DD}/2 – 1.220$	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2 + 1.202$	$V_{DD}/2 + 1.292$	$V_{DD}/2 + 1.364$	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.033$	$V_{DD}/2$	$V_{DD}/2 + 0.030$	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2 – 1.364$	$V_{DD}/2 – 1.297$	$V_{DD}/2 – 1.222$	V
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.072	P2[4] + P2[6] – 0.017	P2[4] + P2[6] + 0.041	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.029	P2[4] – P2[6] + 0.010	P2[4] – P2[6] + 0.048	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.066	P2[4] + P2[6] – 0.010	P2[4] + P2[6] + 0.043	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.024	P2[4] – P2[6] + 0.004	P2[4] – P2[6] + 0.034	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.007	P2[4] + P2[6] + 0.053	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.028	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.033	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.006	P2[4] + P2[6] + 0.056	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.030	P2[4] – P2[6]	P2[4] – P2[6] + 0.032	V
0b010	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	$V_{DD} – 0.102$	$V_{DD} – 0.003$	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.040$	$V_{DD}/2 + 0.001$	$V_{DD}/2 + 0.039$	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	$V_{SS} + 0.005$	$V_{SS} + 0.020$	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	$V_{DD} – 0.082$	$V_{DD} – 0.002$	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.031$	$V_{DD}/2$	$V_{DD}/2 + 0.028$	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	$V_{SS} + 0.003$	$V_{SS} + 0.015$	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	$V_{DD} – 0.083$	$V_{DD} – 0.002$	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.032$	$V_{DD}/2 – 0.001$	$V_{DD}/2 + 0.029$	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	$V_{SS} + 0.002$	$V_{SS} + 0.014$	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	$V_{DD} – 0.081$	$V_{DD} – 0.002$	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.033$	$V_{DD}/2 – 0.001$	$V_{DD}/2 + 0.029$	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	$V_{SS} + 0.002$	$V_{SS} + 0.013$	V
0b011	All power settings Not allowed at 3.3 V	–	–	–	–	–	–	–

Table 29. 5-V and 3.3-V AC Chip-Level Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
DC24M	24 MHz duty cycle	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
Step24M	24 MHz trim step size	–	50	–	kHz	
Fout48M	48 MHz output frequency	46.8	48.0	49.2[24, 25]	MHz	Trimmed. Using factory trim values.
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power-up.
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the System Resets section of the PSoC Technical Reference Manual.
t_{jit_IMO} [26]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	700	ps	N = 32
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	900	ps	
	24 MHz IMO period jitter (RMS)	–	100	400	ps	
t_{jit_PLL} [26]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	800	ps	N = 32
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	1200		
	24 MHz IMO period jitter (RMS)	–	100	700		

Notes

24. 4.75 V < V_{DD} < 5.25 V.
25. 3.0 V < V_{DD} < 3.6 V. See application note Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 for information on trimming for operation at 3.3 V.
26. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

Table 38. 2.7-V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All Functions	Block input clock frequency	–	–	12.7	MHz	2.4 V < V_{DD} < 3.0 V
Timer	Capture pulse width	100[31]	–	–	ns	
	Input clock frequency, with or without capture	–	–	12.7	MHz	
Counter	Enable Input Pulse Width	100[31]	–	–	ns	
	Input clock frequency, no enable input	–	–	12.7	MHz	
	Input clock frequency, enable input	–	–	12.7	MHz	
Dead Band	Kill pulse width:					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	100[31]	–	–	ns	
	Disable mode	100[31]	–	–	ns	
	Input clock frequency	–	–	12.7	MHz	
CRCPRS (PRS Mode)	Input clock frequency	–	–	12.7	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	12.7	MHz	
SPIM	Input clock frequency	–	–	6.35	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock frequency	–	–	4.23	MHz	
	Width of SS_ Negated between transmissions	100[31]	–	–	ns	
Transmitter	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.
Receiver	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.

Note

[31] 50 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

AC Analog Output Buffer Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 39. 5-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
t_{ROB}	Rising settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high	 – –	 – –	 2.5 2.5	 µs µs
t_{SOB}	Falling settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high	 – –	 – –	 2.2 2.2	 µs µs
SR_{ROB}	Rising slew rate (20% to 80%), 1 V Step, 100 pF load Power = low Power = high	 0.65 0.65	 – –	 – –	 V/µs V/µs
SR_{FOB}	Falling slew rate (80% to 20%), 1 V Step, 100 pF load Power = low Power = high	 0.65 0.65	 – –	 – –	 V/µs V/µs
BW_{OB}	Small signal bandwidth, 20mV$_{pp}$, 3dB BW, 100 pF load Power = low Power = high	 0.8 0.8	 – –	 – –	 MHz MHz
BW_{OB}	Large signal bandwidth, 1V$_{pp}$, 3dB BW, 100 pF load Power = low Power = high	 300 300	 – –	 – –	 kHz kHz

Table 40. 3.3-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
t_{ROB}	Rising settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high	 – –	 – –	 3.8 3.8	 µs µs
t_{SOB}	Falling settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high	 – –	 – –	 2.6 2.6	 µs µs
SR_{ROB}	Rising slew rate (20% to 80%), 1 V Step, 100 pF load Power = low Power = high	 0.5 0.5	 – –	 – –	 V/µs V/µs
SR_{FOB}	Falling slew rate (80% to 20%), 1 V Step, 100 pF load Power = low Power = high	 0.5 0.5	 – –	 – –	 V/µs V/µs
BW_{OB}	Small signal bandwidth, 20mV$_{pp}$, 3dB BW, 100 pF load Power = low Power = high	 0.7 0.7	 – –	 – –	 MHz MHz
BW_{OB}	Large signal bandwidth, 1V$_{pp}$, 3dB BW, 100 pF load Power = low Power = high	 200 200	 – –	 – –	 kHz kHz

Table 41. 2.7-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
t_{ROB}	Rising settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high	 – –	 – –	 4 4	 µs µs
t_{SOB}	Falling settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high	 – –	 – –	 3 3	 µs µs
SR_{ROB}	Rising slew rate (20% to 80%), 1 V Step, 100 pF load Power = low Power = high	 0.4 0.4	 – –	 – –	 V/µs V/µs
SR_{FOB}	Falling slew rate (80% to 20%), 1 V Step, 100 pF load Power = low Power = high	 0.4 0.4	 – –	 – –	 V/µs V/µs
BW_{OB}	Small signal bandwidth, 20 mV_{pp}, 3dB BW, 100 pF load Power = low Power = high	 0.6 0.6	 – –	 – –	 MHz MHz
BW_{OB}	Large signal bandwidth, 1 V_{pp}, 3dB BW, 100 pF load Power = low Power = high	 180 180	 – –	 – –	 kHz kHz

AC External Clock Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C $\le T_A \le$ 85 °C, 3.0 V to 3.6 V and –40 °C $\le T_A \le$ 85 °C, or 2.4 V to 3.0 V and –40 °C $\le T_A \le$ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 42. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz
–	High period	20.6	–	5300	ns
–	Low period	20.6	–	–	ns
–	Power-up IMO to switch	150	–	–	µs

Table 43. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency with CPU clock divide by 1[32]	0.093	–	12.3	MHz
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater[33]	0.186	–	24.6	MHz
–	High period with CPU clock divide by 1	41.7	–	5300	ns
–	Low period with CPU clock divide by 1	41.7	–	–	ns
–	Power-up IMO to switch	150	–	–	µs

Notes

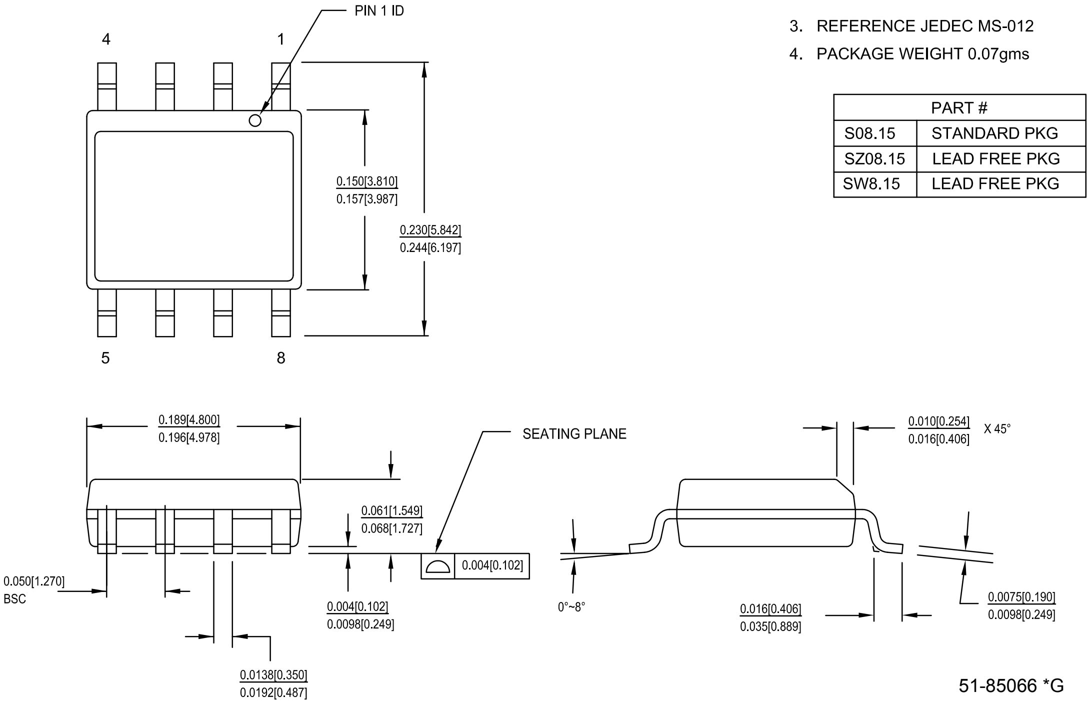
[32] Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.

[33] If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met

Figure 18. 8-Pin (150-Mil) SOIC

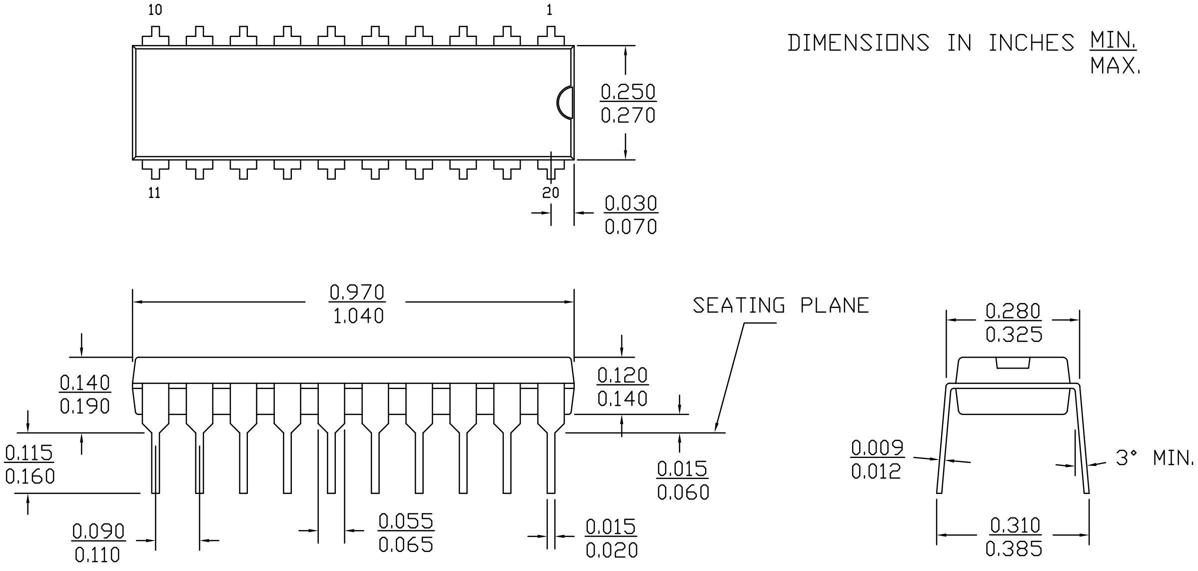
1. DIMENSIONS IN INCHES[MM] MIN. / MAX.
2. PIN 1 ID IS OPTIONAL, ROUND ON SINGLE LEADFRAME RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG
SZ08.15	LEAD FREE PKG
SW8.15	LEAD FREE PKG



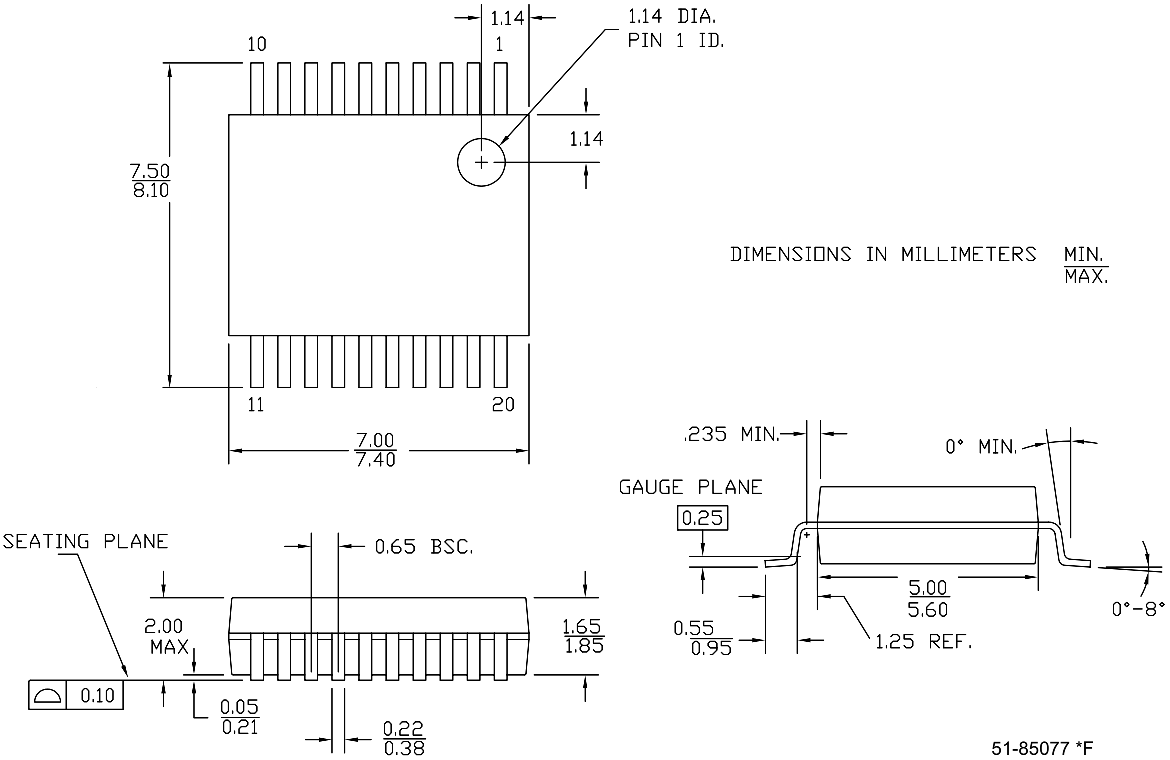
51-85066 *G

Figure 19. 20-Pin (300-Mil) Molded DIP



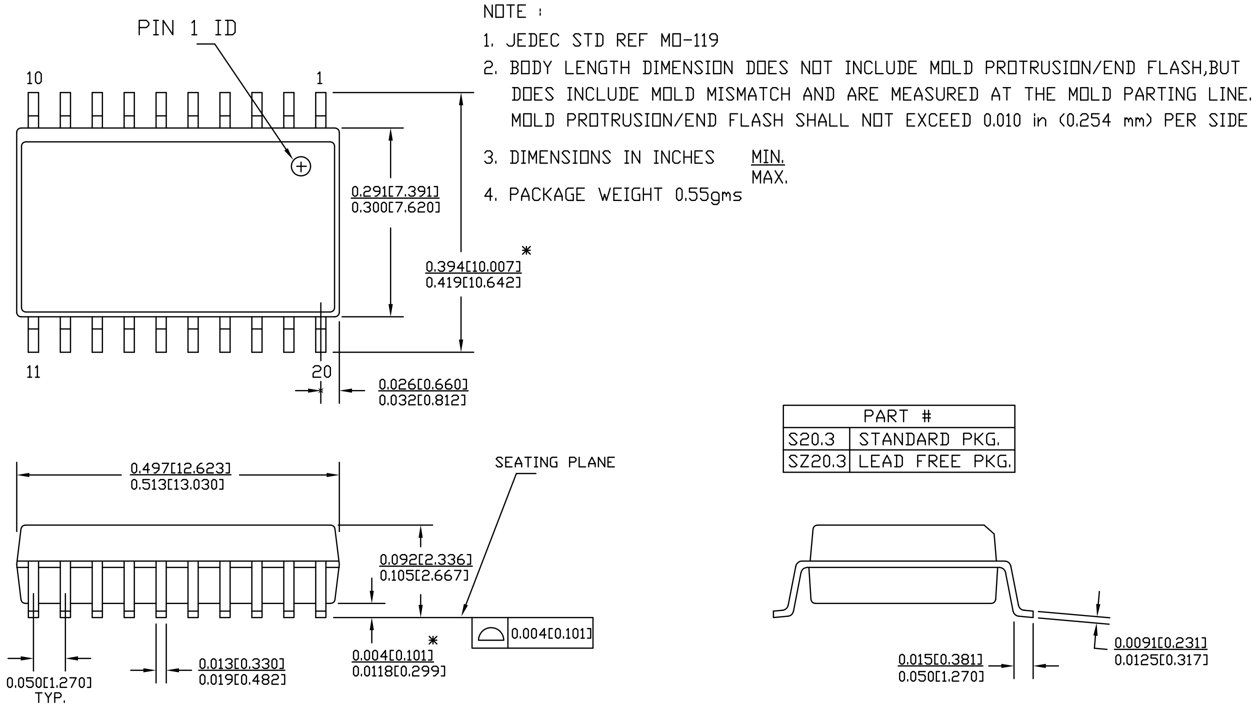
51-85011 *D

Figure 20. 20-Pin (210-Mil) SSOP



51-85077 *F

Figure 21. 20-Pin (300-Mil) Molded SOIC



NOTE :

1. JEDEC STD REF MO-119
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH,BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.010 in (0.254 mm) PER SIDE
3. DIMENSIONS IN INCHES MIN. MAX.
4. PACKAGE WEIGHT 0.55gms

PART #	
S20.3	STANDARD PKG.
SZ20.3	LEAD FREE PKG.

51-85024 *F

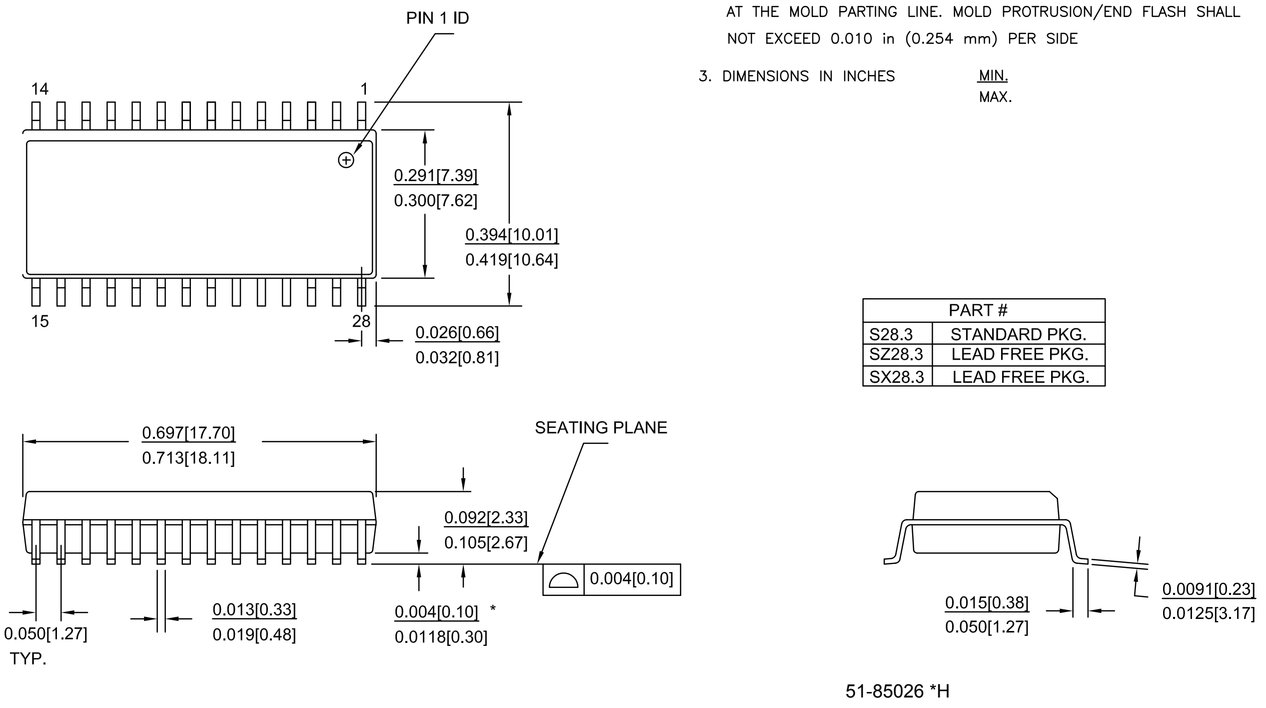


Figure 24. 28-Pin (300-Mil) Molded SOIC

NOTE :

1. JEDEC STD REF MO-119
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH,BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.010 in (0.254 mm) PER SIDE
3. DIMENSIONS IN INCHES MIN. / MAX.

PART #	
S28.3	STANDARD PKG.
SZ28.3	LEAD FREE PKG.
SX28.3	LEAD FREE PKG.

Thermal Impedances

Table 48. Thermal Impedances per Package

Package	Typical θ_{JA}[38]
8-pin PDIP	123 °C/W
8-pin SOIC	185 °C/W
20-pin PDIP	109 °C/W
20-pin SSOP	117 °C/W
20-pin SOIC	81 °C/W
28-pin PDIP	69 °C/W
28-pin SSOP	101 °C/W
28-pin SOIC	74 °C/W
32-pin QFN[39]	22 °C/W

Capacitance on Crystal Pins

Table 49. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
8-pin PDIP	2.8 pF
8-pin SOIC	2.0 pF
20-pin PDIP	3.0 pF
20-pin SSOP	2.6 pF
20-pin SOIC	2.5 pF
28-pin PDIP	3.5 pF
28-pin SSOP	2.8 pF
28-pin SOIC	2.7 pF
32-pin QFN	2.0 pF

Solder Reflow Specifications

Table 50 shows the solder reflow temperature limits that must not be exceeded.

Table 50. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
8-pin PDIP	260 °C	30 seconds
8-pin SOIC	260 °C	30 seconds
20-pin PDIP	260 °C	30 seconds
20-pin SSOP	260 °C	30 seconds
20-pin SOIC	260 °C	30 seconds
28-pin PDIP	260 °C	30 seconds
28-pin SSOP	260 °C	30 seconds
28-pin SOIC	260 °C	30 seconds
32-pin QFN	260 °C	30 seconds

Notes

38. $T_J = T_A + \text{Power} \times \theta_{JA}$
39. To achieve the thermal impedance specified for the QFN package, refer to *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages* available at www.amkor.com.

Acronyms

Acronyms Used

Table 53 lists the acronyms that are used in this document.

Table 53. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MIPS	million instructions per second
ADC	analog-to-digital converter	OCD	on-chip debug
API	application programming interface	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PDIP	plastic dual-in-line package
CPU	central processing unit	PGA	programmable gain amplifier
CRC	cyclic redundancy check	PLL	phase-locked loop
CT	continuous time	POR	power on reset
DAC	digital-to-analog converter	PPOR	precision power on reset
DC	direct current	PRS	pseudo-random sequence
DTMF	dual-tone multi-frequency	PSoC®	Programmable System-on-Chip
ECO	external crystal oscillator	PWM	pulse width modulator
EEPROM	electrically erasable programmable read-only memory	QFN	quad flat no leads
GPIO	general purpose I/O	RTC	real time clock
ICE	in-circuit emulator	SAR	successive approximation
IDE	integrated development environment	SC	switched capacitor
ILO	internal low speed oscillator	SLIMO	slow IMO
IMO	internal main oscillator	SMP	switch mode pump
I/O	input/output	SOIC	small-outline integrated circuit
IrDA	infrared data association	SPI™	serial peripheral interface
ISSP	in-system serial programming	SRAM	static random access memory
LCD	liquid crystal display	SROM	supervisory read only memory
LED	light-emitting diode	SSOP	shrink small-outline package
LPC	low power comparator	UART	universal asynchronous receiver / transmitter
LVD	low voltage detect	USB	universal serial bus
MAC	multiply-accumulate	WDT	watchdog timer
MCU	microcontroller unit	XRES	external reset

Reference Documents

CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip Technical Reference Manual (TRM) (001-14463)

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages – available at http://www.amkor.com.

Errata

This section describes the errata for the CY8C24xxxA device family. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Ordering Information
CY8C24123A	CY8C24123A-24PXI
	CY8C24123A-24SXI
	CY8C24123A-24SXIT
	CY8C24223A-24PXI
	CY8C24223A-24PVXI
	CY8C24223A-24PVXIT
	CY8C24223A-24SXI
	CY8C24223A-24SXIT
	CY8C24423A-24PXI
	CY8C24423A-24PVXI
	CY8C24423A-24PVXIT
	CY8C24423A-24SXI
	CY8C24423A-24SXIT
	CY8C24423A-24LFXI
	CY8C24423A-24LTXI
	CY8C24423A-24LTXIT
	CY8C24000A-24PVXI

CY8C24123A Qualification Status

Product Status: Production

CY8C24123A Errata Summary

The following table defines the errata applicability to available CY8C24123A family devices.

Items	Part Number	Silicon Revision	Fix Status
[1.]. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes	CY8C24123A	*A	No silicon fix planned. Workaround is required.

1. **Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes**
   - **Problem Definition**
     Asynchronous Digital Communications Interfaces may fail framing beyond 0 to 70 °C. This problem does not affect end-product usage between 0 and 70 °C.
   - **Parameters Affected**
     The IMO frequency tolerance. The worst case deviation when operated below 0°C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.
   - **Trigger Condition(S)**
     The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the data sheet limit of ±2.5% when operated beyond the temperature range of 0 to +70 °C.
   - **Scope of Impact**
     This problem may affect UART, IrDA, and FSK implementations.
   - **Workaround**
     Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.
   - **Fix Status**
     Silicon fix is not planned. The workaround mentioned above should be used.