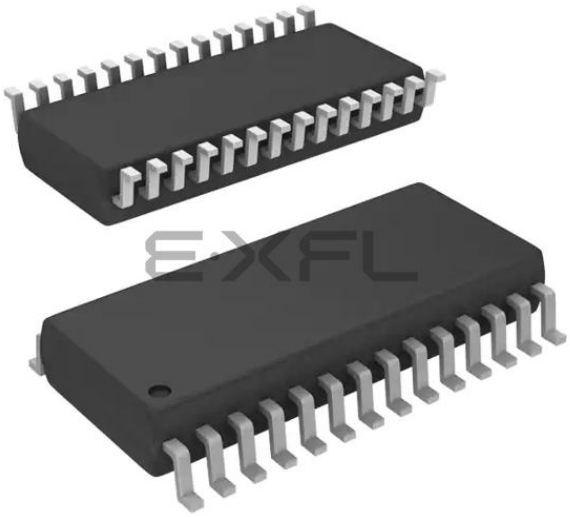

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	A/D 10x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24423a-24sxit

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. Following is an abbreviated list for PSoC 1:

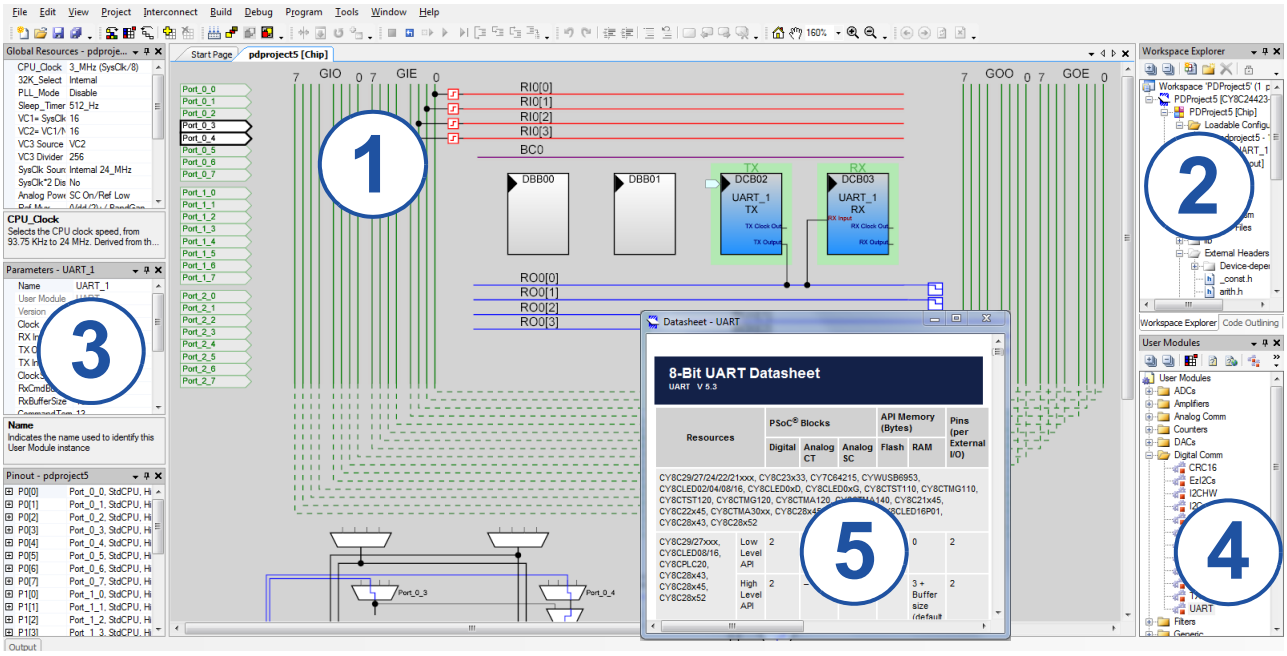
- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP
  In addition, PSoC Designer offers a device selection tool within PSoC 1, at the time of creating a new project.
- Datasheets: Describe and provide electrical specifications for all the PSoC 1 family of devices. Visit the PSoC 1 datasheets web page for a complete list
- Application notes and code examples:
  - Visit the PSoC 1 Code Examples web page for a comprehensive list of code examples
  - Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 1 are:
    - AN75320: Getting Started with PSoC® 1
    - AN2094: PSoC® 1 - Getting Started with GPIO
    - AN2015: PSoC® 1 - Getting Started with Flash & E2PROM
    - AN2014: Basics of PSoC® 1 Programming
    - AN32200: PSoC® 1 - Clocks and Global Resources
    - AN2010: PSoC® 1 Best Practices and Recommendations
- Technical Reference Manual (TRM):
  - Visit the PSoC 1 TRM page for the complete list of TRMs. Following documents provide detailed descriptions of the Architecture, Programming specification and Register map details of CY8C2XXXX PSoC 1 device family.
    - PSoC1 CY8C2XXXX TRM
    - PSoC1 ISSP Programming Specifications
- Development Kits:
  - CY3210 - CY8C24x23 PSoC(R) Evaluation Pods (EvalPod) are 28-pin PDIP adapters that seamlessly connect any PSoC device to the 28-pin PDIP connector on any Cypress PSoC development kit. CY3210-24x23 provides evaluation of the CY8C24x23A PSoC device family on any PSoC developer kit. PSoC developer kits are sold separately.
  - Visit the PSoC® 1 Kits page and refer the Kit Selector Guide document to find out the suitable development kits and debuggers for all PSoC 1 families.
- The CY3217-MiniProg1 and CY8CKIT-002 PSoC® MiniProg3 device provide an interface for flash programming.
- Knowledge Base Articles (KBA): Provide design and application tips from experts on the devices/kits. For example, Flash read/write access from firmware, explains how we can read and write to flash in PSoC 1 devices

PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of systems based on CapSense (see Figure 1). With PSoC Designer, you can:

1. Drag and drop user modules to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Designer IDE C compiler
3. Configure user module
4. Explore the library of user modules
5. Review user module datasheets

Figure 1. PSoC Designer Features



Getting Started

For in depth information, along with detailed programming details, see the PSoC® Technical Reference Manual.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable knowledge base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Register Reference

This section lists the registers of the CY8C24x23A PSoC device. For detailed register information, see the PSoC Programmable Sytem-on-Chip Reference Manual.

Register Conventions

Abbreviations Used

The register conventions specific to this section are listed in the following table.

Table 7. Abbreviations

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, Bank 0 and Bank 1. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set, the user is in Bank 1.

Note In the following register mapping tables, blank fields are reserved and must not be accessed.

DC Operational Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

The operational amplifier is a component of both the analog continuous time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the analog continuous time PSoC block. Typical parameters are measured at 5 V at 25 °C and are for design guidance only.

Table 14. 5-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 1.6 1.3 1.2	 10 8 7.5	 mV mV mV	
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	20	–	pA	Gross tested to 1 µA
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range Common mode voltage range (high power or high Opamp bias)	0.0 0.5	– –	V_{DD} V_{DD} – 0.5	V	The common mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 60 60 80	 – – –	 – – –	 dB dB dB	Specification is applicable at high Opamp bias. For low Opamp bias mode, minimum is 60 dB.
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.5	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 0.2 0.2 0.5	 V V V	
I_{SOA}	Supply current (including associated AGND buffer) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – – – –	 150 300 600 1200 2400 4600	 200 400 800 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply voltage rejection ratio	64	80	–	dB	$V_{SS} \le V_{IN} \le (V_{DD} – 2.25)$ or $(V_{DD} – 1.25\ V) \le V_{IN} \le V_{DD}$

DC Analog Output Buffer Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 18. 5-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (absolute value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	µV/°C	
V_{CMOB}	Common mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 1 1	 – –	 W W	
$V_{OHIGHOB}$	High output voltage swing (Load = 32 ohms to $V_{DD/2}$) Power = low Power = high	 0.5 × V_{DD} + 1.1 0.5 × V_{DD} + 1.1	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 32 ohms to $V_{DD/2}$) Power = low Power = high	 – –	 – –	 .5 × V_{DD} – 1.3 0.5 × V_{DD} – 1.3	 V V	
I_{SOB}	Supply current including Opamp bias cell (No Load) Power = low Power = high	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	52	64	–	dB	V_{OUT} > (V_{DD} – 1.25)

Table 19. 3.3-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load Capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (absolute value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	µV/°C	
V_{CMOB}	Common mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (Load = 1 K ohms to $V_{DD/2}$) Power = low Power = high	 0.5 × V_{DD} + 1.0 0.5 × V_{DD} + 1.0	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 1 K ohms to $V_{DD/2}$) Power = low Power = high	 – –	 – –	 0.5 × V_{DD} – 1.0 0.5 × V_{DD} – 1.0	 V V	
I_{SOB}	Supply current including Opamp bias cell (no load) Power = low Power = high	 – –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	52	64	–	dB	V_{OUT} > (V_{DD} – 1.25)

Figure 10. Basic Switch Mode Pump Circuit

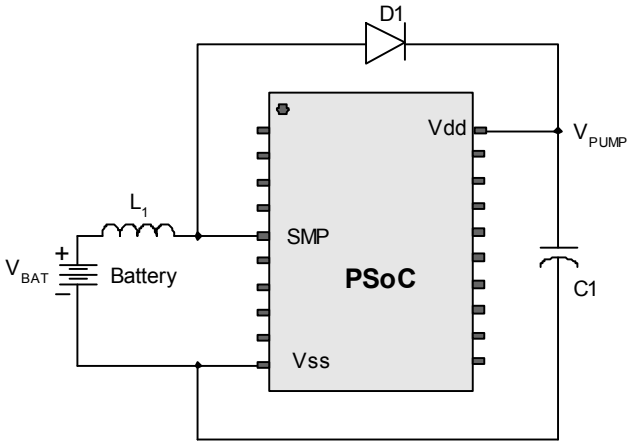


Table 22. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b101	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.228	P2[4] + 1.284	P2[4] + 1.332	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.358	P2[4] – 1.293	P2[4] – 1.226	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.236	P2[4] + 1.289	P2[4] + 1.332	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.357	P2[4] – 1.297	P2[4] – 1.229	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.237	P2[4] + 1.291	P2[4] + 1.337	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.356	P2[4] – 1.299	P2[4] – 1.232	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.237	P2[4] + 1.292	P2[4] + 1.337	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.357	P2[4] – 1.300	P2[4] – 1.233	V
0b110	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.512	2.594	2.654	V
		V_{AGND}	AGND	Bandgap	1.250	1.303	1.346	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.011	V_{SS} + 0.027	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.515	2.592	2.654	V
		V_{AGND}	AGND	Bandgap	1.253	1.301	1.340	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.02	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.518	2.593	2.651	V
		V_{AGND}	AGND	Bandgap	1.254	1.301	1.338	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.017	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.517	2.594	2.650	V
		V_{AGND}	AGND	Bandgap	1.255	1.300	1.337	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.015	V
0b111	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	3.2 × Bandgap	4.011	4.143	4.203	V
		V_{AGND}	AGND	1.6 × Bandgap	2.020	2.075	2.118	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.011	V_{SS} + 0.026	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	3.2 × Bandgap	4.022	4.138	4.203	V
		V_{AGND}	AGND	1.6 × Bandgap	2.023	2.075	2.114	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.017	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	3.2 × Bandgap	4.026	4.141	4.207	V
		V_{AGND}	AGND	1.6 × Bandgap	2.024	2.075	2.114	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.015	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	3.2 × Bandgap	4.030	4.143	4.206	V
		V_{AGND}	AGND	1.6 × Bandgap	2.024	2.076	2.112	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.013	V

Table 23. 3.3-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2 + 1.170$	$V_{DD}/2 + 1.288$	$V_{DD}/2 + 1.376$	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.098$	$V_{DD}/2 + 0.003$	$V_{DD}/2 + 0.097$	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2 – 1.386$	$V_{DD}/2 – 1.287$	$V_{DD}/2 – 1.169$	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2 + 1.210$	$V_{DD}/2 + 1.290$	$V_{DD}/2 + 1.355$	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.055$	$V_{DD}/2 + 0.001$	$V_{DD}/2 + 0.054$	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2 – 1.359$	$V_{DD}/2 – 1.292$	$V_{DD}/2 – 1.214$	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2 + 1.198$	$V_{DD}/2 + 1.292$	$V_{DD}/2 + 1.368$	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.041$	$V_{DD}/2$	$V_{DD}/2 + 0.04$	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2 – 1.362$	$V_{DD}/2 – 1.295$	$V_{DD}/2 – 1.220$	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2 + 1.202$	$V_{DD}/2 + 1.292$	$V_{DD}/2 + 1.364$	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.033$	$V_{DD}/2$	$V_{DD}/2 + 0.030$	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2 – 1.364$	$V_{DD}/2 – 1.297$	$V_{DD}/2 – 1.222$	V
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.072	P2[4] + P2[6] – 0.017	P2[4] + P2[6] + 0.041	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.029	P2[4] – P2[6] + 0.010	P2[4] – P2[6] + 0.048	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.066	P2[4] + P2[6] – 0.010	P2[4] + P2[6] + 0.043	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.024	P2[4] – P2[6] + 0.004	P2[4] – P2[6] + 0.034	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.007	P2[4] + P2[6] + 0.053	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.028	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.033	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.006	P2[4] + P2[6] + 0.056	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.030	P2[4] – P2[6]	P2[4] – P2[6] + 0.032	V
0b010	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	$V_{DD} – 0.102$	$V_{DD} – 0.003$	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.040$	$V_{DD}/2 + 0.001$	$V_{DD}/2 + 0.039$	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	$V_{SS} + 0.005$	$V_{SS} + 0.020$	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	$V_{DD} – 0.082$	$V_{DD} – 0.002$	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.031$	$V_{DD}/2$	$V_{DD}/2 + 0.028$	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	$V_{SS} + 0.003$	$V_{SS} + 0.015$	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	$V_{DD} – 0.083$	$V_{DD} – 0.002$	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.032$	$V_{DD}/2 – 0.001$	$V_{DD}/2 + 0.029$	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	$V_{SS} + 0.002$	$V_{SS} + 0.014$	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	$V_{DD} – 0.081$	$V_{DD} – 0.002$	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2 – 0.033$	$V_{DD}/2 – 0.001$	$V_{DD}/2 + 0.029$	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	$V_{SS} + 0.002$	$V_{SS} + 0.013$	V
0b011	All power settings Not allowed at 3.3 V	–	–	–	–	–	–	–

Table 24. 2.7-V DC Analog Reference Specifications (continued) (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b011	All power settings Not allowed at 2.7 V	–	–	–	–	–	–	–
0b100	All power settings Not allowed at 2.7 V	–	–	–	–	–	–	–
0b101	All power settings Not allowed at 2.7 V	–	–	–	–	–	–	–
0b110	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	Not allowed	Not allowed	Not allowed	V
		V_{AGND}	AGND	Bandgap	1.160	1.302	1.340	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.007	V_{SS} + 0.025	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	Not allowed	Not allowed	Not allowed	V
		V_{AGND}	AGND	Bandgap	1.160	1.301	1.338	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.017	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	Not allowed	Not allowed	Not allowed	V
		V_{AGND}	AGND	Bandgap	1.160	1.301	1.338	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.013	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	Not allowed	Not allowed	Not allowed	V
		V_{AGND}	AGND	Bandgap	1.160	1.300	1.337	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.011	V
	RefPower = low Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	Not allowed	Not allowed	Not allowed	V
		V_{AGND}	AGND	Bandgap	1.252	1.300	1.339	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.011	V
	RefPower = low Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	Not allowed	Not allowed	Not allowed	V
		V_{AGND}	AGND	Bandgap	1.252	1.300	1.339	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.001	V_{SS} + 0.01	V
0b111	All power settings Not allowed at 2.7 V	–	–	–	–	–	–	–

DC Analog PSoC Block Specifications

Table 23 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 25. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor unit value (continuous time)	–	12.2	–	kΩ	
C_{SC}	Capacitor unit value (switched capacitor)	–	80	–	fF	

Table 30. 2.7-V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO12}	IMO frequency for 12 MHz	11.5	12	12.7[27, 28]	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 8 on page 18. SLIMO mode = 1.
F_{IMO6}	IMO frequency for 6 MHz	5.5	6	6.5[27, 28]	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 8 on page 18. SLIMO mode = 1.
F_{CPU1}	CPU frequency (2.7 V nominal)	0.937	3	3.15[27]	MHz	SLIMO mode = 0.
F_{BLK27}	Digital PSoC block frequency (2.7 V nominal)	0	12	12.7[27, 28]	MHz	Refer to the AC Digital Block Specifications.
F_{32K1}	ILO frequency	8	32	96	kHz	
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on timing this
t_{XRST}	External reset pulse width	10	–	–	µs	
DC12M	12 MHz duty cycle	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.7	MHz	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power-up.
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the System Resets section of the PSoC Technical Reference Manual.
t_{jit_IMO}[29]	12 MHz IMO cycle-to-cycle jitter (RMS)	–	400	1000	ps	N = 32
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	600	1300	ps	
	12 MHz IMO period jitter (RMS)	–	100	500	ps	
t_{jit_PLL}[29]	12 MHz IMO cycle-to-cycle jitter (RMS)	–	400	1000	ps	N = 32
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	700	1300		
	12 MHz IMO period jitter (RMS)	–	300	500		

Notes
27. 2.4 V < V_{DD} < 3.0 V.
28. Refer to application note Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 for information on trimming for operation at 3.3 V.
29. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

Figure 11. PLL Lock Timing Diagram

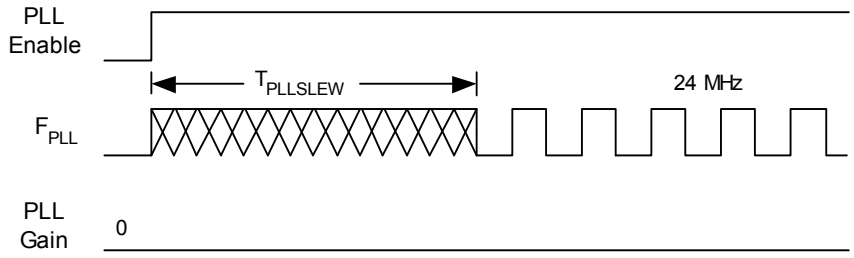


Figure 12. PLL Lock for Low Gain Setting Timing Diagram

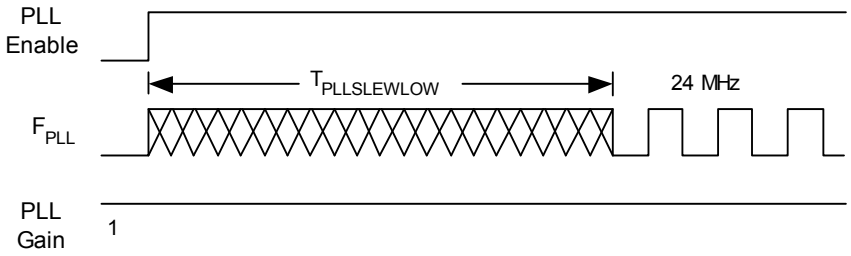
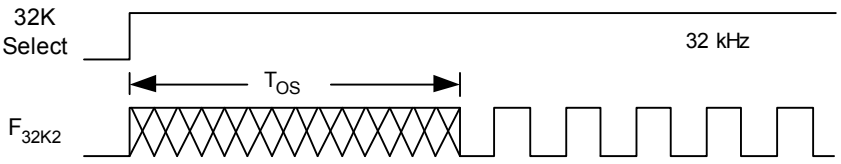


Figure 13. External Crystal Oscillator Startup Timing Diagram



AC GPIO Specifications

These tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

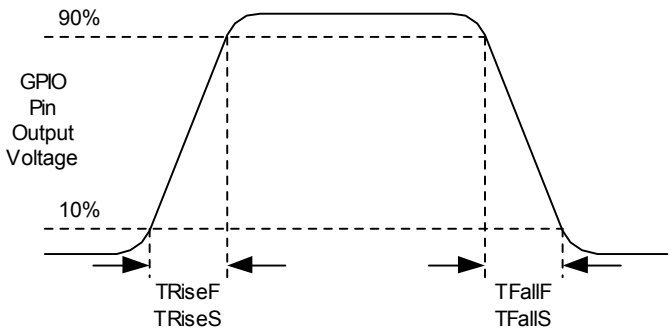
Table 31. 5-V and 3.3-V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12	MHz	Normal Strong Mode
tRiseF	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10% to 90%
tFallF	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10% to 90%
tRiseS	Rise time, slow strong mode, Cload = 50 pF	10	27	–	ns	V_{DD} = 3 to 5.25 V, 10% to 90%
tFallS	Fall time, slow strong mode, Cload = 50 pF	10	22	–	ns	V_{DD} = 3 to 5.25 V, 10% to 90%

Table 32. 2.7-V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	3	MHz	Normal strong mode
tRiseF	Rise time, normal strong mode, Cload = 50 pF	6	–	50	ns	V_{DD} = 2.4 to 3.0 V, 10% to 90%
tFallF	Fall time, normal strong mode, Cload = 50 pF	6	–	50	ns	V_{DD} = 2.4 to 3.0 V, 10% to 90%
tRiseS	Rise time, slow strong mode, Cload = 50 pF	18	40	120	ns	V_{DD} = 2.4 to 3.0 V, 10% to 90%
tFallS	Fall time, slow strong mode, Cload = 50 pF	18	40	120	ns	V_{DD} = 2.4 to 3.0 V, 10% to 90%

Figure 0-1. GPIO Timing Diagram



AC Operational Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the analog continuous time PSoC block.

Power = high and Opamp bias = high is not supported at 3.3 V and 2.7 V.

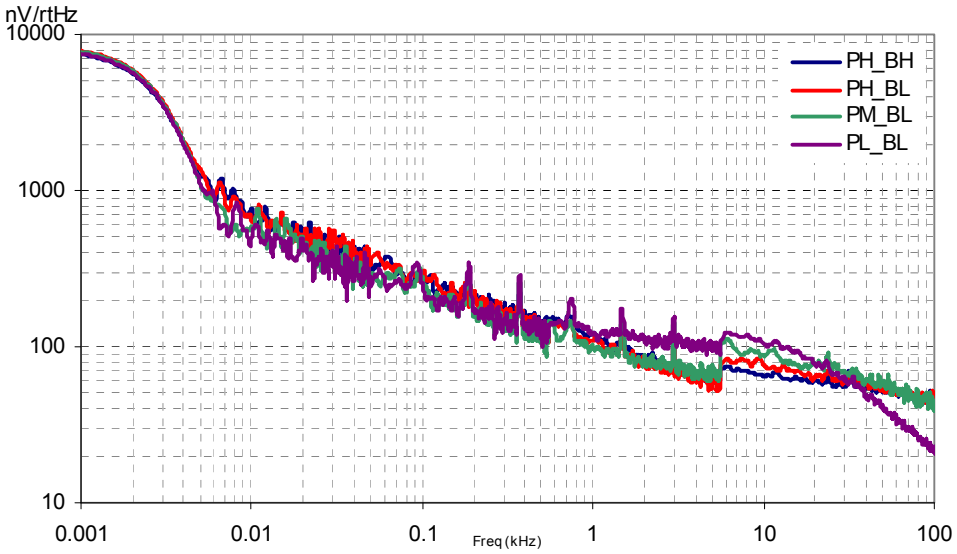
Table 33. 5-V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
t_{ROA}	Rising settling time from 80% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs
t_{SOA}	Falling settling time from 20% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs
SR_{ROA}	Rising slew rate (20% to 80%) (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 0.15 1.7 6.5	 – – –	 – – –	 V/µs V/µs V/µs
SR_{FOA}	Falling slew rate (20% to 80%) (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 0.01 0.5 4.0	 – – –	 – – –	 V/µs V/µs V/µs
BW_{OA}	Gain bandwidth product Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz
E_{NOA}	Noise at 1 kHz (Power = medium, Opamp bias = high)	–	100	–	nV/rt-Hz

Table 34. 3.3-V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
t_{ROA}	Rising settling time from 80% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 – –	 – –	 3.92 0.72	 µs µs
t_{SOA}	Falling settling time from 20% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 – –	 – –	 5.41 0.72	 µs µs
SR_{ROA}	Rising slew rate (20% to 80%) (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 0.31 2.7	 – –	 – –	 V/µs V/µs
SR_{FOA}	Falling slew rate (20% to 80%) (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 0.24 1.8	 – –	 – –	 V/µs V/µs
BW_{OA}	Gain bandwidth product Power = low, Opamp bias = low Power = medium, Opamp bias = high	 0.67 2.8	 – –	 – –	 MHz MHz
E_{NOA}	Noise at 1 kHz (Power = medium, Opamp bias = high)	–	100	–	nV/rt-Hz

Figure 15. Typical Opamp Noise



AC Low Power Comparator Specifications

Table 36 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V at 25 °C and are for design guidance only.

Table 36. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}

Figure 20. 20-Pin (210-Mil) SSOP

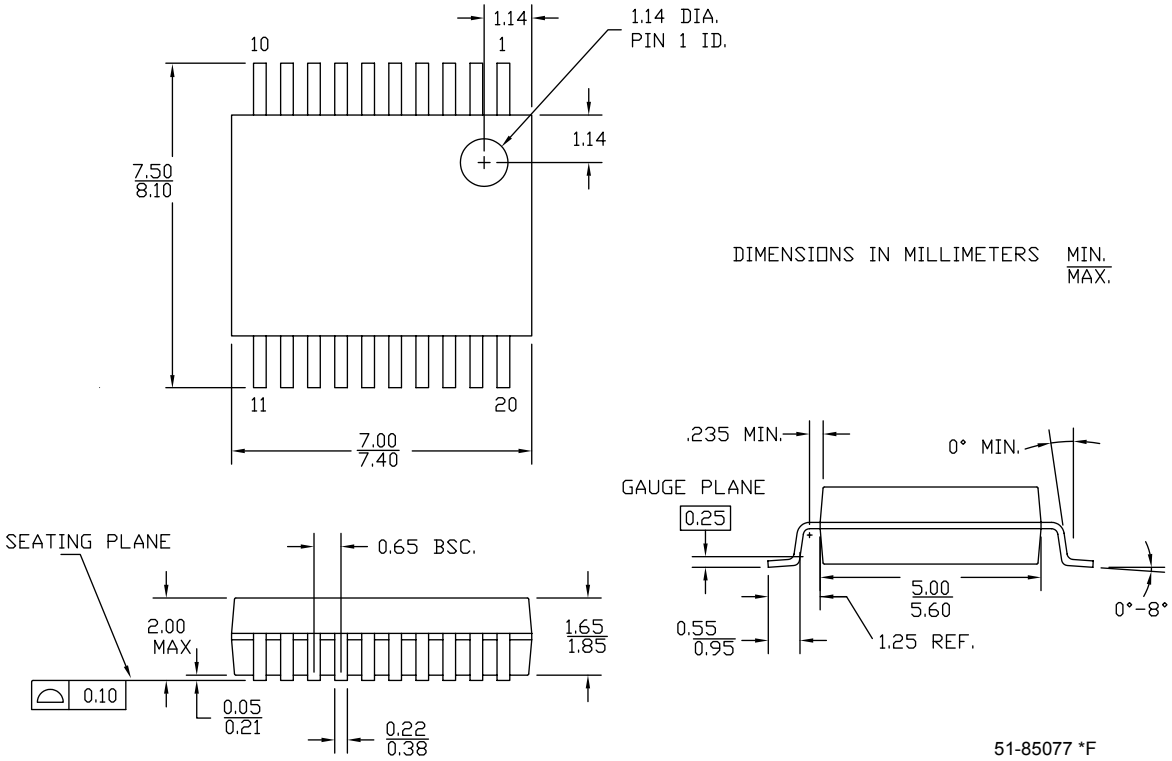


Figure 21. 20-Pin (300-Mil) Molded SOIC

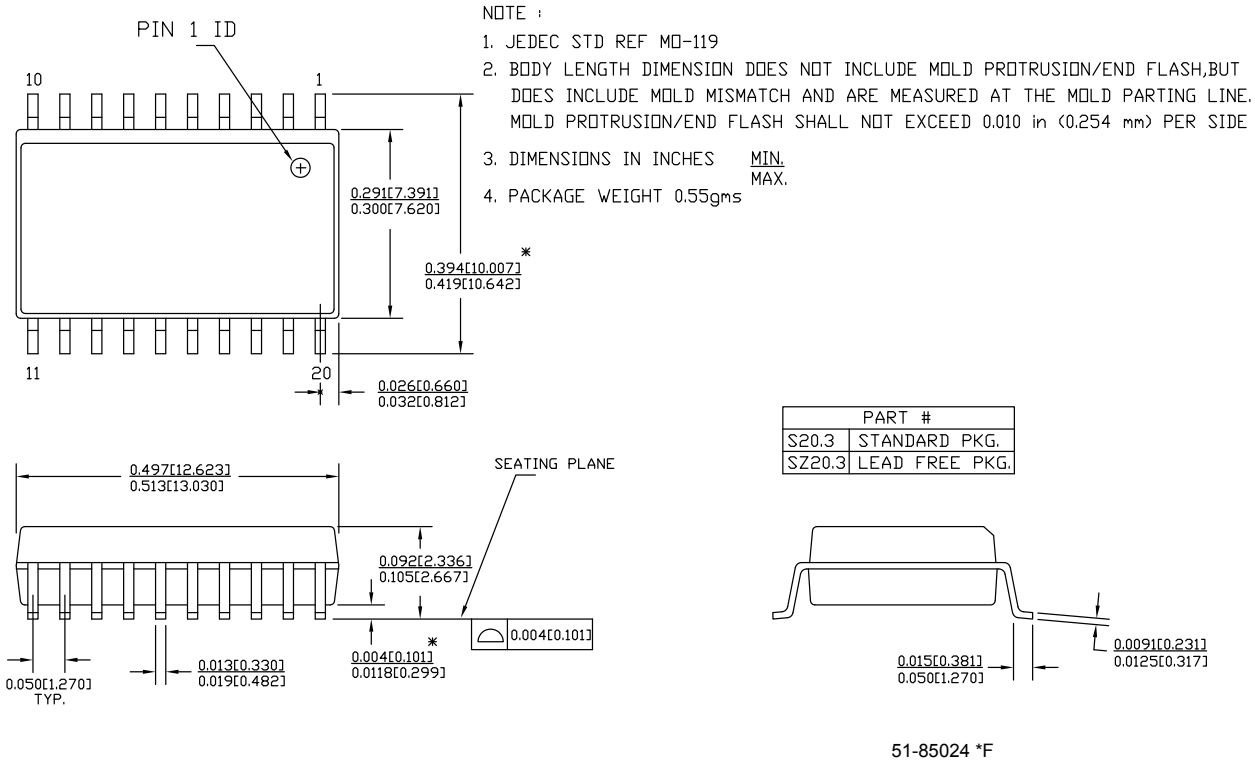


Figure 22. 28-Pin (300-Mil) Molded DIP

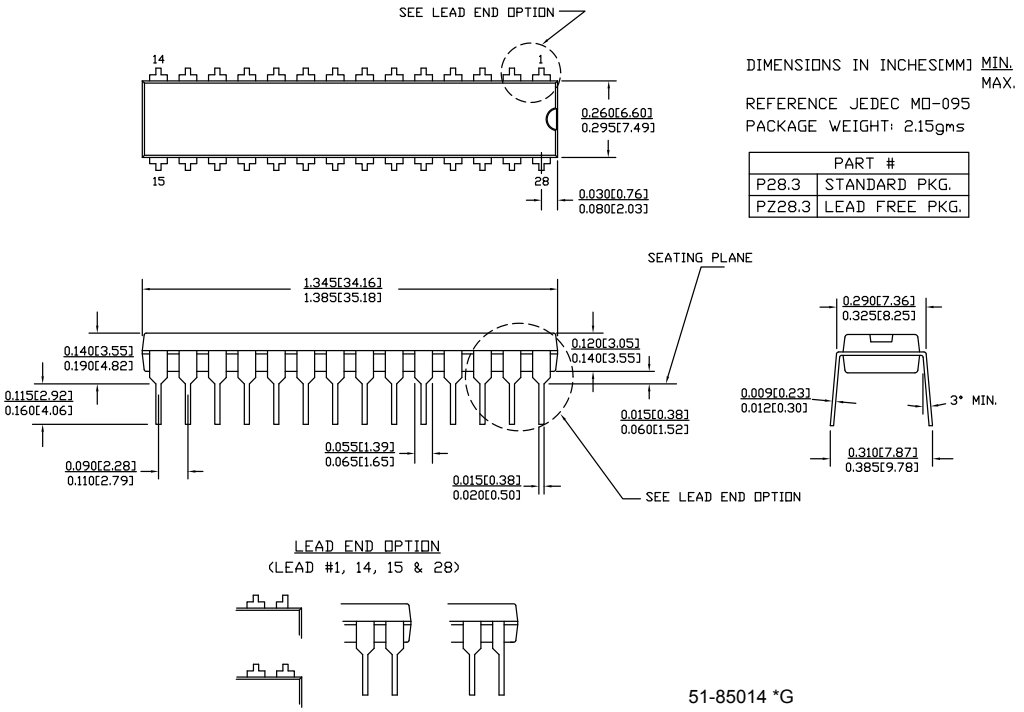
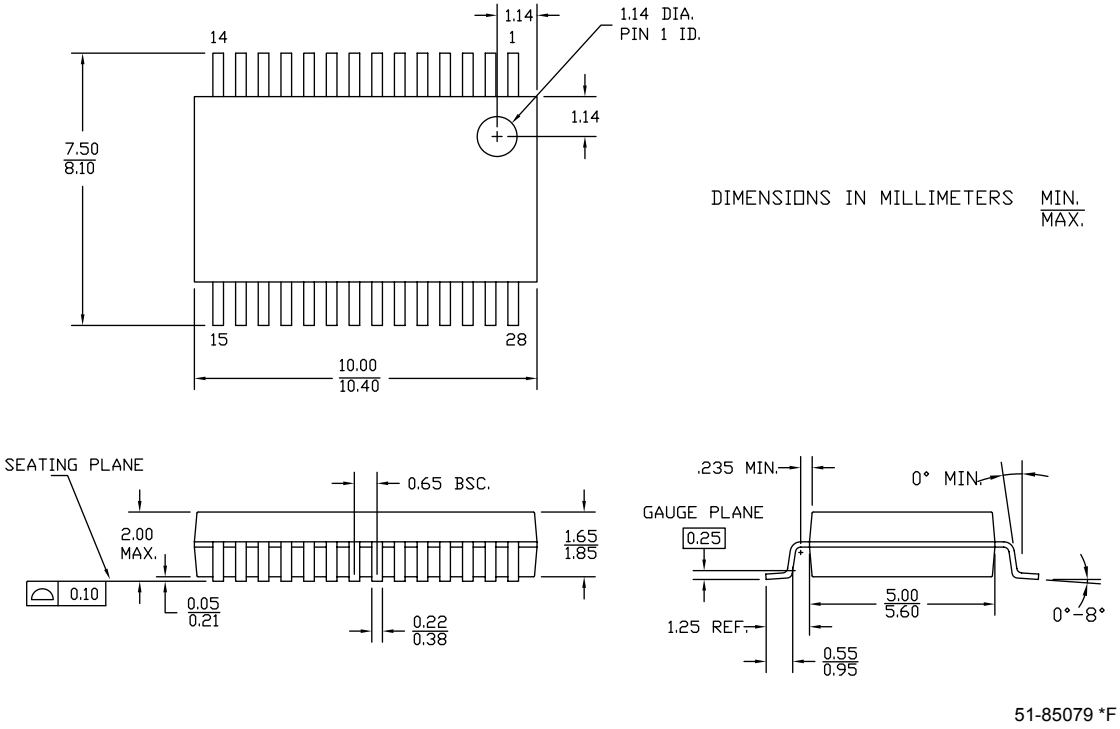


Figure 23. 28-Pin (210-Mil) SSOP



Acronyms

Acronyms Used

Table 53 lists the acronyms that are used in this document.

Table 53. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MIPS	million instructions per second
ADC	analog-to-digital converter	OCD	on-chip debug
API	application programming interface	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PDIP	plastic dual-in-line package
CPU	central processing unit	PGA	programmable gain amplifier
CRC	cyclic redundancy check	PLL	phase-locked loop
CT	continuous time	POR	power on reset
DAC	digital-to-analog converter	PPOR	precision power on reset
DC	direct current	PRS	pseudo-random sequence
DTMF	dual-tone multi-frequency	PSoC®	Programmable System-on-Chip
ECO	external crystal oscillator	PWM	pulse width modulator
EEPROM	electrically erasable programmable read-only memory	QFN	quad flat no leads
GPIO	general purpose I/O	RTC	real time clock
ICE	in-circuit emulator	SAR	successive approximation
IDE	integrated development environment	SC	switched capacitor
ILO	internal low speed oscillator	SLIMO	slow IMO
IMO	internal main oscillator	SMP	switch mode pump
I/O	input/output	SOIC	small-outline integrated circuit
IrDA	infrared data association	SPI™	serial peripheral interface
ISSP	in-system serial programming	SRAM	static random access memory
LCD	liquid crystal display	SROM	supervisory read only memory
LED	light-emitting diode	SSOP	shrink small-outline package
LPC	low power comparator	UART	universal asynchronous receiver / transmitter
LVD	low voltage detect	USB	universal serial bus
MAC	multiply-accumulate	WDT	watchdog timer
MCU	microcontroller unit	XRES	external reset

Reference Documents

CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip Technical Reference Manual (TRM) (001-14463)

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages – available at http://www.amkor.com.

Document Conventions

Units of Measure

Table 54 lists the unit sof measures.

Table 54. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
kB	1024 bytes	µs	microsecond
dB	decibels	ms	millisecond
°C	degree Celsius	ns	nanosecond
fF	femto farad	ps	picosecond
pF	picofarad	µV	microvolts
kHz	kilohertz	mV	millivolts
MHz	megahertz	mVpp	millivolts peak-to-peak
rt-Hz	root hertz	nV	nanovolts
kΩ	kilohm	V	volts
Ω	ohm	µW	microwatts
µA	microampere	W	watt
mA	milliampere	mm	millimeter
nA	nanoampere	ppm	parts per million
pA	pikoampere	%	percent
mH	millihenry		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	10.A logic signal having its asserted state as the logic 1 state. 11.A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
API (Application Programming Interface)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
Bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.

Glossary (continued)

shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Document History Page (continued)

Document Title: CY8C24123A/CY8C24223A/CY8C24423A, PSoC® Programmable System-on-Chip Document Number: 38-12028				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*L	2897881	MAXK / NJF	03/23/2010	Add "More Information" on page 2. Update unit in Table 10-28 and Table 38 of SPIS Maximum Input Clock Frequency from ns to MHz. Update revision of package diagrams for 8 PDIP, 8 SOIC, 20 PDIP, 20 SSOP, 20 SOIC, 28 PDIP, 28 SSOP, 28 SOIC, 32 QFN. Updated Cypress website links. Removed reference to PSoC Designer 4.4. Updated 56-Pin SSOP definitions and diagram. Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings. Updated 5-V DC Analog Reference Specifications table. Updated Note in Packaging Information. Added Note 29. Updated Solder Reflow Specifications table. Removed Third Party Tools and Build a PSoC Emulator into your Board. Removed inactive parts from Ordering Information. Update trademark info. and Sales, Solutions, and Legal Information.
*M	2942375	VMAD	06/02/2010	Updated content to match current style guide and datasheet template. No technical updates.
*N	3032514	NJF	09/17/10	Added PSoC Device Characteristics table. Added DC I^2C Specifications table. Added F_{32K_U} max limit. Added Tjit_IMO specification, removed existing jitter specifications. Updated Analog reference tables. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changes were made to AC Digital Block Specifications table and I^2C Timing Diagram. They were updated for clearer understanding. Updated Figure 13 since the labelling for y-axis was incorrect. Template and styles update.
*O	3098766	YJI	12/01/2010	Sunset review; no content update
*P	3351721	YJI	08/31/2011	Full annual review of document. No changes are required.
*Q	3367463	BTK / GIR	09/22/2011	Updated text under DC Analog Reference Specifications on page 28. Removed package diagram spec 51-85188 as there is no active MPN using this outline drawing. The text "Pin must be left floating" is included under Description of NC pin in Table 5 on page 13 and Table 6 on page 14. Updated Table 50 on page 57 to give more clarity. Removed Footnote #35.
*R	3598291	LURE / XZNG	04/24/2012	Changed the PWM description string from "8- to 32-bit" to "8- and 16-bit".
*S	3991993	PMAD	05/08/2013	Updated Packaging Information: spec 51-85066 – Changed revision from *E to *F. spec 51-85014 – Changed revision from *F to *G. spec 51-85026 – Changed revision from *F to *G. spec 001-30999 – Changed revision from *C to *D. spec 51-85062 – Changed revision from *E to *F. Updated Reference Documents (Removed 001-17397 spec, 001-14503 spec related information). Added Errata.