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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	A/D 10x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24423a4-24ltxi

Contents

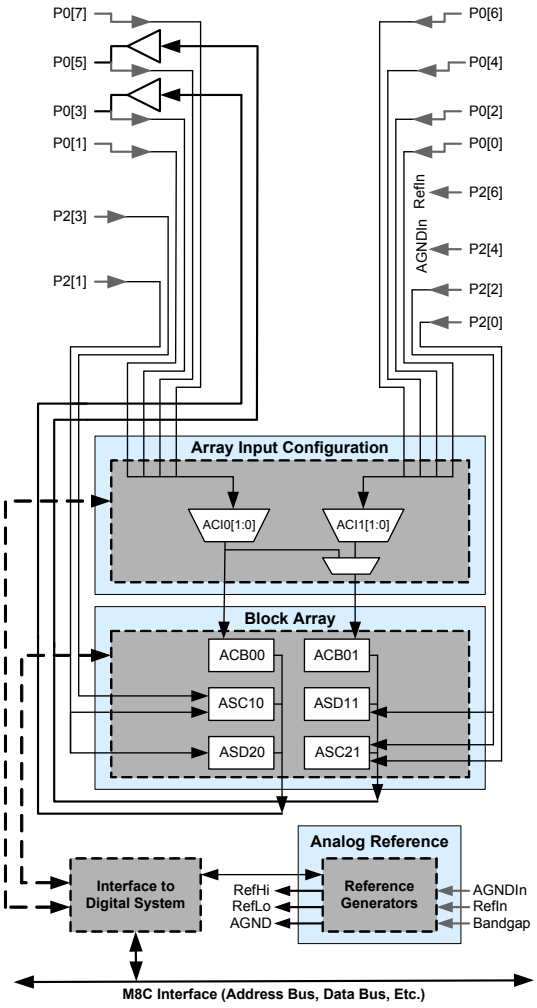
Analog System

The analog system consists of six configurable blocks, each consisting of an opamp circuit that allows the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- ADCs (up to two, with 6- to 14-bit resolution, selectable as incremental, delta sigma, and SAR)
- Filters (two and four pole band-pass, low-pass, and notch)
- Amplifiers (up to two, with selectable gain to 48x)
- Instrumentation amplifiers (one with selectable gain to 93x)
- Comparators (up to two, with 16 selectable thresholds)
- DACs (up to two, with 6 to 9-bit resolution)
- Multiplying DACs (up to two, with 6 to 9-bit resolution)
- High current output drivers (two with 30 mA drive as a PSoC Core resource)
- 1.3 V reference (as a system resource)
- DTMF dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are arranged in a column of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks, as shown in Figure 3

Figure 3. Analog System Block Diagram



Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

6. Select user modules.
7. Configure user modules.
8. Organize and connect.
9. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

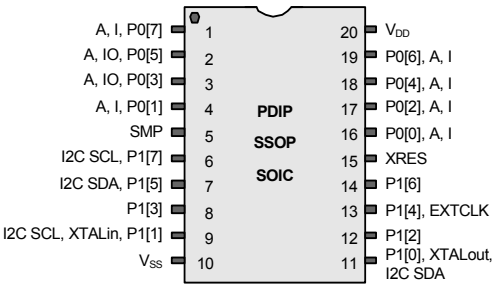
20-Pin Part Pinout

Table 3. 20-Pin PDIP, SSOP, and SOIC

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I/O	P0[5]	Analog column mux input and column output
3	I/O	I/O	P0[3]	Analog column mux input and column output
4	I/O	I	P0[1]	Analog column mux input
5	Power		SMP	SMP connection to external components required
6	I/O		P1[7]	I^2C SCL
7	I/O		P1[5]	I^2C SDA
8	I/O		P1[3]	
9	I/O		P1[1]	XTALin, I^2C SCL, ISSP-SCLK[5]
10	Power		V_{SS}	Ground connection.
11	I/O		P1[0]	XTALout, I^2C SDA, ISSP-SDATA[5]
12	I/O		P1[2]	
13	I/O		P1[4]	Optional external clock input (EXTCLK)
14	I/O		P1[6]	
15	Input		XRES	Active high external reset with internal pull-down
16	I/O	I	P0[0]	Analog column mux input
17	I/O	I	P0[2]	Analog column mux input
18	I/O	I	P0[4]	Analog column mux input
19	I/O	I	P0[6]	Analog column mux input
20	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 5. CY8C24223A 20-Pin PSoC Device



Note
5. These are the ISSP pins, which are not high Z at POR. See the PSoC Technical Reference Manual for details.

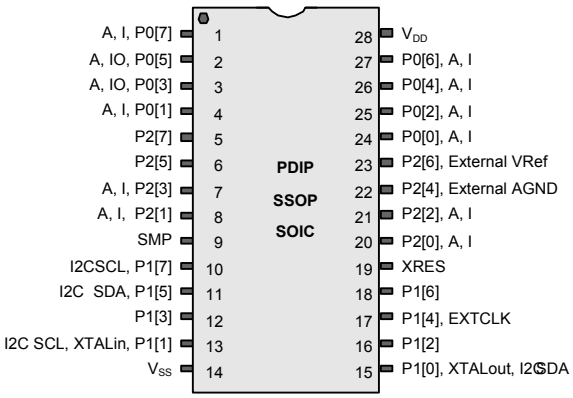
28-Pin Part Pinout

Table 4. 28-Pin PDIP, SSOP, and SOIC

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I/O	P0[5]	Analog column mux input and column output
3	I/O	I/O	P0[3]	Analog column mux input and column output
4	I/O	I	P0[1]	Analog column mux input
5	I/O		P2[7]	
6	I/O		P2[5]	
7	I/O	I	P2[3]	Direct switched capacitor block input
8	I/O	I	P2[1]	Direct switched capacitor block input
9	Power		SMP	SMP connection to external components required
10	I/O		P1[7]	I^2C SCL
11	I/O		P1[5]	I^2C SDA
12	I/O		P1[3]	
13	I/O		P1[1]	XTALin, I^2C SCL, ISSP-SCLK[6]
14	Power		V_{SS}	Ground connection.
15	I/O		P1[0]	XTALout, I^2C SDA, ISSP-SDATA[6]
16	I/O		P1[2]	
17	I/O		P1[4]	Optional EXTCLK
18	I/O		P1[6]	
19	Input		XRES	Active high external reset with internal pull-down
20	I/O	I	P2[0]	Direct switched capacitor block input
21	I/O	I	P2[2]	Direct switched capacitor block input
22	I/O		P2[4]	External analog ground (AGND)
23	I/O		P2[6]	External voltage reference (V_{REF})
24	I/O	I	P0[0]	Analog column mux input
25	I/O	I	P0[2]	Analog column mux input
26	I/O	I	P0[4]	Analog column mux input
27	I/O	I	P0[6]	Analog column mux input
28	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 6. CY8C24423A 28-Pin PSoC Device



Not for Production

Note
6. These are the ISSP pins, which are not high Z at POR. See the PSoC Technical Reference Manual for details.

Register Reference

This section lists the registers of the CY8C24x23A PSoC device. For detailed register information, see the PSoC Programmable Sytem-on-Chip Reference Manual.

Register Conventions

Abbreviations Used

The register conventions specific to this section are listed in the following table.

Table 7. Abbreviations

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, Bank 0 and Bank 1. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set, the user is in Bank 1.

Note In the following register mapping tables, blank fields are reserved and must not be accessed.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C24x23A PSoC device. For the latest electrical specifications, check if you have the most recent datasheet by visiting the website at http://www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted.

Refer to Table 29 on page 37 for the electrical specifications for the IMO using SLIMO mode.

Figure 9. Voltage versus CPU Frequency

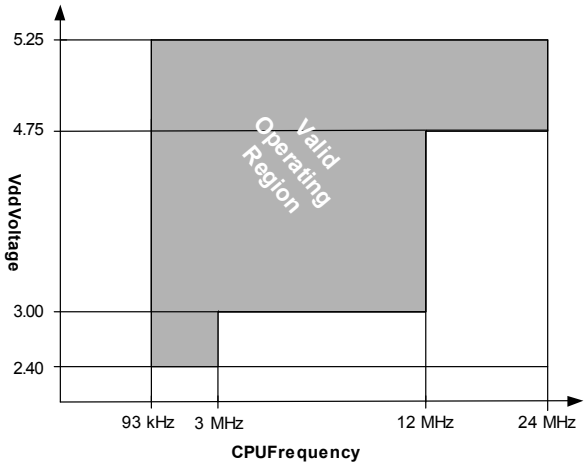
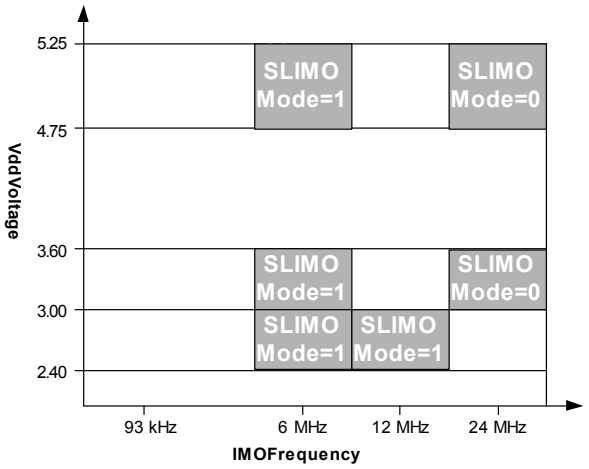


Figure 8. IMO Frequency Trim Options



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 9. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 65 °C degrades reliability.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	
$t_{BAKETIME}$	Bake time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied	–40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tri-state	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
ESD	Electrostatic discharge voltage	2000	–	–	V	Human body model ESD.
LU	Latch up current	–	–	200	mA	

DC GPIO Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 12. 5-V and 3.3-V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	
V_{OH}	High output level	V_{DD} – 1.0	–	–	V	I_{OH} = 10 mA, V_{DD} = 4.75 to 5.25 V (maximum 40 mA on even port pins (for example, P0[2], P1[4]), maximum 40 mA on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I_{OH} budget.
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 25 mA, V_{DD} = 4.75 to 5.25 V (maximum 100 mA on even port pins (for example, P0[2], P1[4]), maximum 100 mA on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I_{OL} budget.
I_{OH}	High level source current	10	–	–	mA	V_{OH} = V_{DD} – 1.0 V, see the limitations of the total current in the note for V_{OH}
I_{OL}	Low level sink current	25	–	–	mA	V_{OL} = 0.75 V, see the limitations of the total current in the note for V_{OL}
V_{IL}	Input low level	–	–	0.8	V	V_{DD} = 3.0 to 5.25
V_{IH}	Input high level	2.1	–		V	V_{DD} = 3.0 to 5.25
V_H	Input hysterisis	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C

Table 13. 2.7-V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	
V_{OH}	High output level	V_{DD} – 0.4	–	–	V	I_{OH} = 2 mA (6.25 Typ), V_{DD} = 2.4 to 3.0 V (16 mA maximum, 50 mA Typ combined I_{OH} budget).
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 11.25 mA, V_{DD} = 2.4 to 3.0 V (90 mA maximum combined I_{OL} budget).
I_{OH}	High level source current	2	–	–	mA	V_{OH} = V_{DD} – 0.4, see the limitations of total current in note for V_{OH}.
V_{IL}	Input low level	–	–	0.75	V	V_{DD} = 2.4 to 3.0
V_{IH}	Input high level	2.0	–	–	V	V_{DD} = 2.4 to 3.0
V_H	Input hysteresis	–	90	–	mV	
I_{OL}	Low level sink current	11.25	–	–	mA	V_{OL} = .75, see the limitations of total current in note for V_{OL}.
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C

DC Switch Mode Pump Specifications

Table 21 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 21. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PUMP} 5 V	5 V output voltage from pump	4.75	5.0	5.25	V	Configuration listed in footnote.[11] Average, neglecting ripple. SMP trip voltage is set to 5.0 V.
V_{PUMP} 3 V	3.3 V output voltage from pump	3.00	3.25	3.60	V	Configuration listed in footnote.[11] Average, neglecting ripple. SMP trip voltage is set to 3.25 V.
V_{PUMP} 2 V	2.6 V output voltage from pump	2.45	2.55	2.80	V	Configuration listed in footnote.[11] Average, neglecting ripple. SMP trip voltage is set to 2.55 V.
I_{PUMP}	Available output current V_{BAT} = 1.8 V, V_{PUMP} = 5.0 V V_{BAT} = 1.5 V, V_{PUMP} = 3.25 V V_{BAT} = 1.3 V, V_{PUMP} = 2.55 V	 5 8 8	 – – –	 – – –	 mA mA mA	Configuration listed in footnote.[11] SMP trip voltage is set to 5.0 V. SMP trip voltage is set to 3.25 V. SMP trip voltage is set to 2.55 V.
V_{BAT}5 V	Input voltage range from battery	1.8	–	5.0	V	Configuration listed in footnote.[11] SMP trip voltage is set to 5.0 V.
V_{BAT}3 V	Input voltage range from battery	1.0	–	3.3	V	Configuration listed in footnote.[11] SMP trip voltage is set to 3.25 V.
V_{BAT}2 V	Input voltage range from battery	1.0	–	3.0	V	Configuration listed in footnote.[11] SMP trip voltage is set to 2.55 V.
$V_{BATSTART}$	Minimum input voltage from battery to start pump	1.2	–	–	V	Configuration listed in footnote.[11] 0 °C ≤ T_A ≤ 100. 1.25 V at T_A = –40 °C
ΔV_{PUMP_Line}	Line regulation (over V_{BAT} range)	–	5	–	$\%V_O$	Configuration listed in footnote.[11] V_O is the V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 26 on page 35.
ΔV_{PUMP_Load}	Load regulation	–	5	–	$\%V_O$	Configuration listed in footnote.[11] V_O is the "V_{DD} value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 26 on page 35.
ΔV_{PUMP_Ripple}	Output voltage ripple (depends on capacitor/load)	–	100	–	mVpp	Configuration listed in footnote.[11] Load is 5 mA.
E_3	Efficiency	35	50	–	%	Configuration listed in footnote.[11] Load is 5 mA. SMP trip voltage is set to 3.25 V.
E_2	Efficiency	–	–	–		
F_{PUMP}	Switching frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching duty cycle	–	50	–	%	

Note
11. L_1 = 2 mH inductor, C_1 = 10 mF capacitor, D_1 = Schottky diode. See Figure 10

DC POR, SMP, and LVD Specifications

Table 24 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the PSoC Programmable Sytem-on-Chip Technical Reference Manual for more information on the VLT_CR register.

Table 26. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip					V_{DD} must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b		2.82	2.95	V	
V_{PPOR2}	PORLEV[1:0] = 10b		4.55	4.70	V	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.40	2.45	2.51[12]	V	
V_{LVD1}	VM[2:0] = 001b	2.85	2.92	2.99[13]	V	
V_{LVD2}	VM[2:0] = 010b	2.95	3.02	3.09	V	
V_{LVD3}	VM[2:0] = 011b	3.06	3.13	3.20	V	
V_{LVD4}	VM[2:0] = 100b	4.37	4.48	4.55	V	
V_{LVD5}	VM[2:0] = 101b	4.50	4.64	4.75	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	
	V_{DD} value for SMP trip					
V_{PUMP0}	VM[2:0] = 000b	2.50	2.55	2.62[14]	V	
V_{PUMP1}	VM[2:0] = 001b	2.96	3.02	3.09	V	
V_{PUMP2}	VM[2:0] = 010b	3.03	3.10	3.16	V	
V_{PUMP3}	VM[2:0] = 011b	3.18	3.25	3.32[15]	V	
V_{PUMP4}	VM[2:0] = 100b	4.54	4.64	4.74	V	
V_{PUMP5}	VM[2:0] = 101b	4.62	4.73	4.83	V	
V_{PUMP6}	VM[2:0] = 110b	4.71	4.82	4.92	V	
V_{PUMP7}	VM[2:0] = 111b	4.89	5.00	5.12	V	

Notes
12. Always greater than 50 mV above V_{PPOR} (PORLEV=00) for falling supply.
13. Always greater than 50 mV above V_{PPOR} (PORLEV=01) for falling supply.
14. Always greater than 50 mV above V_{LVD0}.
15. Always greater than 50 mV above V_{LVD3}.

DC Programming Specifications

Table 27 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 27. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	2.4	2.5	2.6	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	2.7		5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.1	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)	50,000[16]	–	–	–	Erase/write cycles per block
$Flash_{ENT}$	Flash endurance (total)[17]	1,800,000	–	–	–	Erase/write cycles
$Flash_{DR}$	Flash data retention	10	–	–	Years	

DC I^2C Specifications

Table 28 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 28. DC I^2C Specifications[18]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	2.4 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	2.4 V ≤ V_{DD} ≤ 5.25 V

Notes
16. The 50,000 cycle flash endurance per block is only guaranteed if the flash is operating within one voltage range. Voltage ranges are 2.4 V to 3.0 V, 3.0 V to 3.6 V, and 4.75 V to 5.25 V.
17. A maximum of 36 × 50,000 block endurance cycles is allowed. This may be balanced between operations on 36 × 1 blocks of 50,000 maximum cycles each, 36 × 2 blocks of 25,000 maximum cycles each, or 36 × 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 × 50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs application note Design Aids – Reading and Writing PSoC® Flash – AN2015 for more information.
18. All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I^2C GPIO pins also meet the above specs.

Table 30. 2.7-V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO12}	IMO frequency for 12 MHz	11.5	12	12.7[27, 28]	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 8 on page 18. SLIMO mode = 1.
F_{IMO6}	IMO frequency for 6 MHz	5.5	6	6.5[27, 28]	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 8 on page 18. SLIMO mode = 1.
F_{CPU1}	CPU frequency (2.7 V nominal)	0.937	3	3.15[27]	MHz	SLIMO mode = 0.
F_{BLK27}	Digital PSoC block frequency (2.7 V nominal)	0	12	12.7[27, 28]	MHz	Refer to the AC Digital Block Specifications.
F_{32K1}	ILO frequency	8	32	96	kHz	
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on timing this
t_{XRST}	External reset pulse width	10	–	–	µs	
DC12M	12 MHz duty cycle	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.7	MHz	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power-up.
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the System Resets section of the PSoC Technical Reference Manual.
t_{jit_IMO}[29]	12 MHz IMO cycle-to-cycle jitter (RMS)	–	400	1000	ps	N = 32
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	600	1300	ps	
	12 MHz IMO period jitter (RMS)	–	100	500	ps	
t_{jit_PLL}[29]	12 MHz IMO cycle-to-cycle jitter (RMS)	–	400	1000	ps	N = 32
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	700	1300		
	12 MHz IMO period jitter (RMS)	–	300	500		

Notes
27. 2.4 V < V_{DD} < 3.0 V.
28. Refer to application note Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 for information on trimming for operation at 3.3 V.
29. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

Figure 18. 8-Pin (150-Mil) SOIC

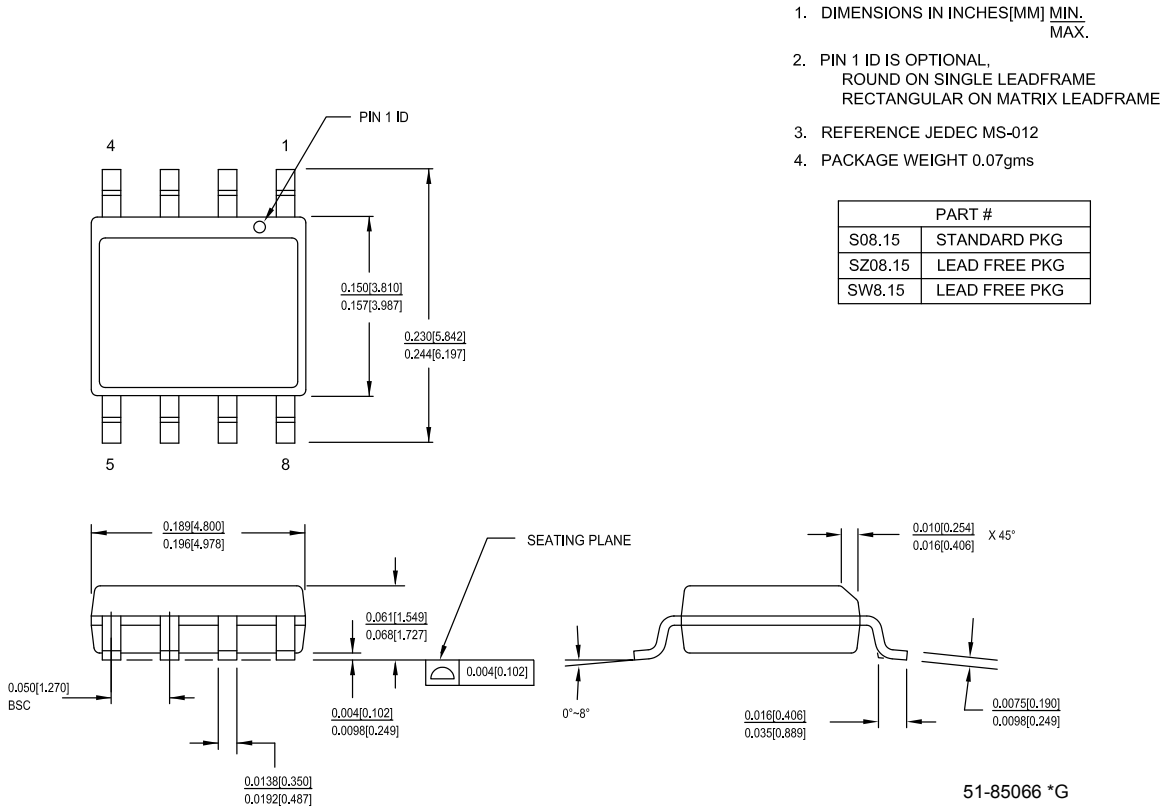


Figure 19. 20-Pin (300-Mil) Molded DIP

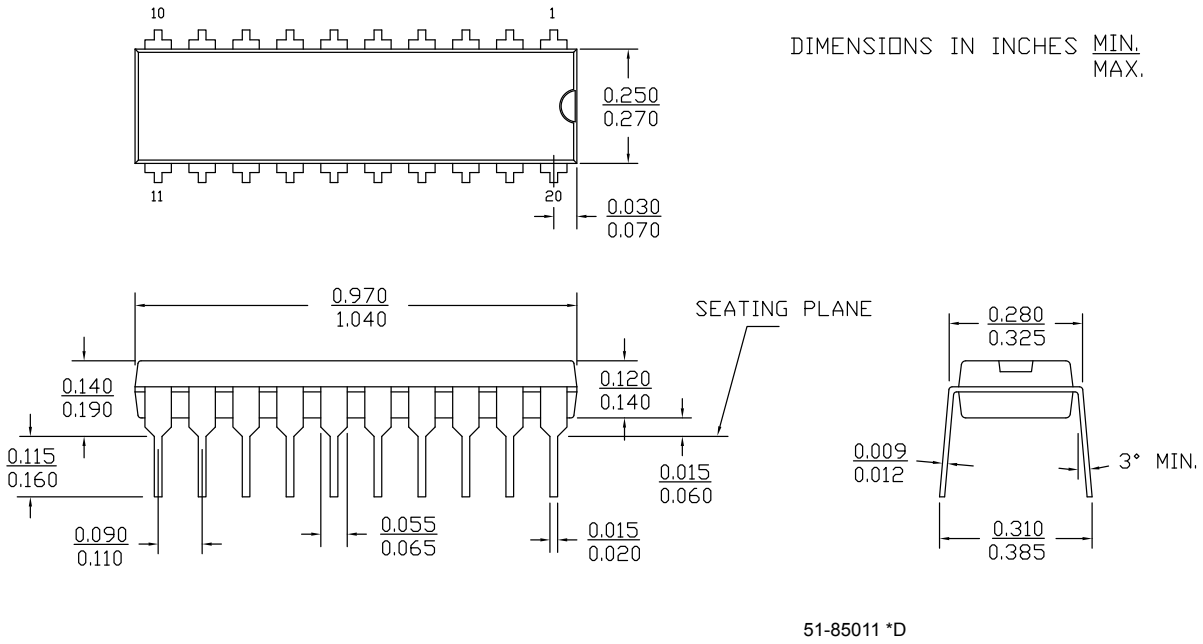


Figure 20. 20-Pin (210-Mil) SSOP

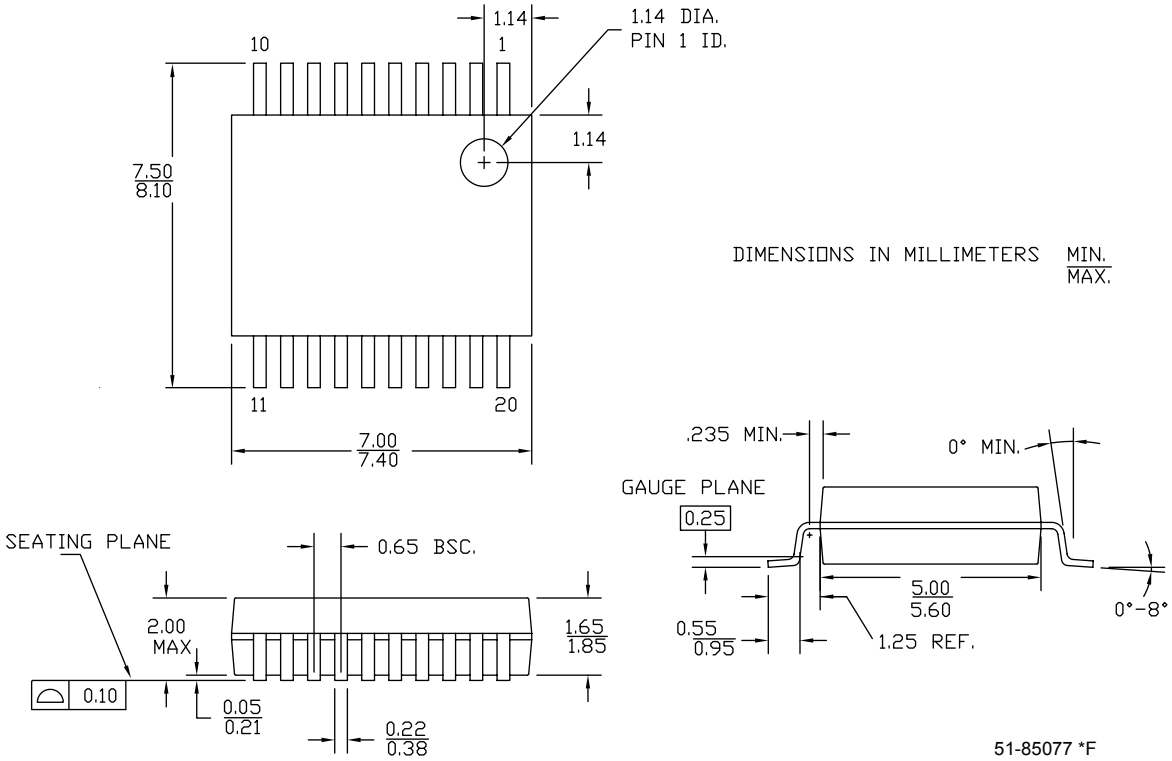


Figure 21. 20-Pin (300-Mil) Molded SOIC

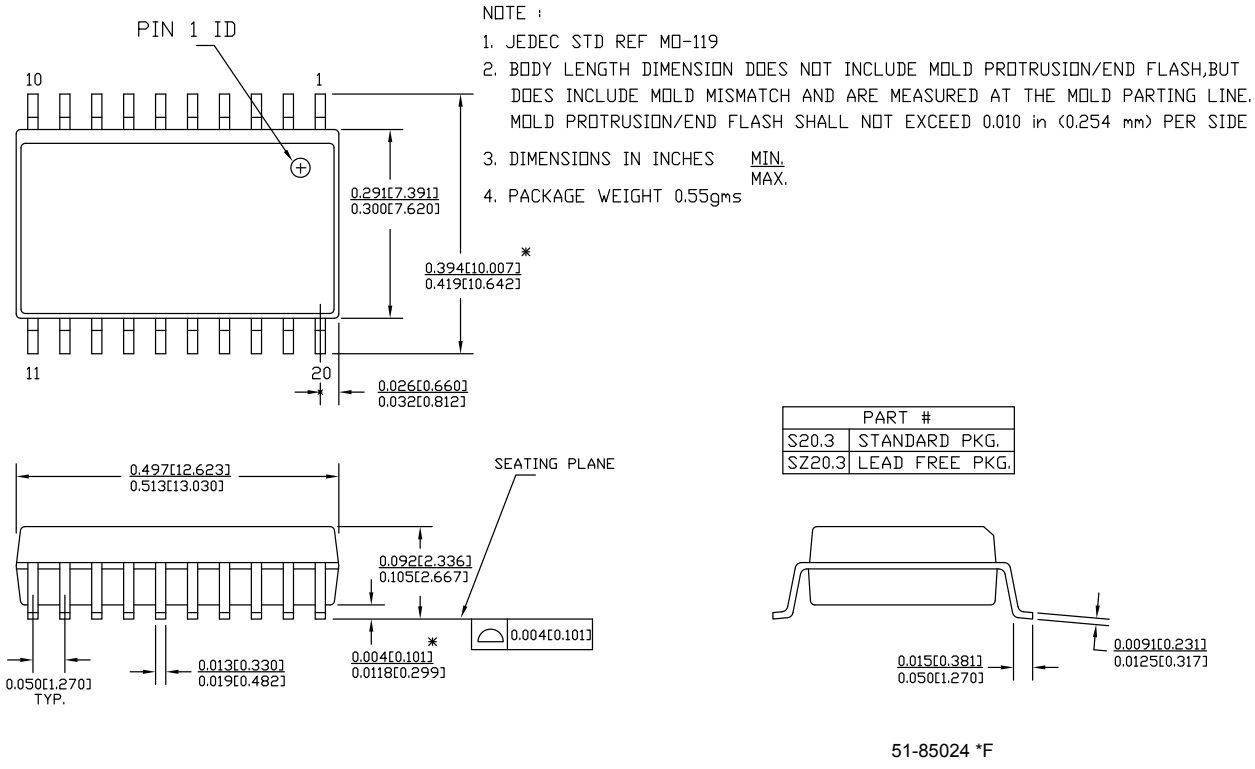


Figure 24. 28-Pin (300-Mil) Molded SOIC

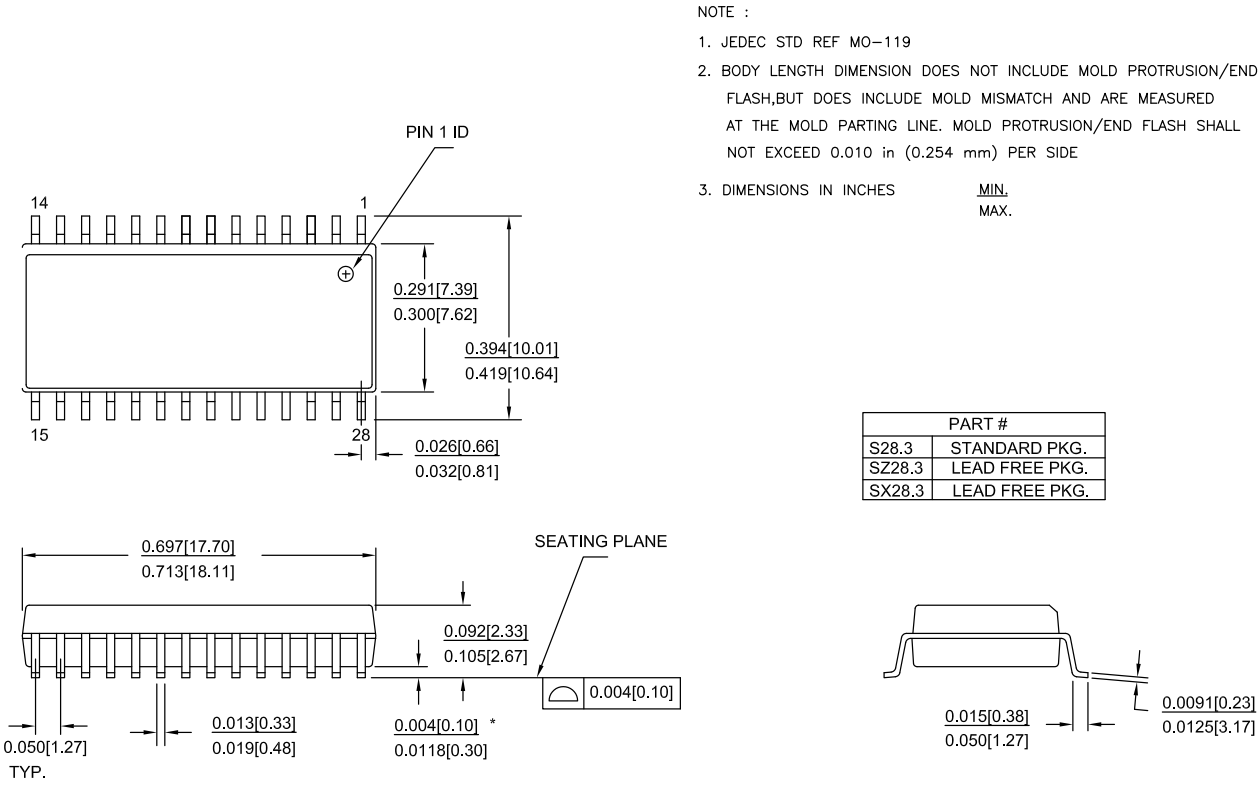
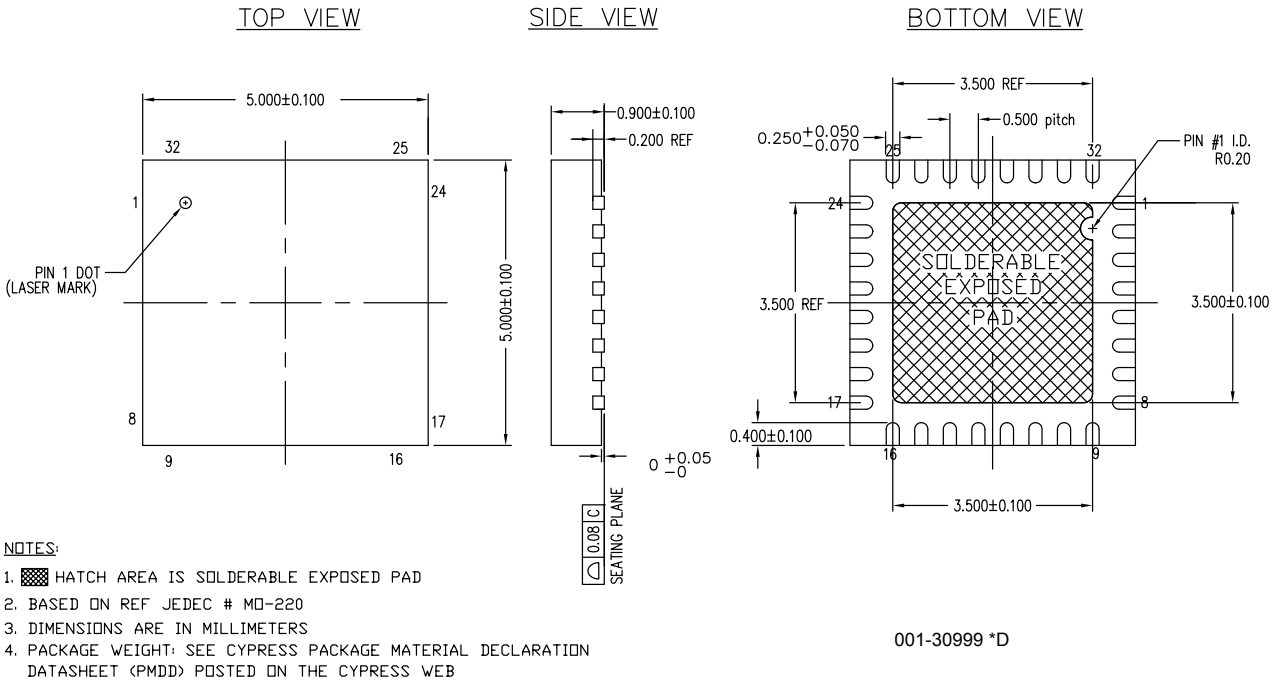
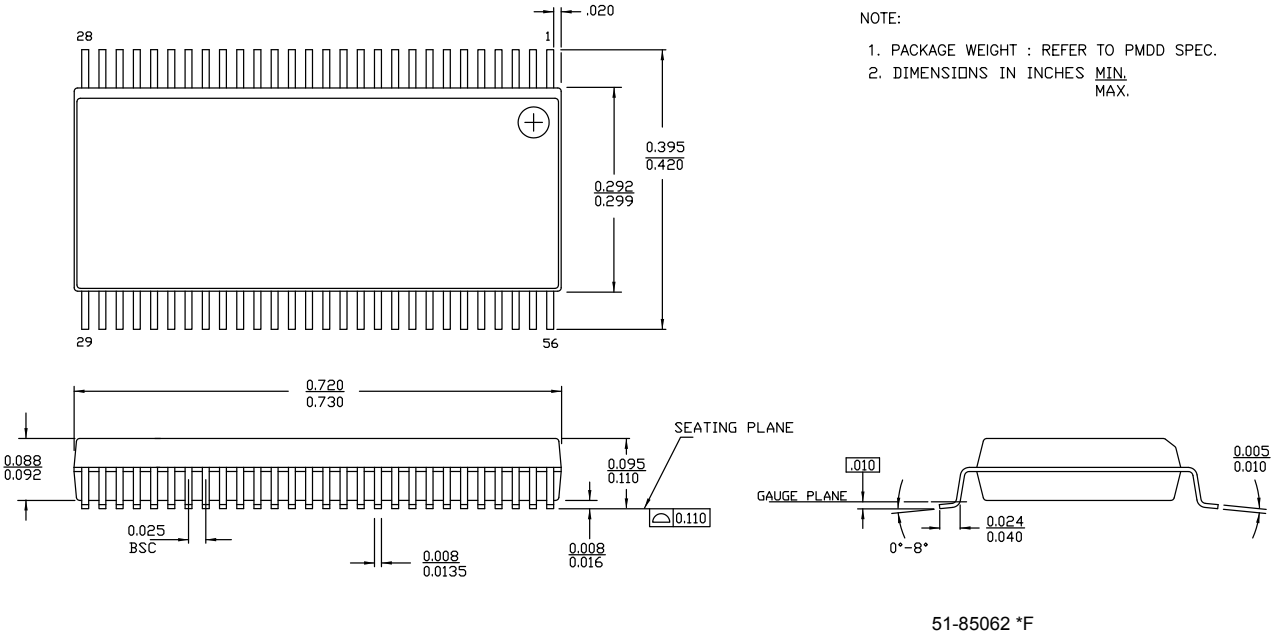


Figure 25. 32-Pin Sawn QFN Package



Important Note For information on the preferred dimensions for mounting QFN packages, see the application note, *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages* available at http://www.amkor.com.

Figure 26. 56-Pin (300-Mil) SSOP



Thermal Impedances

Table 48. Thermal Impedances per Package

Package	Typical θ_{JA}[38]
8-pin PDIP	123 °C/W
8-pin SOIC	185 °C/W
20-pin PDIP	109 °C/W
20-pin SSOP	117 °C/W
20-pin SOIC	81 °C/W
28-pin PDIP	69 °C/W
28-pin SSOP	101 °C/W
28-pin SOIC	74 °C/W
32-pin QFN[39]	22 °C/W

Capacitance on Crystal Pins

Table 49. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
8-pin PDIP	2.8 pF
8-pin SOIC	2.0 pF
20-pin PDIP	3.0 pF
20-pin SSOP	2.6 pF
20-pin SOIC	2.5 pF
28-pin PDIP	3.5 pF
28-pin SSOP	2.8 pF
28-pin SOIC	2.7 pF
32-pin QFN	2.0 pF

Solder Reflow Specifications

Table 50 shows the solder reflow temperature limits that must not be exceeded.

Table 50. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
8-pin PDIP	260 °C	30 seconds
8-pin SOIC	260 °C	30 seconds
20-pin PDIP	260 °C	30 seconds
20-pin SSOP	260 °C	30 seconds
20-pin SOIC	260 °C	30 seconds
28-pin PDIP	260 °C	30 seconds
28-pin SSOP	260 °C	30 seconds
28-pin SOIC	260 °C	30 seconds
32-pin QFN	260 °C	30 seconds

Notes
38. $T_J = T_A + \text{Power} \times \theta_{JA}$
39. To achieve the thermal impedance specified for the QFN package, refer to *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages* available at www.amkor.com.

Ordering Information

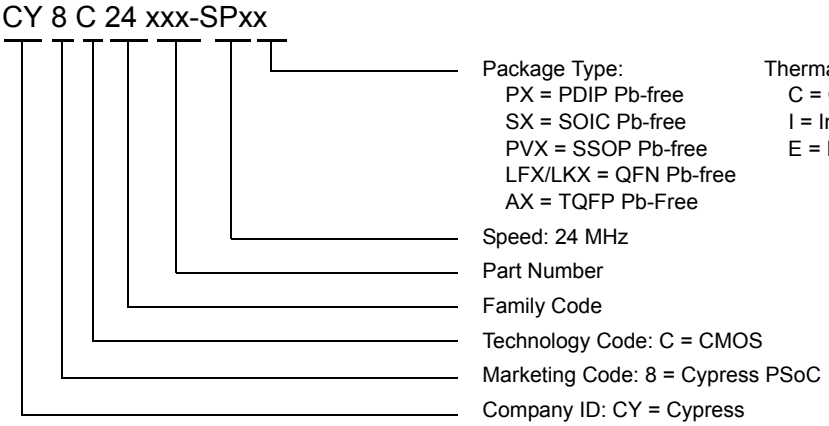
The following table lists the CY8C24x23A PSoC device's key package features and ordering codes.

Table 52. CY8C24x23A PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Switch Mode Pump	Temperature Range	Digital Blocks	Analog Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
8-pin (300-mil) DIP	CY8C24123A-24PXI	4 K	256	No	–40 °C to +85 °C	4	6	6	4	2	No
8-pin (150-mil) SOIC	CY8C24123A-24SXI	4 K	256	No	–40 °C to +85 °C	4	6	6	4	2	No
8-pin (150-mil) SOIC (Tape and Reel)	CY8C24123A-24SXIT	4 K	256	No	–40 °C to +85 °C	4	6	6	4	2	No
20-pin (300-mil) DIP	CY8C24223A-24PXI	4 K	256	Yes	–40 °C to +85 °C	4	6	16	8	2	Yes
20-pin (210-mil) SSOP	CY8C24223A-24PVXI	4 K	256	Yes	–40 °C to +85 °C	4	6	16	8	2	Yes
20-pin (210-mil) SSOP (Tape and Reel)	CY8C24223A-24PVXIT	4 K	256	Yes	–40 °C to +85 °C	4	6	16	8	2	Yes
20-pin (300-mil) SOIC	CY8C24223A-24SXI	4 K	256	Yes	–40 °C to +85 °C	4	6	16	8	2	Yes
20-pin (300-mil) SOIC (Tape and Reel)	CY8C24223A-24SXIT	4 K	256	Yes	–40 °C to +85 °C	4	6	16	8	2	Yes
28-pin (300-mil) DIP	CY8C24423A-24PXI	4 K	256	Yes	–40 °C to +85 °C	4	6	24	10	2	Yes
28-pin (210-mil) SSOP	CY8C24423A-24PVXI	4 K	256	Yes	–40 °C to +85 °C	4	6	24	10	2	Yes
28-pin (210-mil) SSOP (Tape and Reel)	CY8C24423A-24PVXIT	4 K	256	Yes	–40 °C to +85 °C	4	6	24	10	2	Yes
28-pin (300-mil) SOIC	CY8C24423A-24SXI	4 K	256	Yes	–40 °C to +85 °C	4	6	24	10	2	Yes
28-pin (300-mil) SOIC (Tape and Reel)	CY8C24423A-24SXIT	4 K	256	Yes	–40 °C to +85 °C	4	6	24	10	2	Yes
32-pin (5 × 5 mm 1.00 max) Sawn QFN	CY8C24423A-24LTXI	4 K	256	Yes	–40 °C to +85 °C	4	6	24	10	2	Yes
32-pin (5 × 5 mm 1.00 max) Sawn QFN (Tape and Reel)	CY8C24423A-24LTXIT	4 K	256	Yes	–40 °C to +85 °C	4	6	24	10	2	Yes
56-pin OCD SSOP	CY8C24000A-24PVXI[43]	4 K	256	Yes	–40 °C to +85 °C	4	6	24	10	2	Yes

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions



Note
43. This part may be used for in-circuit debugging. It is NOT available for production.

Errata

This section describes the errata for the CY8C24xxxA device family. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Ordering Information
CY8C24123A	CY8C24123A-24PXI
	CY8C24123A-24SXI
	CY8C24123A-24SXIT
	CY8C24223A-24PXI
	CY8C24223A-24PVXI
	CY8C24223A-24PVXIT
	CY8C24223A-24SXI
	CY8C24223A-24SXIT
	CY8C24423A-24PXI
	CY8C24423A-24PVXI
	CY8C24423A-24PVXIT
	CY8C24423A-24SXI
	CY8C24423A-24SXIT
	CY8C24423A-24LFXI
	CY8C24423A-24LTXI
	CY8C24423A-24LTXIT
	CY8C24000A-24PVXI

CY8C24123A Qualification Status

Product Status: Production

CY8C24123A Errata Summary

The following table defines the errata applicability to available CY8C24123A family devices.

Items	Part Number	Silicon Revision	Fix Status
[1.]. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes	CY8C24123A	*A	No silicon fix planned. Workaround is required.

1. **Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes**
   - **Problem Definition**
     Asynchronous Digital Communications Interfaces may fail framing beyond 0 to 70 °C. This problem does not affect end-product usage between 0 and 70 °C.
   - **Parameters Affected**
     The IMO frequency tolerance. The worst case deviation when operated below 0°C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.
   - **Trigger Condition(S)**
     The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the data sheet limit of ±2.5% when operated beyond the temperature range of 0 to +70 °C.
   - **Scope of Impact**
     This problem may affect UART, IrDA, and FSK implementations.
   - **Workaround**
     Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.
   - **Fix Status**
     Silicon fix is not planned. The workaround mentioned above should be used.

Document History Page

Document Title: CY8C24123A/CY8C24223A/CY8C24423A, PSoC® Programmable System-on-Chip Document Number: 38-12028				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	236409	SFV	See ECN	New silicon and new document – Preliminary datasheet.
*A	247589	SFV	See ECN	Changed the title to read “Final” datasheet. Updated Electrical Specifications chapter.
*B	261711	HMT	See ECN	Input all SFV memo changes. Updated Electrical Specifications chapter.
*C	279731	HMT	See ECN	Update Electrical Specifications chapter, including 2.7 VIL DC GPIO spec. Add Solder Reflow Peak Temperature table. Clean up pinouts and fine tune wording and format throughout.
*D	352614	HMT	See ECN	Add new color and CY logo. Add URL to preferred dimensions for mounting MLF packages. Update Transmitter and Receiver AC Digital Block Electrical Specifications. Re-add ISSP pinout identifier. Delete Electrical Specification sentence re: devices running at greater than 12 MHz. Update Solder Reflow Peak Temperature table. Fix CY.com URLs. Update CY copyright.
*E	424036	HMT	See ECN	Fix SMP 8-pin SOIC error in Feature and Order table. Update 32-pin QFN E-Pad dimensions and rev. *A. Add ISSP note to pinout tables. Update typical and recommended Storage Temperature per industrial specs. Add OCD non-production pinout and package diagram. Update CY branding and QFN convention. Update package diagram revisions.
*F	521439	HMT	See ECN	Add Low Power Comparator (LPC) AC/DC electrical spec. tables. Add new Dev. Tool section. Add CY8C20x34 to PSoC Device Characteristics table.
*G	2256806	UVS / PYRS	See ECN	Added Sawn pin information.
*H	2425586	DSO / AESA	See ECN	Corrected Ordering Information to include CY8C24423A-24LTXI and CY8C24423A-24LTXIT
*I	2619935	OGNE / AESA	12/11/2008	Changed title to “CY8C24123A, CY8C24223A, CY8C24423A PSoC® Programmable System-on-Chip™” Updated package diagram 001-30999 to *A. Added note on digital signaling in DC Analog Reference Specifications on page 28. Added Die Sales information note to Ordering Information on page 60.
*J	2692871	DPT / PYRS	04/16/2009	Updated Max package thickness for 32-pin QFN package Formatted Notes Updated “Getting Started” on page 7 Updated “Development Tools” on page 8 and “Designing with PSoC Designer” on page 9
*K	2762168	JVY / AESA	06/25/2009	Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: Modified FIMO6 and TWRITE specifications. Replaced T_{RAMP} (time) specification with SR_{POWER_UP} (slew rate) specification. Added note [9] to Flash Endurance specification. Added IOH, IOL, DC_{ILO}, F_{32K_U}, $T_{POWERUP}$, $T_{ERASEALL}$, $T_{PROGRAM\_HOT}$, and $T_{PROGRAM\_COLD}$ specifications.