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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	6
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SO
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc901fd-112

3. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
P89LPC901FD	SO8	plastic small outline package; 8 leads; body width 7.5 mm	SOT96-1
P89LPC902FD			
P89LPC903FD			
P89LPC901FN	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
P89LPC902FN			

3.1 Ordering options

Table 2: Part options

Type number	Temperature range	Frequency
P89LPC901xx	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC902xx		Internal RC or watchdog
P89LPC903xx		Internal RC or watchdog

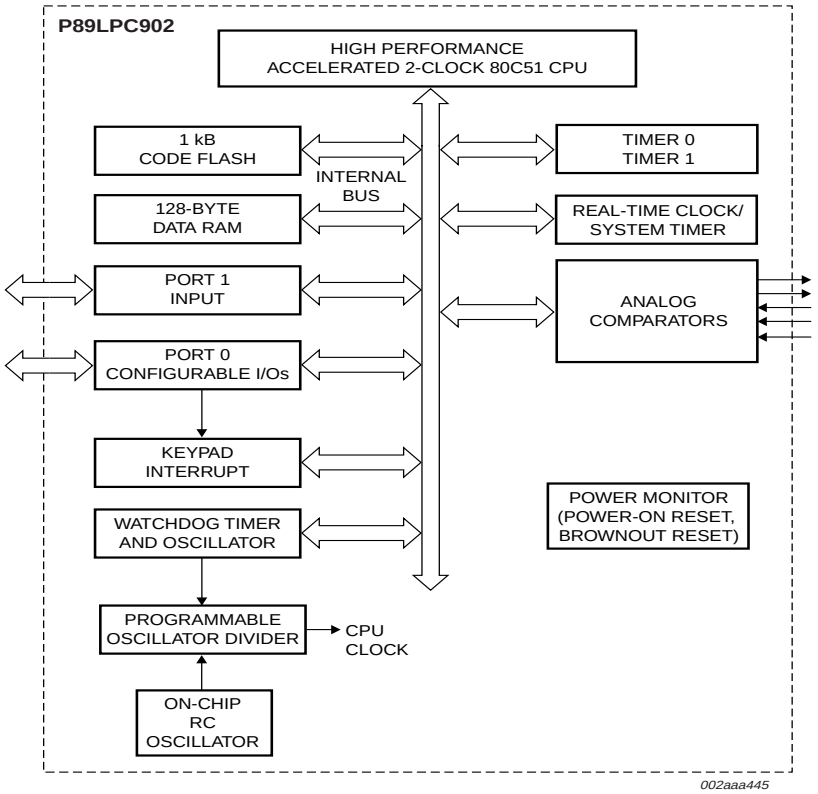


Fig 2. P89LPC902 block diagram.

Table 3: P89LPC901 pin description...*continued*

Symbol	Pin	Type	Description
P1.0 to P1.5			**Port 1:** Port 1 is an I/O port with a user-configurable output type. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.12.1 “Port configurations” and Table 13 “DC electrical characteristics” for details. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
	5	I/O	**P1.2 —** Port 1 bit 2.
		O	**T0 —** Timer/counter 0 external count input or overflow output.
	4	I	**P1.5 —** Port 1 bit 5 (input only).
		I	**$\overline{\text{RST}}$ —** External Reset input during Power-on or if selected via UCFG1. When functioning as a reset input a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.** Also used during a power-on sequence to force In-System Programming mode.
P3.0 to P3.1		I/O	**Port 3:** Port 3 is an I/O port with a user-configurable output types. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 “Port configurations” and Table 13 “DC electrical characteristics” for details. All pins have Schmitt triggered inputs. Port 3 also provides various special functions as described below:
	3	I/O	**P3.0 —** Port 3 bit 0.
		O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the FLASH configuration).
		O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK to TRIM.6). It can be used if the CPU clock is the internal RC oscillator, Watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the real time clock/system timer.
	2	I/O	**P3.1 —** Port 3 bit 1.
		I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the FLASH configuration). It can be a port pin if internal RC oscillator or Watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the real time clock/system timer.
V_{SS}	8	I	**Ground:** 0 V reference.
V_{DD}	1	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

Table 5: P89LPC903 pin description

Symbol	Pin	Type	Description
P0.0 to P0.6		I/O	**Port 0:** Port 0 is an I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 “Port configurations” and Table 13 “DC electrical characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
	2	I/O	**P0.2 —** Port 0 bit 2.
		I	**CIN2A —** Comparator 2 positive input.
		I	**KBI2 —** Keyboard input 2.
	7	I/O	**P0.4 —** Port 0 bit 4.
		I	**CIN1A —** Comparator 1 positive input.
		I	**KBI4 —** Keyboard input 4.
	6	I/O	**P0.5 —** Port 0 bit 5.
		I	**CMPREF —** Comparator reference (negative) input.
		I	**KBI5 —** Keyboard input 5.
P1.0 to P1.5			**Port 1:** Port 1 is an I/O port with a user-configurable output type. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.12.1 “Port configurations” and Table 13 “DC electrical characteristics” for details. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
	5	I/O	**P1.0 —** Port 1 bit 0.
		O	**TxD —** Serial port transmitter data.
	3	I/O	**P1.1 —** Port 1 bit 1.
		I	**RxD —** Serial port receiver data.
	4	I	**P1.5 —** Port 1 bit 5 (input only).
		I	**$\overline{\text{RST}}$ —** External Reset input during Power-on or if selected via UCFG1. When functioning as a reset input a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force In-System Programming mode.
V_{SS}	8	I	**Ground:** 0 V reference.
V_{DD}	1	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

6. Logic symbols

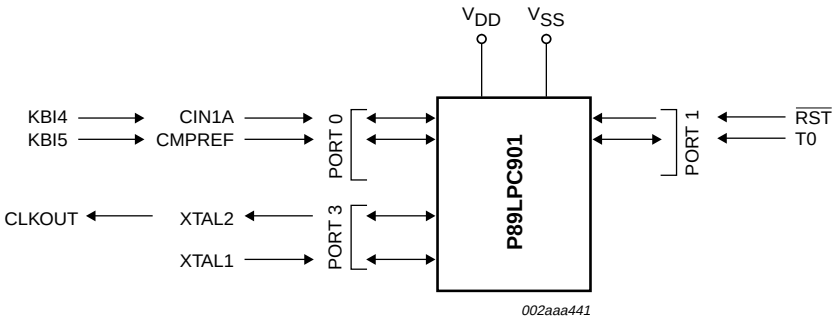


Fig 9. P89LPC901 logic symbol.

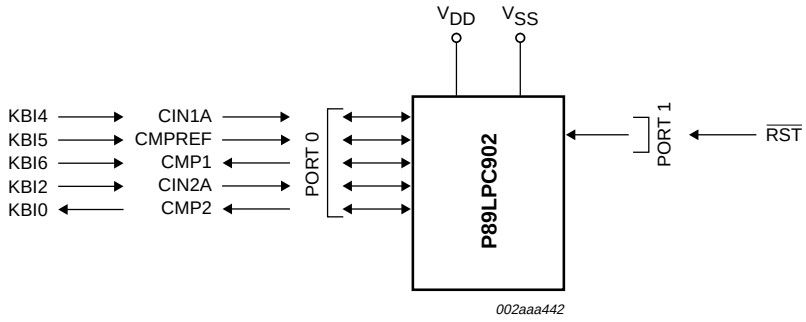


Fig 10. P89LPC902 logic symbol.

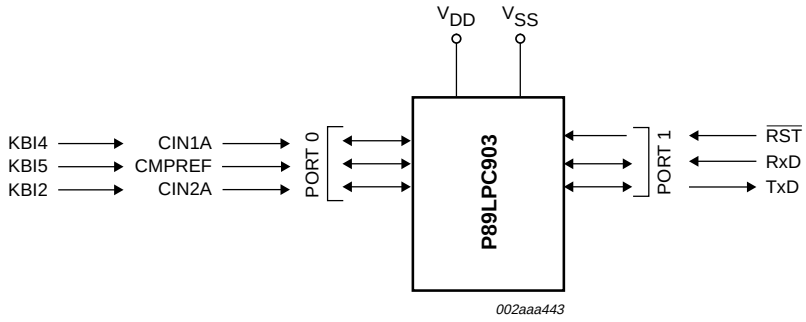


Fig 11. P89LPC903 logic symbol.

Table 7: P89LPC901 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	8F	8E	8D	8C	8B	8A	89	88		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	-	-	-	-	00	00000000
TH0	Timer 0 high	8CH									00	00000000
TH1	Timer 1 high	8DH									00	00000000
TL0	Timer 0 low	8AH									00	00000000
TL1	Timer 1 low	8BH									00	00000000
TMOD	Timer 0 and 1 mode	89H	-	-	T1M1	T1M0	-	-	T0M1	T0M0	00	00000000
TRIM	Internal oscillator trim register	96H	-	-	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[5] [6]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[4] [6]	
WDL	Watchdog load	C1H									FF	11111111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] All ports are in input only (high impedance) state after power-up.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is '0'. If any are written while BRGEN = 1, the result is unpredictable.

Unimplemented bits in SFRs (labeled '-') are X (unknown) at all times. Unless otherwise specified, ones should not be written to these bits since they may be used for other purposes in future derivatives. The reset values shown for these bits are '0's although they are unknown when read.

[3] The RSTSRC register reflects the cause of the P89LPC901/902/903 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx110000.

[4] After reset, the value is 111001x1, i.e., PRE2-PRE0 are all '1', WDRUN = 1 and WDCLK = 1. WDTOF bit is '1' after Watchdog reset and is '0' after power-on reset. Other resets will not affect WDTOF.

[5] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6] The only reset source that affects these SFRs is power-on reset.

Table 8: P89LPC902 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00[1]	xxxxxx00
KBMASK	Keypad interrupt mask register	86H									00	00000000
KBPATN	Keypad pattern register	93H									FF	11111111
	Bit address		**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**		
P0*	Port 0	80H	-	CMP1 /KB6	CMPREF /KB5	CIN1A /KB4	-	KB2	-	KB0	[1]	
	Bit address		**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P1*	Port 1	90H	-	-	$\overline{\text{RST}}$	-	-	-	-	-		
	Bit address		**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
P0M1	Port 0 output mode 1	84H	-	(P0M1.6)	(P0M1.5)	(P0M1.4)	-	(P0M1.2)	-	(P0M1.0)	FF	11111111
P0M2	Port 0 output mode 2	85H	-	(P0M2.6)	(P0M2.5)	(P0M2.4)	-	(P0M2.2)	-	(P0M2.0)	00	00000000
P1M1	Port 1 output mode 1	91H	-	-	(P1M1.5)	-	-	-	-	-	FF[1]	11111111
P1M2	Port 1 output mode 2	92H	-	-	(P1M2.5)	-	-	-	-	-	00[1]	00000000
PCON	Power control register	87H	-	-	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	00000000
PCONA	Power control register A	B5H	RTCPD		VCPD			-	-		00[1]	00000000
PCONB	reserved for Power Control Register B	B6H	-	-	-	-	-	-	-	-	00[1]	xxxxxxxx
	Bit address		**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	00000000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	-	PT0AD.2	-	-	00	xx00000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	-	R_WD	R_SF	R_EX	[3]	
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[1] [6]	011xxx00
RTCH	Real-time clock register high	D2H									00[6]	00000000
RTCL	Real-time clock register low	D3H									00[6]	00000000
SP	Stack pointer	81H									07	00000111

Table 9: P89LPC903 Special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	00000000
AUXR1	Auxiliary function register	A2H	-	EBRR	-	-	SRST	0	-	DPS	00[1]	000000x0
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	00000000
BRGR0[2]	Baud rate generator rate low	BEH									00	00000000
BRGR1[2]	Baud rate generator rate high	BFH									00	00000000
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00[6]	xxxxxx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	-	CN1	-	CO1	CMF1	00[1]	xx000000
CMP2	Comparator 2 control register	ADH	-	-	CE2	-	CN2	-	CO2	CMF2	00[1]	xx000000
DIVM	CPU clock divide-by-M control	95H									00	00000000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	00000000
DPL	Data pointer low	82H									00	00000000
FMADRH	Program Flash address high	E7H									00	00000000
FMADRL	Program Flash address low	E6H									00	00000000
FMCON	Program Flash Control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	01110000
	Program Flash Control (Write)		FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program Flash data	E5H									00	00000000
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	-	ET0	-	00	00000000
		Bit address	EF	EE	ED	EC	EB	EA	E9	E8		
IEN1*	Interrupt enable 1	E8H	-	EST	-	-	-	EC	EKBI	-	00[1]	00x00000
		Bit address	BF	BE	BD	BC	BB	BA	B9	B8		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	-	PT0	-	00[1]	x0000000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/PSRH	PT1H	-	PT0H	-	00[1]	x0000000
		Bit address	FF	FE	FD	FC	FB	FA	F9	F8		

9397 750 14465

8. Functional description

Remark: Please refer to the *P89LPC901/902/903 User's Manual* for a more detailed functional description.

8.1 Enhanced CPU

The P89LPC901/902/903 uses an enhanced 80C51 CPU which runs at 6 times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

8.2 Clocks

8.2.1 Clock definitions

The P89LPC901/902/903 device has several internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of the clock sources (see Figure 12, 13, and 14) and can also be optionally divided to a slower frequency (see Section 8.7 "CPU CLOCK (CCLK) modification: DIVM register").

Note: f_{osc} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output.

PCLK — Clock for the various peripheral devices and is CCLK/2

8.2.2 CPU clock (OSCCLK)

The P89LPC901/902/903 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the FLASH is programmed and include an on-chip Watchdog oscillator and an on-chip RC oscillator.

The P89LPC901, in addition, includes an option for an oscillator using an external crystal or an external clock source. The crystal oscillator can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 12 MHz.

8.2.3 Low speed oscillator option (P89LPC901)

This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

8.2.4 Medium speed oscillator option (P89LPC901)

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

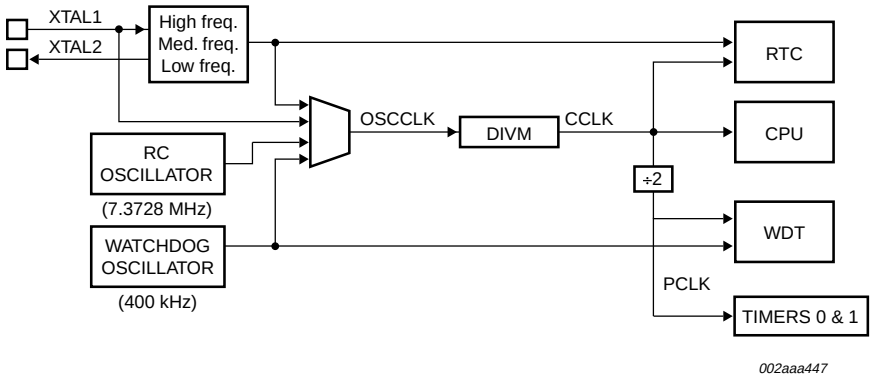


Fig 12. Block diagram of oscillator control (P89LPC901).

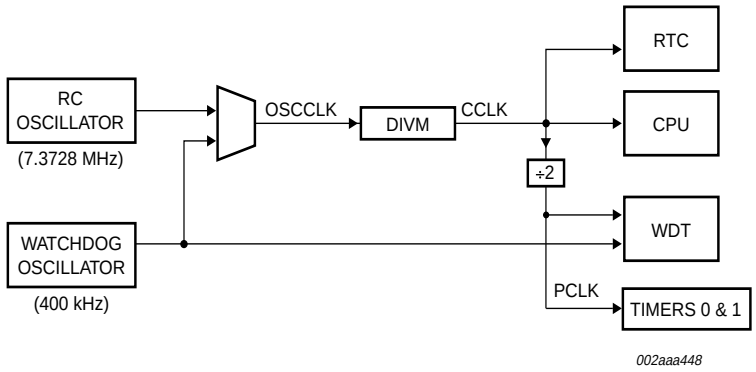


Fig 13. Block diagram of oscillator control (P89LPC902).

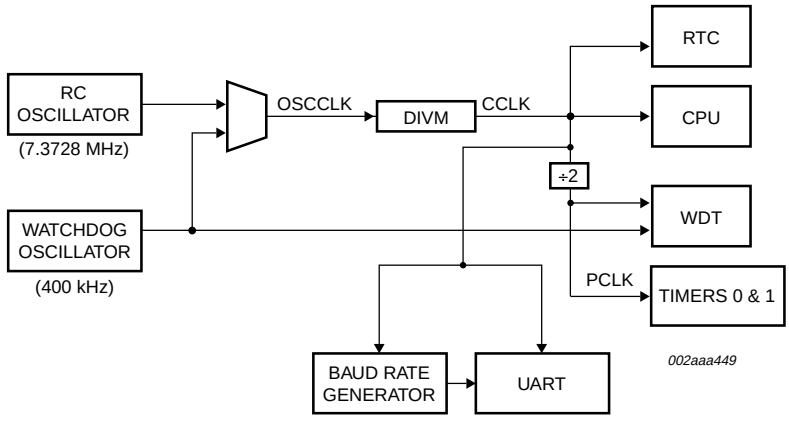


Fig 14. Block diagram of oscillator control (P89LPC903).

8.6 CPU CLock (CCLK) wake-up delay

The P89LPC901/902/903 has an internal wake-up timer that delays the clock until it stabilizes depending to the clock source used. If the clock source is any of the three crystal selections (P89LPC901) the delay is 992 OSCCLK cycles plus 60 to 100 µs.

8.7 CPU CLOCK (CCLK) modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

8.8 Low power select

The P89LPC901 is designed to run at 18 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to ‘1’ to lower the power consumption further. On any reset, CLKLP is ‘0’ allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

8.9 Memory organization

The various P89LPC901/902/903 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00h:7Fh) accessed via direct or indirect addressing, using instruction other than MOVX and MOVC. All or part of the Stack may be in this area.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC901/902/903 has 1 kB of on-chip Code memory.

8.10 Data RAM arrangement

The 128 bytes of on-chip RAM is organized as follows:

Table 10: On-chip data memory usages

Type	Data RAM	Size (Bytes)
DATA	Memory that can be addressed directly and indirectly	128

8.11 Interrupts

The P89LPC901/902/903 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources.

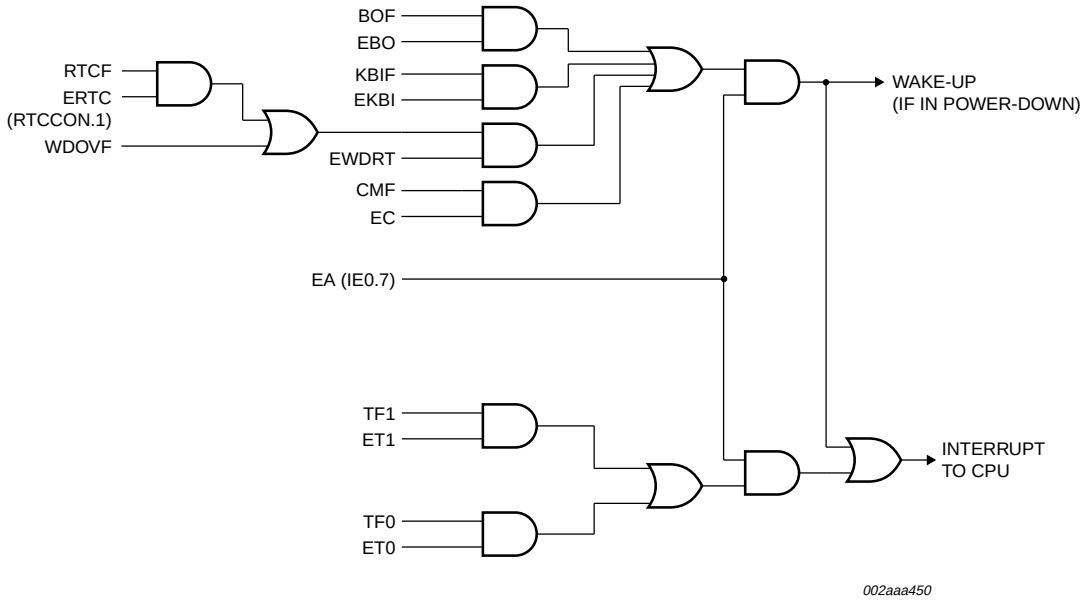


Fig 15. Interrupt sources, interrupt enables, and power-down wake-up sources (P89LPC901).

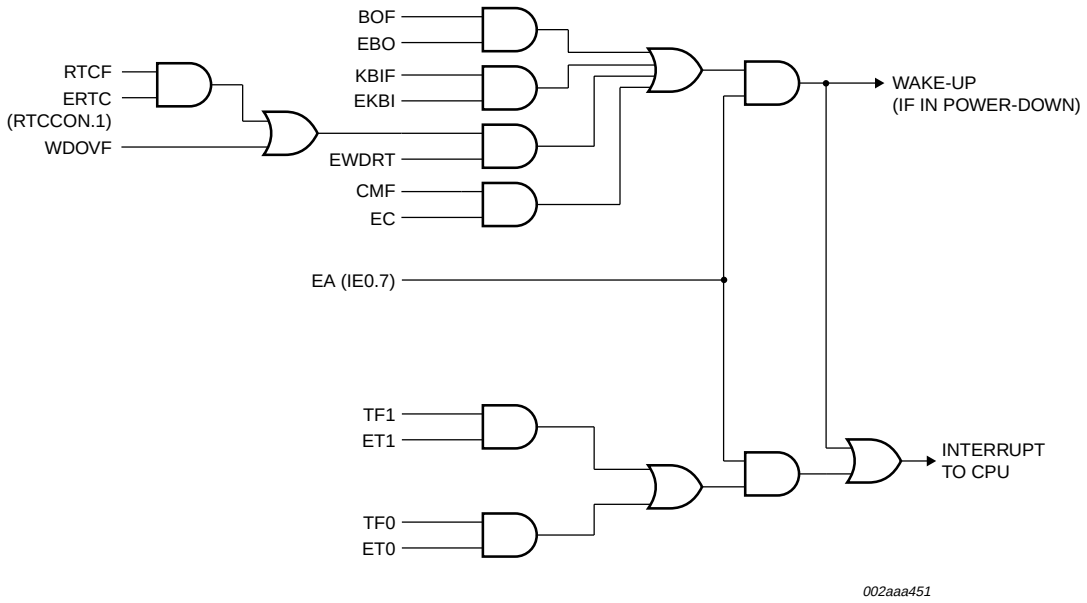


Fig 16. Interrupt sources, interrupt enables, and power-down wake-up sources (P89LPC902).

8.16.6 Timer overflow toggle output (P89LPC901)

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

8.17 Real-Time clock/system timer

The P89LPC901/902/903 has a simple Real-Time clock that allows a user to continue running an accurate timer while the rest of the device is powered-down. The Real-Time clock can be a wake-up or an interrupt source. The Real-Time clock is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all ‘0’s, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator, provided that the XTAL oscillator is not being used as the CPU clock. If the XTAL oscillator is used as the CPU clock, then the RTC will use CCLK as its clock source. Only power-on reset will reset the Real-Time clock and its associated SFRs to the default state.

8.18 UART (P89LPC903)

The P89LPC903 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC903 does include an independent Baud Rate Generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in 4 modes: shift register, 8-bit UART, 9-bit UART, and CPU clock/32 or CPU clock/16.

8.18.1 Mode 0

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $\frac{1}{16}$ of the CPU clock frequency.

8.18.2 Mode 1

10 bits are transmitted (through TxD) or received (through RxD): a start bit (logical ‘0’), 8 data bits (LSB first), and a stop bit (logical ‘1’). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in Section 8.18.5 “Baud rate generator and selection”).

8.18.3 Mode 2

11 bits are transmitted (through TxD) or received (through RxD): start bit (logical ‘0’), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical ‘1’). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of ‘0’ or ‘1’. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is not saved. The baud rate is programmable to either $\frac{1}{16}$ or $\frac{1}{32}$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

8.18.9 Transmit interrupts with double buffering enabled (Modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the Tx interrupt is generated when the double buffer is ready to receive new data.

8.18.10 The 9th bit (bit 8) in double buffering (Modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the Tx interrupt.

If double buffering is enabled, TB8 **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

8.19 Analog comparators

One analog comparator is provided on the P89LPC901. Two analog comparators are provided on the P89LPC902 and P89LPC903 devices. Comparator operation is such that the output is a logical one (which may be read in a register) when the positive input is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. The comparator may be configured to cause an interrupt when the output value changes.

The connections to the comparator are shown in Figure 19. **Note:** Not all possible comparator configurations are available on all three devices. Please refer to the Logic diagrams in Section 6 “Logic symbols” on page 12. The comparator functions to V_{DD} = 2.4 V.

When the comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 microseconds. The comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

When a comparator is disabled the comparator’s output, COx, goes HIGH. If the comparator output was LOW and then is disabled, the resulting transition of the comparator output from a LOW to HIGH state will set the comparator flag, CMFx. This will cause an interrupt if the comparator interrupt is enabled. The user should therefore disable the comparator interrupt prior to disabling the comparator. Additionally, the user should clear the comparator flag, CMFx, after disabling the comparator.

designed to optimize the erase and programming mechanisms. The P89LPC901/902/903 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms.

8.26.2 Features

- Programming and erase over the full operating voltage range.
- Byte-erase allowing code memory to be used for data storage.
- Read/Programming/Erase using ICP.
- Any flash program/erase operation in 2 ms.
- Programming with industry-standard commercial programmers.
- Programmable security for the code in the Flash for each sector.
- More than 100,000 minimum erase/program cycles for each byte.
- 10-year minimum data retention.

8.26.3 Flash organization

The P89LPC901/902/903 program memory consists of four 256 byte sectors. Each sector can be further divided into 16-byte pages. In addition to sector erase, page erase, and byte erase, a 16-byte page register is included which allows from 1 to 16 bytes of a given page to be programmed at the same time, substantially reducing overall programming time. In addition, erasing and reprogramming of user-programmable configuration bytes including UCFG1, the Boot Status Bit, and the Boot Vector is supported.

8.26.4 Flash programming and erasing

Different methods of erasing or programming of the Flash are available. The Flash may be programmed or erased in the end-user application (IAP) under control of the application's firmware. Another option is to use the In-Circuit Programming (ICP) mechanism. This ICP system provides for programming through a serial clock- serial data interface. Third, the Flash may be programmed or erased using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead this device provides a 32-bit CRC result on either a sector or the entire 1 KB of user code space.

8.26.5 In-circuit programming (ICP)

In-Circuit Programming is performed without removing the microcontroller from the system. The In-Circuit Programming facility consists of internal hardware resources to facilitate remote programming of the P89LPC901/902/903 through a two-wire serial interface. The Philips In-Circuit Programming facility has made in-circuit programming in an embedded application, using commercially available programmers, possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the *P89LPC901/902/903 User's Manual*.

10. Static characteristics

Table 13: DC electrical characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(oper)}$	power supply current, operating (P89LPC901)	3.6 V; 12 MHz	[2]	-	11	18	mA
		3.6 V; 18 MHz	[2]	-	14	23	mA
$I_{DD(idle)}$	power supply current, Idle mode (P89LPC901)	3.6 V; 12 MHz	[2]	-	1	4	mA
		3.6 V; 18 MHz	[2]	-	1.5	5.6	mA
$I_{DD(oper)}$	power supply current, operating (P89LPC902, P89LPC903)	3.6 V; 7.373 MHz	[3]	-	4	8	mA
$I_{DD(idle)}$	power supply current, Idle mode (P89LPC902, P89LPC903)	3.6 V; 7.373 MHz	[3]	-	1	3	mA
$I_{DD(PD)}$	power supply current, Power-down mode, voltage comparators powered-down	3.6 V	[2][3]	-	-	70	µA
$I_{DD(TPD)}$	power supply current, total Power-down mode	3.6 V	[2][3]	-	1	5	µA
$(dV_{DD}/dt)_r$	V_{DD} rise rate			-	-	2	mV/µs
$(dV_{DD}/dt)_f$	V_{DD} fall rate			-	-	50	mV/µs
V_{POR}	Power-on reset detect voltage			-	-	0.2	V
V_{RAM}	RAM keep-alive voltage			1.5	-	-	V
$V_{th(HL)}$	negative-going threshold voltage (Schmitt trigger input)			$0.22V_{DD}$	$0.4V_{DD}$	-	V
$V_{th(LH)}$	positive-going threshold voltage (Schmitt trigger input)			-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{hys}	hysteresis voltage			-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage; all ports, all modes except Hi-Z	I_{OL} = 20 mA		-	0.6	1.0	V
		I_{OL} = 10 mA		-	0.3	0.5	V
		I_{OL} = 3.2 mA		-	0.2	0.3	V
V_{OH}	HIGH-level output voltage, all ports	I_{OH} = −8 mA; push-pull mode		V_{DD} − 1.0	-	-	V
		I_{OH} = −3.2 mA; push-pull mode		V_{DD} − 0.7	V_{DD} − 0.4	-	V
		I_{OH} = −20 µA; quasi-bidirectional mode		V_{DD} − 0.3	V_{DD} − 0.2	-	V
C_{ig}	input/output pin capacitance		[4]	-	-	15	pF
I_{IL}	logical 0 input current, all ports	V_{IN} = 0.4 V	[5]	-	-	−80	µA
I_{LI}	input leakage current, all ports	$V_{IN} = V_{IL}$ or V_{IH}	[6]	-	-	±10	µA
I_{TL}	logical 1-to-0 transition current, all ports	V_{IN} = 2.0 V at V_{DD} = 3.6 V	[7][8]	−30	-	−450	µA
R_{RST}	internal reset pull-up resistor			10	-	30	kΩ

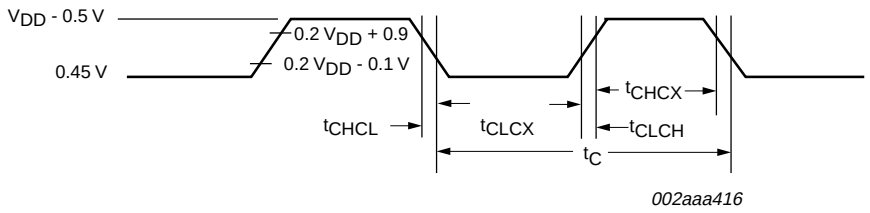


Fig 22. External clock timing.

12. Comparator electrical characteristics

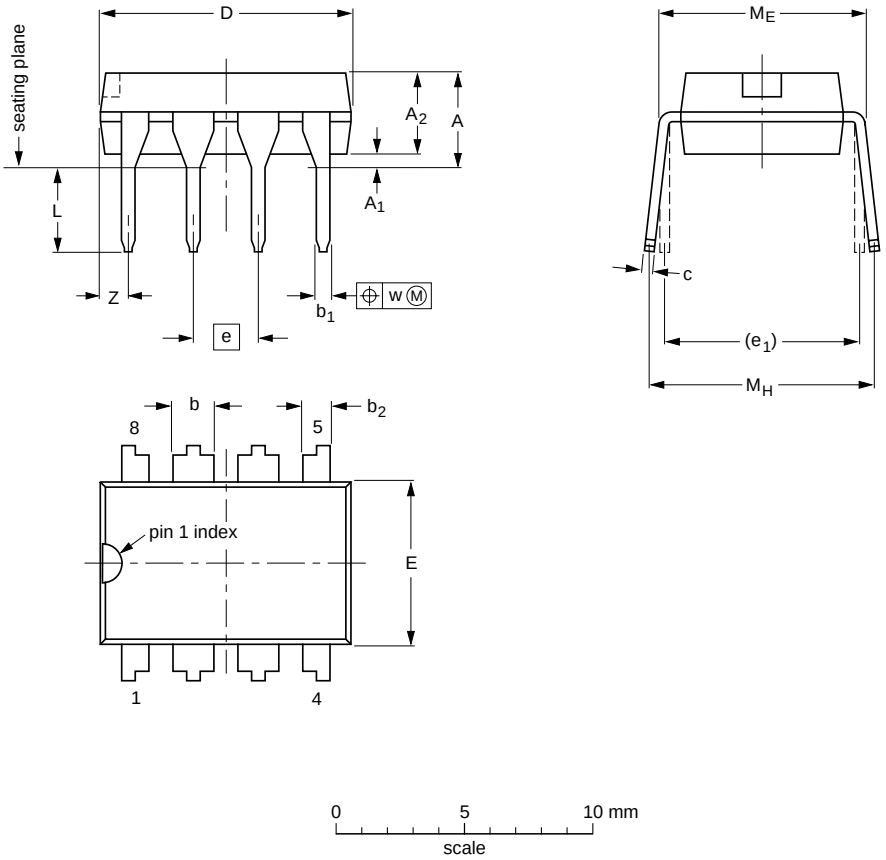
Table 16: Comparator electrical characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = –40 °C to +85 °C for industrial, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IO}	offset voltage comparator inputs			-	-	±20	mV
V_{CR}	common mode range comparator inputs			0	-	V_{DD} – 0.3	V
CMRR	common mode rejection ratio		[1]	-	-	–50	dB
	response time			-	250	500	ns
	comparator enable to output valid			-	-	10	µs
I_{IL}	input leakage current, comparator	$0 < V_{IN} < V_{DD}$		-	-	±10	µA

[1] This parameter is characterized, but not tested in production.

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.02	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT97-1	050G01	MO-001	SC-504-8			~~99-12-27~~ 03-02-13

Fig 24. SOT97-1 (DIP8).

15. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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9397 750 14465

Contents

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