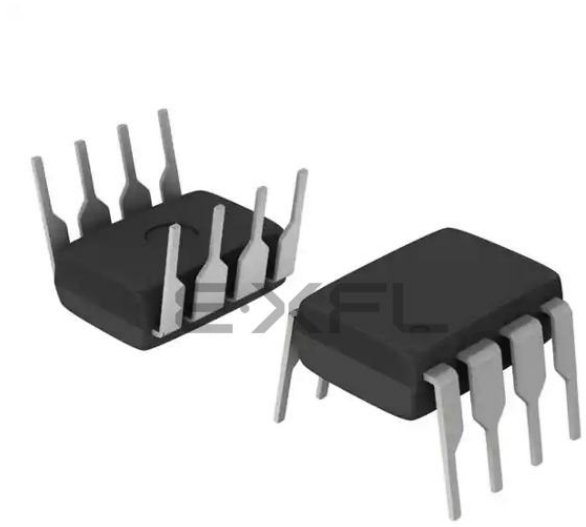


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	6
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-DIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc901fn-129

- Serial Flash In-Circuit Programming (ICP) allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog prescaler is selectable from 8 values.
- Low voltage reset (Brownout detect) allows a graceful system shutdown when power fails. May optionally be configured as an interrupt.
- Idle and two different Power-down reduced power modes. Improved wake-up from Power-down mode (a low interrupt input starts execution). Typical Power-down current is 1 μA (total Power-down with voltage comparators disabled).
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets. A software reset function is also available.
- Configurable on-chip oscillator with frequency range options selected by user programmed Flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz (P89LPC901).
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog prescaler is selectable from 8 values.
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.
- Port ‘input pattern match’ detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- LED drive capability (20 mA) on all port pins. A maximum limit is specified for the entire chip.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Only power and ground connections are required to operate the P89LPC901/902/903 when internal reset option is selected.
- Four interrupt priority levels.
- Two (P89LPC901), three (P89LPC903), or five (P89LPC902) keypad interrupt inputs.
- Second data pointer.
- Schmitt trigger port inputs.
- Emulation support.

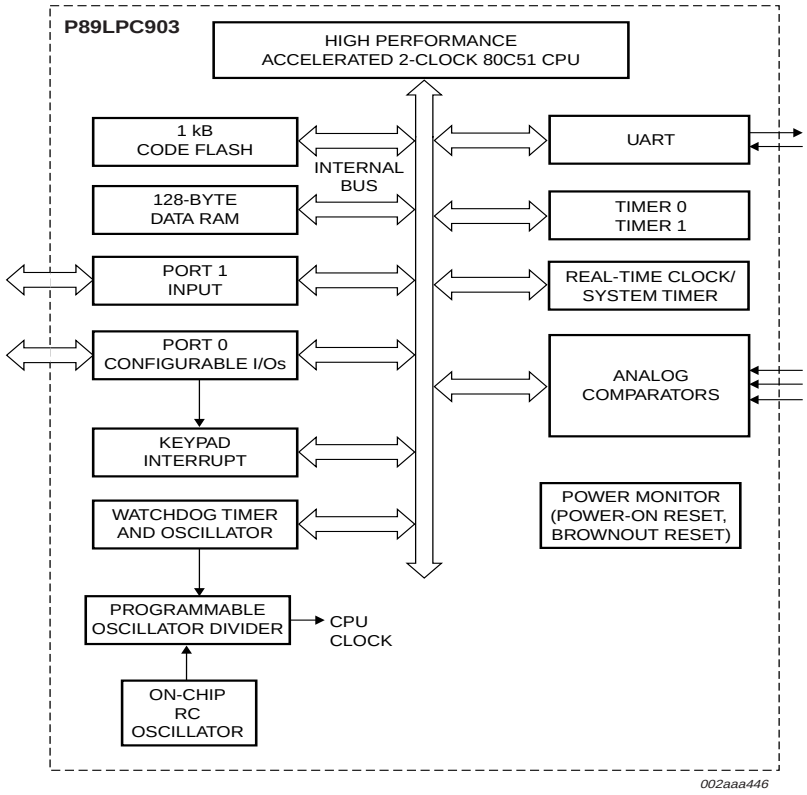


Fig 3. P89LPC903 block diagram.

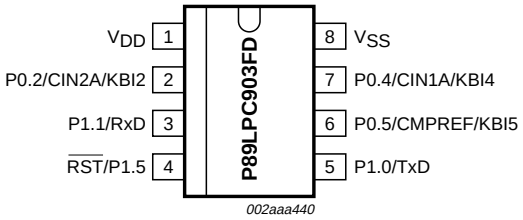


Fig 8. P89LPC903 pinning (SO8).

5.2 Pin description

Table 3: P89LPC901 pin description

Symbol	Pin	Type	Description
P0.0 to P0.6		I/O	**Port 0:** Port 0 is an I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "DC electrical characteristics" for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
	7	I/O	**P0.4 —** Port 0 bit 4.
		I	**CIN1A —** Comparator 1 positive input.
		I	**KBI4 —** Keyboard input 4.
	6	I/O	**P0.5 —** Port 0 bit 5.
		I	**CMPREF —** Comparator reference (negative) input.
		I	**KBI5 —** Keyboard input 5.

Table 7: P89LPC901 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
KBMASK	Keypad interrupt mask register	86H									00	00000000
KBPATN	Keypad pattern register	93H									FF	11111111
		Bit address	87	86	85	84	83	82	81	80		
P0*	Port 0	80H	-	-	CMPREF /KB5	CIN1A /KB4	-	-	-	-	[1]	
		Bit address	97	96	95	94	93	92	91	90		
P1*	Port 1	90H	-	-	$\overline{\text{RST}}$	-	-	T0	-	-	[1]	
		Bit address	B7	B6	B5	B4	B3	B2	B1	B0		
P3*	Port 3	B0H	-	-	-	-	-	-	XTAL1	XTAL2	[1]	
P0M1	Port 0 output mode 1	84H	-	-	(P0M1.5)	(P0M1.4)	-	-	-	-	FF	11111111
P0M2	Port 0 output mode 2	85H	-	-	(P0M2.5)	(P0M2.4)	-	-	-	-	00	00000000
P1M1	Port 1 output mode 1	91H	-	-	(P1M1.5)	-	-	(P1M1.2)	-	-	FF[1]	11111111
P1M2	Port 1 output mode 2	92H	-	-	(P1M2.5)	-	-	(P1M2.2)	-	-	00[1]	00000000
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03[1]	xxxxxx11
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00[1]	xxxxxx00
PCON	Power control register	87H	-	-	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	00000000
PCONA	Power control register A	B5H	RTCPD		VCPD			-	-		00[1]	00000000
PCONB	reserved for Power Control Register B	B6H	-	-	-	-	-	-	-	-	00[1]	xxxxxxxx
		Bit address	D7	D6	D5	D4	D3	D2	D1	D0		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	00000000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	-	-	-	-	00	xx00000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	-	R_WD	R_SF	R_EX	[3]	
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[1] [6]	011xxx00
RTCH	Real-time clock register high	D2H									00[6]	00000000
RTCL	Real-time clock register low	D3H									00[6]	00000000
SP	Stack pointer	81H									07	00000111
TAMOD	Timer 0 auxiliary mode	8FH	-	-	-	-	-	-	-	T0M2	00	xxx0xxx0

9397 750 14465

Table 8: P89LPC902 Special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	00000000
AUXR1	Auxiliary function register	A2H	-	-	-	-	SRST	0	-	DPS	00[1]	000000x0
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	00000000
CMP1	Comparator 1 control register	ACH	-	-	CE1	-	CN1	OE1	CO1	CMF1	00[1]	xx000000
CMP2	Comparator 2 control register	ADH	-	-	CE2	-	CN2	OE2	CO2	CMF2	00[1]	xx000000
DIVM	CPU clock divide-by-M control	95H									00	00000000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	00000000
DPL	Data pointer low	82H									00	00000000
FMADRH	Program Flash address high	E7H									00	00000000
FMADRL	Program Flash address low	E6H									00	00000000
FMCON	Program Flash Control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	01110000
	Program Flash Control (Write)		FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program Flash data	E5H									00	00000000
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	-	ET1	-	ET0	-	00	00000000
		Bit address	EF	EE	ED	EC	EB	EA	E9	E8		
IEN1*	Interrupt enable 1	E8H	-	-	-	-	-	EC	EKBI	-	00[1]	00x00000
		Bit address	BF	BE	BD	BC	BB	BA	B9	B8		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	-	PT1	-	PT0	-	00[1]	x0000000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	-	PT1H	-	PT0H	-	00[1]	x0000000
		Bit address	FF	FE	FD	FC	FB	FA	F9	F8		
IP1*	Interrupt priority 1	F8H	-	-	-	-	-	PC	PKBI	-	00[1]	00x00000
IP1H	Interrupt priority 1 high	F7H	-	-	-	-	-	PCH	PKBIH	-	00[1]	00x00000

Table 8: P89LPC902 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00[1]	xxxxxx00
KBMASK	Keypad interrupt mask register	86H									00	00000000
KBPATN	Keypad pattern register	93H									FF	11111111
	Bit address		**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**		
P0*	Port 0	80H	-	CMP1 /KB6	CMPREF /KB5	CIN1A /KB4	-	KB2	-	KB0	[1]	
	Bit address		**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P1*	Port 1	90H	-	-	$\overline{\text{RST}}$	-	-	-	-	-		
	Bit address		**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
P0M1	Port 0 output mode 1	84H	-	(P0M1.6)	(P0M1.5)	(P0M1.4)	-	(P0M1.2)	-	(P0M1.0)	FF	11111111
P0M2	Port 0 output mode 2	85H	-	(P0M2.6)	(P0M2.5)	(P0M2.4)	-	(P0M2.2)	-	(P0M2.0)	00	00000000
P1M1	Port 1 output mode 1	91H	-	-	(P1M1.5)	-	-	-	-	-	FF[1]	11111111
P1M2	Port 1 output mode 2	92H	-	-	(P1M2.5)	-	-	-	-	-	00[1]	00000000
PCON	Power control register	87H	-	-	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	00000000
PCONA	Power control register A	B5H	RTCPD		VCPD			-	-		00[1]	00000000
PCONB	reserved for Power Control Register B	B6H	-	-	-	-	-	-	-	-	00[1]	xxxxxxxx
	Bit address		**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	00000000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	-	PT0AD.2	-	-	00	xx00000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	-	R_WD	R_SF	R_EX	[3]	
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[1] [6]	011xxx00
RTCH	Real-time clock register high	D2H									00[6]	00000000
RTCL	Real-time clock register low	D3H									00[6]	00000000
SP	Stack pointer	81H									07	00000111

Table 8: P89LPC902 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	8F	8E	8D	8C	8B	8A	89	88		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	-	-	-	-	00	00000000
TH0	Timer 0 high	8CH									00	00000000
TH1	Timer 1 high	8DH									00	00000000
TL0	Timer 0 low	8AH									00	00000000
TL1	Timer 1 low	8BH									00	00000000
TMOD	Timer 0 and 1 mode	89H	-	-	T1M1	T1M0	-	-	T0M1	T0M0	00	00000000
TRIM	Internal oscillator trim register	96H	-	-	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[5] [6]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[4] [6]	
WDL	Watchdog load	C1H									FF	11111111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] All ports are in input only (high impedance) state after power-up.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is '0'. If any are written while BRGEN = 1, the result is unpredictable.

Unimplemented bits in SFRs (labeled '-') are X (unknown) at all times. Unless otherwise specified, ones should not be written to these bits since they may be used for other purposes in future derivatives. The reset values shown for these bits are '0's although they are unknown when read.

[3] The RSTSRC register reflects the cause of the P89LPC901/902/903 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx110000.

[4] After reset, the value is 111001x1, i.e., PRE2-PRE0 are all '1', WDRUN = 1 and WDCLK = 1. WDTOF bit is '1' after Watchdog reset and is '0' after power-on reset. Other resets will not affect WDTOF.

[5] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6] The only reset source that affects these SFRs is power-on reset.

9397 750 14465

The P89LPC901 supports 6 interrupt sources: timers 0 and 1, brownout detect, Watchdog/real-time clock, keyboard, and the comparator.

The P89LPC902 supports 6 interrupt sources: timers 0 and 1, brownout detect, Watchdog/real-time clock, keyboard, and comparators 1 and 2.

The P89LPC903 supports 9 interrupt sources: timers 0 and 1, serial port Tx, serial port Rx, combined serial port Rx/Tx, brownout detect, Watchdog/real-time clock, keyboard, and comparators 1 and 2.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1, and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

8.11.1 External interrupt inputs

The P89LPC901/902/903 has a Keypad Interrupt function. This can be used as an external interrupt input.

If enabled when the P89LPC901/902/903 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 8.14 “Power reduction modes” for details.

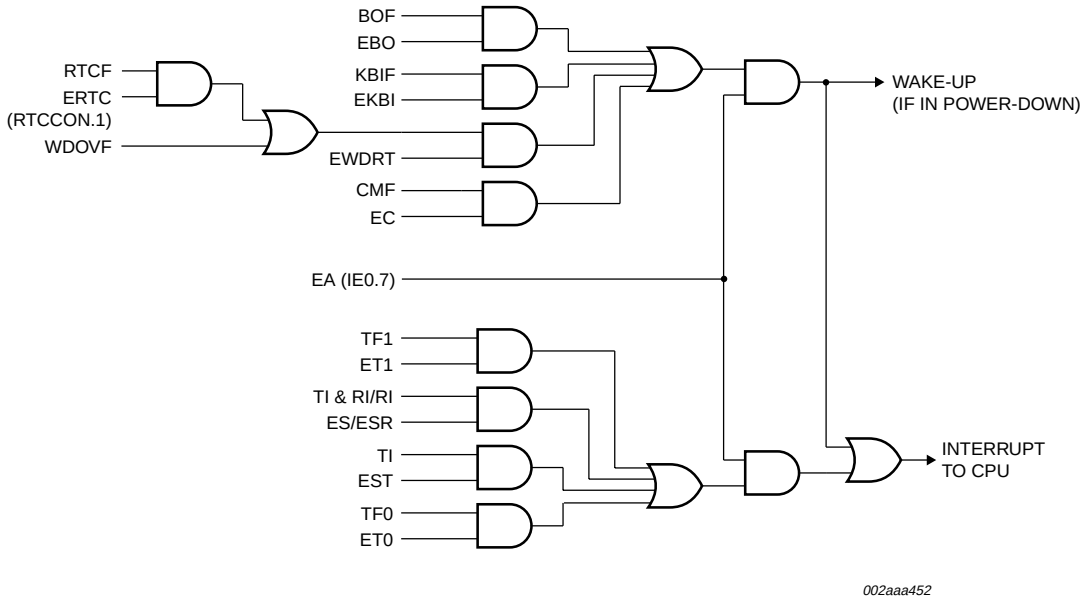


Fig 17. Interrupt sources, interrupt enables, and power-down wake-up sources (P89LPC903).

8.12 I/O ports

The P89LPC901 has between 3 and 6 I/O pins: P0.4, P0.5, P1.2, P1.5, P3.0, and P3.1 The exact number of I/O pins available depends on the clock and reset options chosen, as shown in Table 11.

Table 11: Number of I/O pins available

Clock source	Reset option	Number of I/O pins (8-pin package)
On-chip oscillator or Watchdog oscillator	No external reset (except during power-up)	6
	External $\overline{\text{RST}}$ pin supported	5
External clock input	No external reset (except during power-up)	5
	External $\overline{\text{RST}}$ pin supported[1]	4
Low/medium/high speed oscillator (external crystal or resonator)	No external reset (except during power-up)	4
	External $\overline{\text{RST}}$ pin supported[1]	3

[1] Required for operation above 12 MHz.

The P89LPC902 and P89LPC903 devices have either 5 or 6 I/O pins depending on the reset pin option chosen.

8.12.1 Port configurations

All but one I/O port pin on the P89LPC901/902/903 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

P1.5 ($\overline{\text{RST}}$) can only be an input and cannot be configured.

8.12.2 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC901/902/903 is a 3 V device, however, the pins are 5 V-tolerant (except for XTAL1 and XTAL2). In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.12.3 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic ‘0’. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

An open-drain port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.12.4 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt-triggered input that also has a glitch suppression circuit.

8.12.5 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic ‘1’. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.12.6 Port 0 analog functions

The P89LPC901/902/903 incorporates an Analog Comparator. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high impedance) mode as described in Section 8.12.4 “Input-only configuration”.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register. On any reset, the PT0AD bits default to ‘0’s to enable digital functions.

8.14.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

8.14.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC901/902/903 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the RAM keep-alive voltage V_{RAM}. This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{RAM}, therefore it is highly recommended to wake up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during Power-down. These include: Brownout detect, Watchdog Timer, Comparators (note that Comparators can be powered-down separately), and Real-Time Clock (RTC)/System Timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled.

8.14.3 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled. If the internal RC oscillator is used to clock the RTC during Power-down, there will be high power consumption. Please use an external low frequency clock to achieve low power with the Real-Time Clock running during Power-down.

8.15 Reset

The P1.5/$\overline{\text{RST}}$ pin can function as either an active-LOW reset input or as a digital input, P1.5. The RPE (Reset Pin Enable) bit in UCFG1, when set to ‘1’, enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

Remark: During a power-up sequence, the RPE selection is overridden and this pin will always function as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this input will function either as an external reset input or as a digital input as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit.

Remark: During a power cycle, V_{DD} must fall below V_{POR} (see Table 13 “DC electrical characteristics”) before power is reapplied, in order to ensure a power-on reset.

8.18.9 Transmit interrupts with double buffering enabled (Modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the Tx interrupt is generated when the double buffer is ready to receive new data.

8.18.10 The 9th bit (bit 8) in double buffering (Modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the Tx interrupt.

If double buffering is enabled, TB8 **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

8.19 Analog comparators

One analog comparator is provided on the P89LPC901. Two analog comparators are provided on the P89LPC902 and P89LPC903 devices. Comparator operation is such that the output is a logical one (which may be read in a register) when the positive input is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. The comparator may be configured to cause an interrupt when the output value changes.

The connections to the comparator are shown in Figure 19. **Note:** Not all possible comparator configurations are available on all three devices. Please refer to the Logic diagrams in Section 6 “Logic symbols” on page 12. The comparator functions to V_{DD} = 2.4 V.

When the comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 microseconds. The comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

When a comparator is disabled the comparator’s output, COx, goes HIGH. If the comparator output was LOW and then is disabled, the resulting transition of the comparator output from a LOW to HIGH state will set the comparator flag, CMFx. This will cause an interrupt if the comparator interrupt is enabled. The user should therefore disable the comparator interrupt prior to disabling the comparator. Additionally, the user should clear the comparator flag, CMFx, after disabling the comparator.

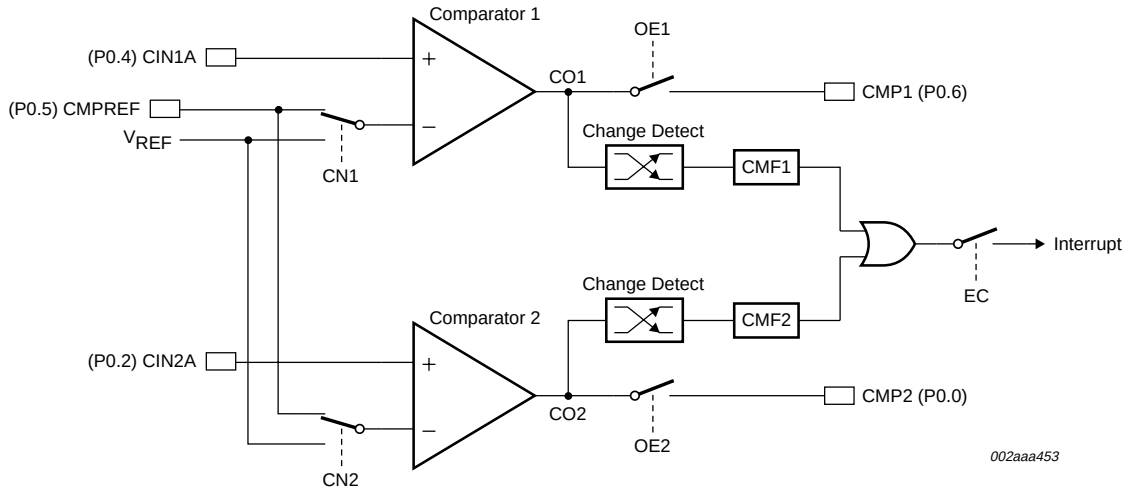


Fig 19. Comparator input and output connections.

8.20 Internal reference voltage

An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as V_{REF}, is 1.23 V ±10%.

8.21 Comparator interrupt

Each comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt.

8.22 Comparator and power reduction modes

The comparators may remain enabled when Power-down or Idle mode is activated, but the comparators are disabled automatically in Total Power-down mode.

If the comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the oscillator stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

The comparator consumes power in Power-down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparator via PCONA.5 or put the device in Total Power-down mode.

8.23 Keypad interrupt (KBI)

The Keypad Interrupt function is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can configure the port via SFRs for different tasks.

The Keypad Interrupt Mask Register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern Register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control Register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control Register (KBCON) is used to define equal or not-equal for the comparison.

In order to use the Keypad Interrupt as an original KBI function like in 87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt may be used to wake up the CPU from Idle or Power-down modes. This feature is particularly useful in handheld, battery powered systems that need to carefully manage power consumption yet also need to be convenient to use.

In order to set the flag and cause an interrupt, the pattern on Port 0 must be held longer than six CCLKs.

8.24 Watchdog timer

The Watchdog timer causes a system reset when it underflows as a result of a failure to feed the timer prior to the timer reaching its terminal count. It consists of a programmable 12-bit prescaler, and an 8-bit down counter. The down counter is decremented by a tap taken from the prescaler. The clock source for the prescaler is either the PCLK or the nominal 400 kHz Watchdog oscillator. The Watchdog timer can only be reset by a power-on reset. When the Watchdog feature is disabled, it can be used as an interval timer and may generate an interrupt. Figure 20 shows the Watchdog timer in Watchdog mode. Feeding the watchdog requires a two-byte sequence. If PCLK is selected as the Watchdog clock and the CPU is powered-down, the watchdog is disabled. The Watchdog timer has a time-out period that ranges from a few μs to a few seconds. Please refer to the *P89LPC901/902/903 User's Manual* for more details.

8.26.6 In-application programming

In-Application Programming is performed in the application under the control of the microcontroller's firmware. The IAP facility consists of internal hardware resources to facilitate programming and erasing. The Philips In-Application Programming has made in-application programming in an embedded application possible without additional components. This is accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the *P89LPC901/902/903 User's Manual*.

8.26.7 Using flash as data storage

The Flash code memory array of this device supports individual byte erasing and programming. Any byte in the code memory array may be read using the MOVC instruction, provided that the sector containing the byte has not been secured (a MOVC instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

8.26.8 User configuration bytes

Some user-configurable features of the P89LPC901/902/903 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the Flash byte UCFG1. Please see the *P89LPC901/902/903 User's Manual* for additional details.

8.26.9 User sector security bytes

There are four User Sector Security Bytes, each corresponding to one sector. Please see the *P89LPC901/902/903 User's Manual* for additional details.

Table 13: DC electrical characteristics…*continued*

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{BO}	brownout trip voltage with BOV = '1', BOPD = '0'	2.4 V < V_{DD} < 3.6 V	2.40	-	2.70	V
V_{REF}	bandgap reference voltage		1.11	1.23	1.34	V
$TC_{(VREF)}$	bandgap temperature coefficient		-	10	20	ppm/ °C

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] The $I_{DD(oper)}$, $I_{PD(idle)}$ specifications are measured using an external clock with the following functions disabled: comparators, brownout detect, and Watchdog timer (P89LPC901).

[3] The $I_{DD(oper)}$, $I_{PD(idle)}$ specifications are measured with the following functions disabled: comparators, brownout detect, and Watchdog timer (P89LPC902, P89LPC903).

[4] Pin capacitance is characterized but not tested.

[5] Measured with port in quasi-bidirectional mode.

[6] Measured with port in high-impedance mode.

[7] Ports in quasi-bidirectional mode with weak pull-up (applies to all port pins with pull-ups)

[8] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from '1' to '0'. This current is highest when V_{IN} is approximately 2 V.

Table 15: AC characteristics (P89LPC901)

V_{DD} = 3.0V to 3.6 V, unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial, unless otherwise specified.[1]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
f_{RCOSC}	internal RC oscillator frequency (nominal f = 7.3728 MHz) trimmed to ± 1% at T_{amb} = 25 °C		7.189	7.557	7.189	7.557	MHz
f_{WDOSC}	internal Watchdog oscillator frequency (nominal f = 400 kHz)		320	520	320	520	kHz
Crystal oscillator							
f_{osc}	oscillator frequency	[2]	0	18	-	-	MHz
t_{CLCL}	clock cycle	see Figure 22	55	-	-	-	ns
f_{CLKP}	CLKLP active frequency		0	8	-	-	MHz
Glitch filter							
	glitch rejection, P1.5/$\overline{RST}$ pin		-	50	-	50	ns
	signal acceptance, P1.5/$\overline{RST}$ pin		125	-	125	-	ns
	glitch rejection, any pin except P1.5/$\overline{RST}$		-	15	-	15	ns
	signal acceptance, any pin except P1.5/$\overline{RST}$		50	-	50	-	ns
External clock							
t_{CHCX}	HIGH time	see Figure 22	22	$t_{CLCL} - t_{CLCX}$	22	-	ns
t_{CLCX}	LOW time	see Figure 22	22	$t_{CLCL} - t_{CHCX}$	22	-	ns
t_{CLCH}	rise time	see Figure 22	-	5	-	5	ns
t_{CHCL}	fall time	see Figure 22	-	5	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified. Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

[2] When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.

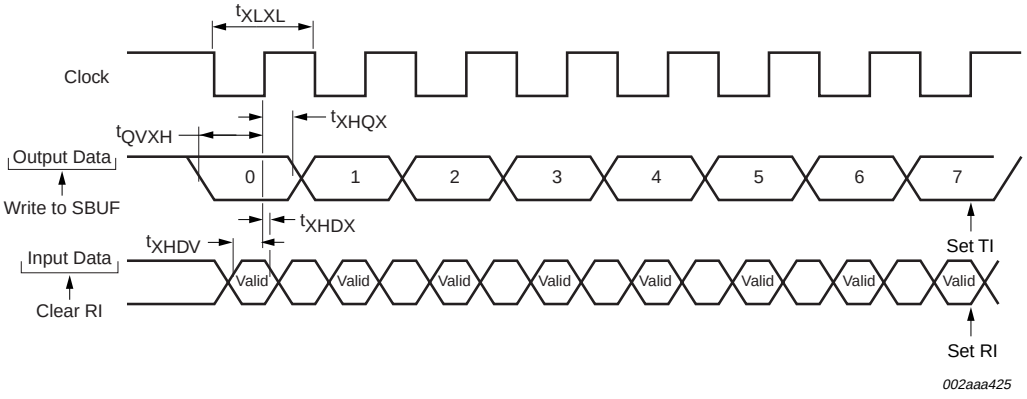


Fig 21. Shift register mode timing.

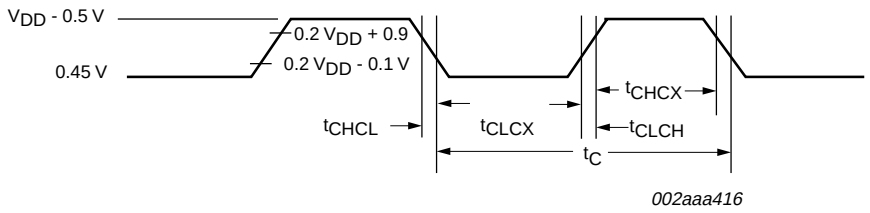


Fig 22. External clock timing.

12. Comparator electrical characteristics

Table 16: Comparator electrical characteristics

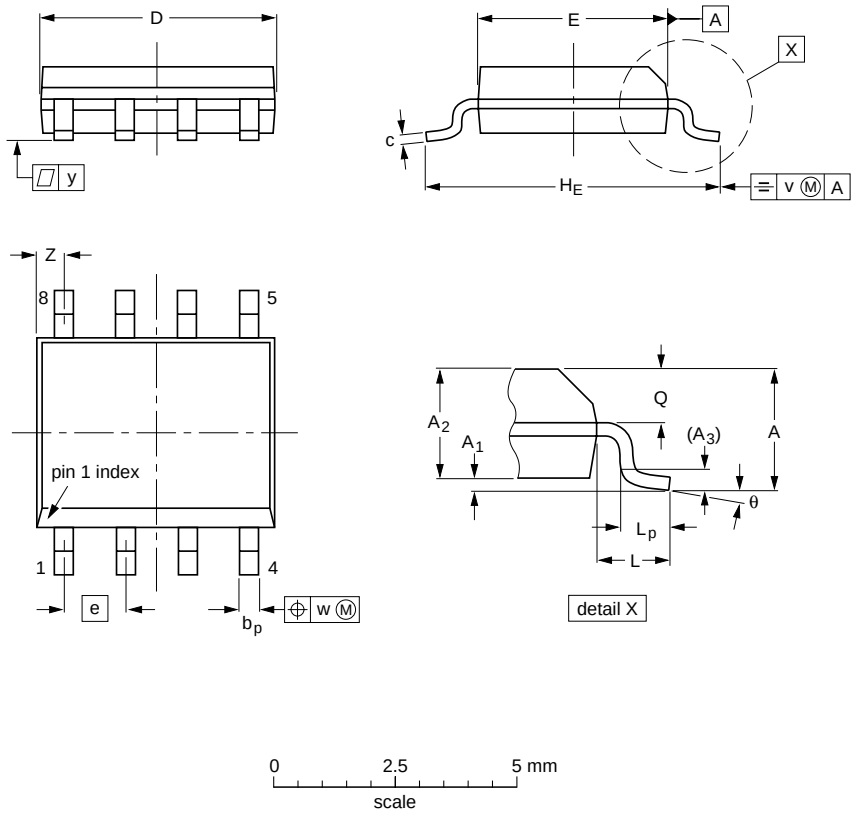
V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = –40 °C to +85 °C for industrial, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IO}	offset voltage comparator inputs			-	-	±20	mV
V_{CR}	common mode range comparator inputs			0	-	V_{DD} – 0.3	V
CMRR	common mode rejection ratio		[1]	-	-	–50	dB
	response time			-	250	500	ns
	comparator enable to output valid			-	-	10	µs
I_{IL}	input leakage current, comparator	$0 < V_{IN} < V_{DD}$		-	-	±10	µA

[1] This parameter is characterized, but not tested in production.

13. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 23. SOT96-1 (SO8).

14. Revision history

Table 17: Revision history

Rev	Date	CPCN	Description
05	20041217	-	**Product data (9397 750 14465)** Modifications: • Added 18 MHz information.
04	20031121	-	**Product data (9397 750 12293); ECN 853-2434 01-A14555 of 18 November 2003**
03	20030929	-	**Product data (9397 750 12031); ECN 853-2434 30348 of 11 September 2003**
02	20030731	-	**Product data (9397 750 11801); ECN 853-2434 30152 of 28 July 2003**
01	20030602	-	**Preliminary data (9397 750 11494)**