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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Networking and Communications
Core Processor	ARM9®
Program Memory Type	External Program Memory
Controller Series	KSZ
RAM Size	-
Interface	EBI/EMI, Ethernet, I²C, I²S,PCI, SPI, UART/USART, USB
Number of I/O	20
Voltage - Supply	1.235V ~ 1.365V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	400-BGA
Supplier Device Package	400-PBGA (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ksz8692pbi

Revision History

Revision	Date	Summary of Changes
1.0	9/23/08	Preliminary Release
2.0	3/10/09	Power Sequencing, Added A1 (PMEN) to pin list, 1.3V Supply for Core, Power Consumption table
3.0	8/10/09	DDR Data Width Changed to 16-bit
4.0	01/28/10	DDR Data Width Changed to 32-bit
4.1	06/10/10	Remove NAND Boot support
5.0	04/14/11	Add small packet device KSZ9692PB-S
	09/13/11	Change the port 0 to port 2 at Figure 12 and 13. Change RSVD to DATA[31..16] in Figure 20.

Contents

System Level Applications

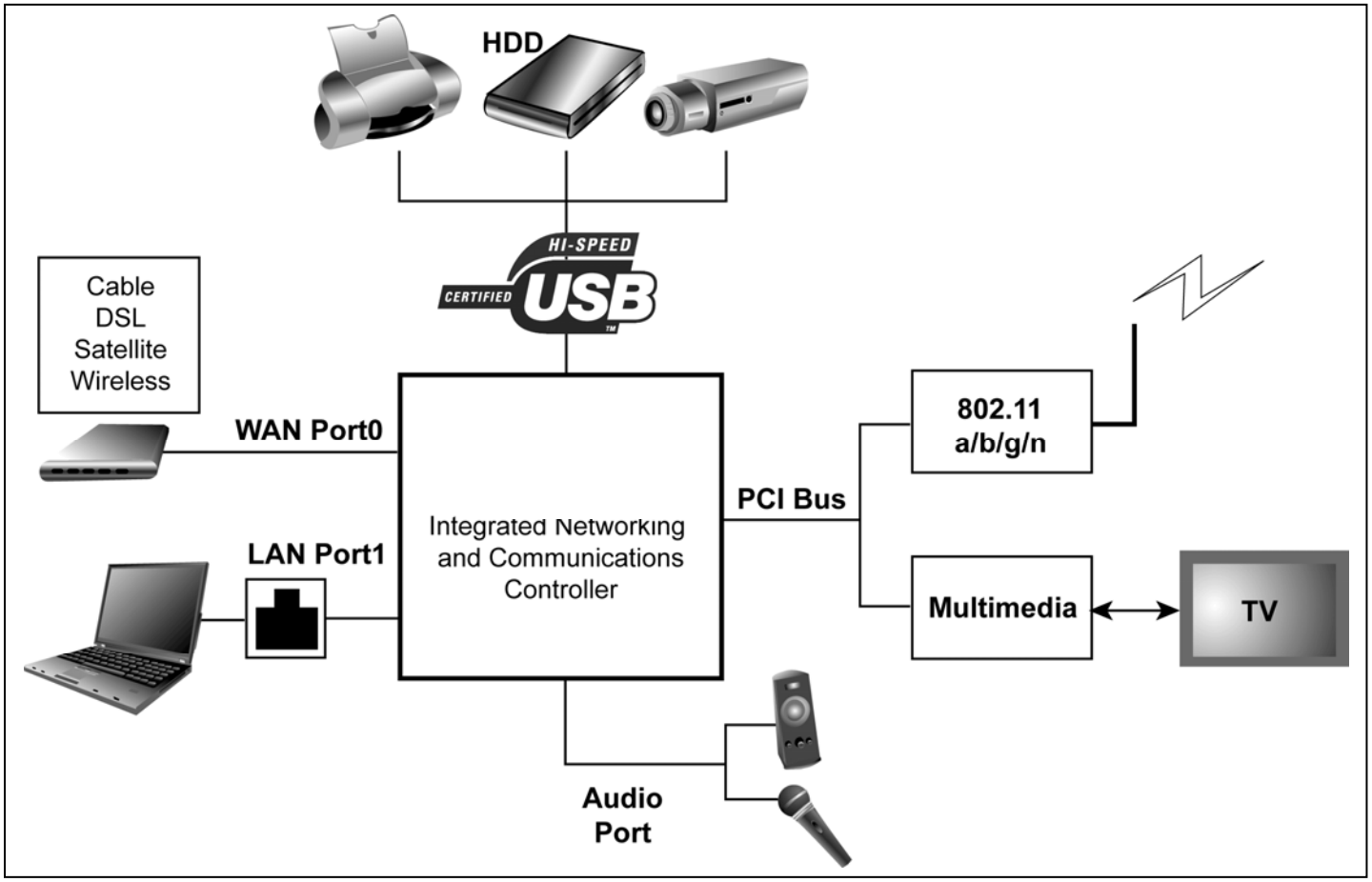

Figure 2. Peripheral Options and Examples

Pin Description: Signal Description by Group

Pin Number	Pin Name	Pin Type	Pin Description
System Interface			
R5	RESETN	I	Reset, asserted Low. RESETN will force the KSZ8692PB, KSZ8692PB-S to reset ARM9 CPU and all functional blocks. Once asserted, RESETN must remain asserted for a minimum duration of 256 system clock cycles. When in the reset state, all the output pins are put into Tri-state and all open drain signals are floated.
N5	WRSTO	O	Watchdog Timer Reset Output When the Watchdog Timer expires, this signal will be asserted for at least 200 msec.
W1	XCLK2	I	System Clock Input 2. External crystal or clock input 2. The clock frequency should be 25MHz ± 50ppm.
Y1	XCLK1	I	System Clock Input 1. Used with XCLK1 pin when other polarity of crystal is needed. This is unused for a normal clock input.
H19	CLK25MHz	O	25MHz output to external PHY
Y15, Y14	DDCLKO[1:0]	O	DDR Clock Out [1:0]. Output of the internal system clock, it is also used as the clock signal for DDR interface.
W15, W14	DDCLKON[1:0]	O	The negative of differential pair of DDR Clock Out [1:0]. Output of the internal system clock, it is also used as the clock signal for DDR interface.
U13	SDCLKEO	O	Clock Enable output for SDRAM (for Power Down Mode)
T7, U7	VREF	I	Reference Voltage for SSTL interface. Must be half of the voltage for the DDR VDD supply. See EIA/JEDEC standard EIA/JESD8-9 (Stub series terminated logic for 2.5V, SSTL_2)
W3	SDOCLK	O	DDR Clock Out for loopback from De-skew PLL
Y3	SDICLK	I	DDR Clock In from loopback to De-skew PLL. This pin must connect to SDOCLK with appropriate de-skew length. See Engineering Evaluation Design Kit for detailed implementation.
Y17, Y16	DDCLKO[3:2]	O	Factory Reserved
W17, W16	DDCLKON[3:2]	O	Factory Reserved
NAND/SRAM/ROM/EXIO Interface			
L2, K1, K2, J3, H5, H4, J2, H3, J1, H2, G5, H1, G3, G4, G2, F1, G1, F2, F3, F5, F4, E1, E2, E3	SADDR[23..0]	O	SRAM Address Bus. The 24-bit address bus covers 16M word memory space of ROM/SRAM/FLASH, and 16M byte external I/O banks. This address bus is shared between ROM/SRAM/FLASH/EXTIO devices.
T2, U1, L5, N4, P3, R2, T1, M4, K5, N3, P2, R1, L4, M3, P1, K4	SDATA[15..0]	Ipu/O	SRAM DATA Bus. Bidirectional Bus for 16-bit DATA In and DATA Out. The KSZ8692PB, KSZ8692PB-S also supports 8-bit data bus for ROM/SRAM/FLASH/EXTIO cycles. This data bus is shared between NAND, ROM/SRAM/FLASH/EXTIO devices.

Pin Description: Signal Description by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
G15	USBCFG	I	USB port 2 configuration "1" = port 2 is host "0" = port 2 is device (port 1 is always host)
F18	USBHOVC0	I	Over current sensing input for Host Controller downstream port 1
F15	USBHOVC1	I	Over current sensing input for Host Controller downstream port 2
F17	USBHPWR0	Ipu/O (open drain)	Power switching control output for downstream port 1; open drain output
F16	USBHPWR1	Ipu/O (open drain)	Power switching control output for downstream port 2; open drain output
SDIO Interface			
D14	KCMD	Ipd/O	SD 4-bit mode: Command line SD 1-bit mode: Command line
C18	KCLK	Ipd/O	SDIO/SD Clock
C15	KDATA3	I/O	SD 4-bit mode : data line 3 SD 1-bit mode : not used
C16	KDATA2	I/O	SD 4-bit mode : data line 2 or read wait (optional) SD 1-bit mode : read wait (optional)
E13	KDATA1	I/O	SD 4-bit mode : data line 1 or interrupt (optional) SD 1-bit mode : interrupt
C17	KDATA0	I/O	SD 4-bit mode : data line 0 SD 1-bit mode : data line
C14	KSDCDN	I	Active low used for Card Detection
D13	KSDWP	I	Active high used for Card write protection
General Purpose I/O			
B14	SLED/GPIO[19]	I/O	SDIO Line Status LED output or General Purpose I/O Pin[19]
B15	CPUINTN/ GPIO[18]	I/O	Internal CPU interrupt request or General Purpose I/O Pin[18] As CPUINTN, any interrupt generated to ARM CPU asserts logic low on this pin. Useful for software development.
B16, B17, B18, D18, E15, D19	GPIO[17:12]	I/O	General Purpose I/O Pin[17:12]
F14	UART 4 RTSN /GPIO[11]	I/O	UART 4 RTS or general purpose I/O Pin[11]
E16	UART 4 CTSN /GPIO[10]	I/O	UART 4 CTS or general purpose I/O Pin[10]
E17	UART 3 RTSN /GPIO[9]	I/O	UART 3 RTS or general purpose I/O Pin[9]
E19	UART 3 CTSN /GPIO[8]	I/O	UART 3 CTS or general purpose I/O Pin[8]
E20	UART 2 RTSN /GPIO[7]	I/O	UART 2 RTS or general purpose I/O Pin[7]

Pin Description: Signal Description by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
E18	UART 2 CTSN /GPIO[6]	I/O	UART 2 CTS or general purpose I/O Pin[6]
U20, U19	TOUT[1:0]/ GPIO[5:4]	I/O	Timer 1/0 out or General Purpose I/O Pin[5:4]
V20, T18, V19, U18	EINT[3:0]/ GPIO[3:0]	I/O	External Interrupt Request or General Purpose I/O Pin[3:0]
I2S Interface			
C20	SCKIN	I	External crystal or clock input for I2S clock The maximum supported frequency is 49.2 MHz
D20	SCKOUT	O	External crystal out for I2S clock
C19	I2S_MCLK	O	I2S master clock out This clock is of same frequency as SCKIN
B20	I2S_BCLK	O	I2S bit clock out
B19	I2S_LRCLK	O	Left/right select
A19	I2S_SDO	O	Serial data out
A20	I2S_SDI	I	Serial data in
MDIO/MDC Interface			
H18	MDC	Ipu/O	Clock for station management
H17	MDIO	Ipu/O	Serial data for station management
I2C/SPI Interface			
E14	SPCK_SCL	Ipu/O	SPI mode: master clock Output I2C mode: serial clock output
D17	SPMOSI_SDA	Ipu/O	SPI mode: master data out, slave data in I2C mode: serial data
D16	SPMISO	I	SPI master data in, slave data out
D15	SPICS	Ipu/O	SPI chip select
F13	SPI_RDY	I	Micrel SPI mode ready signal
PCI Interface Signals			
C3	PRSTN	I	PCI Reset, asserted Low In Host Bridge Mode, the PCI Reset pin is an input. This pin as well as the reset pin of all the devices on the PCI bus could be driven by WRSTO. In Guest Bridge Mode, this pin is input. The system reset to drive this pin.
B2	PCLK	I	PCI Bus Clock input. This signal provides the timing for the PCI bus transactions. This signal is used to drive the PCI bus interface and the internal PCI logic. All PCI bus signals are sampled on the rising edges of the PCLK. PCLK can operate from 20MHz to 33MHz, or 66MHz.
E4	GNT3N	O	PCI Bus Grant 3 Assert Low. In Host Bridge Mode, this is an output signal from the internal PCI arbiter to grant PCI bus access to the master driving REQ3N. In Guest Bridge Mode, this is unused.

Pin Description: Signal Description by Group (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
D4	GNT2N	O	PCI Bus Grant 2 Assert Low. In Host Bridge Mode, this is an output signal from the internal PCI arbiter to grant PCI bus access to the master driving REQ2N. In Guest Bridge Mode, this is unused.
B1	GNT1N	O	PCI Bus Grant 1 Assert Low. In Host Bridge Mode, this is an output signal from the internal PCI arbiter to grant PCI bus access to the master driving REQ1N. In Guest Bridge Mode, this is an output signal to indicate to the external PCI bus arbiter that KSZ8692PB, KSZ8692PB-S is requesting access to the PCI bus.
D3	REQ3N	I	PCI Bus Request 3 Assert Low. In Host Bridge Mode, this is an input signal from the external PCI device to request for PCI bus access In Guest Bridge Mode, this is unused.
E6	REQ2N	I	PCI Bus Request 2 Assert Low. In Host Bridge Mode, this is an input signal from the external PCI device to request for PCI bus access In Guest Bridge Mode, this is unused.
C1	REQ1N	I	PCI Bus Request 1 Assert Low. In Host Bridge Mode, this is an input signal from the external PCI device to request for PCI bus access In Guest Bridge Mode, this signal comes from the external arbiter to indicate that the bus is granted to KSZ8692PB, KSZ8692PB-S.
B3, E7, D6, A2, B4, A3, D7, C5, C6, B5, A4, A5, B6, E8, C7, D8, D10, B10, A11, B11, C11, A12, E11, D11, B12, A13, C12, B13, F12, C13, D12, E12	PAD[31..0]	I/O	32-bit PCI address and data lines Addresses and data bits are multiplexed on the same pins. During the first clock cycle of a PCI transaction, the PAD bus contains the first clock cycle of a PCI transaction, the PAD bus contains the physical address. During subsequent clock cycles, these lines contain the 32-bit data to be transferred. Depending upon the type of the transaction, the source of the data will be the KSZ8692PB, KSZ8692PB-S if it initiates a PCI write transaction, or the data source will be the target if it is a PCI Read transaction. The KSZ8692PB, KSZ8692PB-S bus transaction consists of an address phase followed by one or more data phases. The KSZ8692PB, KSZ8692PB-S supports both Read and Write burst transactions. In case of a Read transaction, a special data turn around cycle is needed between the address phase and the data phase.
A6, A7, E10, C10	CBEN[3..0]	I/O	PCI Commands and Byte Enable, asserted Low. The PCI command and byte enable signals are multiplexed on the same pins. During the first clock cycle of a PCI transaction, the CBEN bus contains the command for the transaction. The PCI transaction consists of the address phases and one or more data phases. During the data phases of the transaction, the bus carries the byte enable for the current data phases.

Pin Descriptions-Power up Strapping Options

Certain pins are sampled upon power up or reset to initialize KSZ8692PB, KSZ8692PB-S system registers per system configuration requirements.

Pin Number	Pin Name	Pin Type	Pin Description
E3	SADDR[0]	Ipd/O	During reset, this pin is input strap option for NAND Boot small page size 0 = 512 Bytes (default) 1 = 528 Bytes (Not support NAND Boot)
E1, E2	SADDR[2:1]	Ipd/O	During reset, this pin is input strap option for NAND Flash configuration register (0x8054) bit [7:6]. These pins are used to specify number of active banks (CE#) in cascade. 00 = 1 bank (default) 01 = 2 banks
F4	SADDR[3]	Ipd/O	During reset, this pin is input strap option for NAND Flash configuration register (0x8054) bit [8], NAND Flash type. This pin is used to specify using large or small block NAND Flash as a boot bank as follows: “0” = small block (default) “1” = large block (Not support NAND Boot)
F5	SADDR[4]	Ipd/O	During reset, this pin is input strap option for NAND Flash configuration register (0x8054) bit [4], NAND Flash type. This pin is used to specify number of NAND Flash in parallel for combined data width as follows: “0” = 1 NAND Flash (default) “1” = 2 NAND Flash
F3	SADDR[5]	Ipu/O	During reset, this is input strap option to enter ARM9 tic test mode 0: ARM tic test mode (factory reserved) 1: Normal mode (default)
F2	SADDR[6]	Ipd/O	During reset, this pin is input strap option for NAND FLASH device support automatic page crossing 0: NAND FLASH device does not support automatic page crossing (default) 1: NAND FLASH device supports automatic page crossing
G1	SADDR[7]	Ipd/O	During reset, this pin is a strapping option for B0SIZE, Bank 0 Data Access Size. This is applicable to ROM/SRAM/FLASH boot bank. Bank 0 is used for boot program. This pin is used to specify the size of the bank 0 data bus width as follow: “0” = one byte (default) “1” = half word
F1	SADDR[8]	Ipd/O	During reset, this pin is a strapping option for BTSEL: “0” = Boot select from NOR flash (default) “1” = Boot select from NAND flash (Not support NAND Boot)
G2	SADDR[9]	Ipd/O	During reset this pin is a strapping option for BYP_SYSPLL: “0” = Use systems PLL (default) “1” = Bypass systems PLL, use external clock (factory reserved)
G4	SADDR[10]	Ipd/O	During reset this pin is a strapping option for BYP_CLKSEL: “0” = Select 200MHz external clock (default) “1” = Select 250MHz external clock (factory reserved)

Pin Descriptions-Power up Strapping Options (Continued)

Pin Number	Pin Name	Pin Type	Pin Description
U2	NALE	Ipd/O	NAND Address Latch Enable NALE controls the activating path for address sent to NAND flash. During reset, this pin is input strap option for NAND Flash configuration register (0x8054) bit [1]. This bit along with configuration register bits [2], [0] is used for boot program. This pin along with NCLE and NWEN is used to specify NAND Flash size. [NCLE, NALE, NWEN] 000 = 64Mbit 001 = 128Mbit (default) 010 = 256Mbit 011 = 512Mbit 100 = 1Gbit 101 = 2Gbit 110 = 4Gbit 111 = 8Gbit (Not support NAND Boot)
T4	NWEN	Ipu/O	NAND Write Enable, asserted low During reset, this pin is input strap option for NAND Flash configuration register (0x8054) bit [0]. This bit along with configuration register bits [2:1] is used for boot program. This pin along with NCLE and NALE is used to specify NAND Flash size. [NCLE, NALE, NWEN] 000 = 64Mbit 001 = 128Mbit (default) 010 = 256Mbit 011 = 512Mbit 100 = 1Gbit 101 = 2Gbit 110 = 4Gbit 111 = 8Gbit (Not support NAND Boot)
U3	NWPN	Ipu/O	NAND Write Protection, asserted low During reset, this pin is input strap option to enable test modes. This pin along with TESTEN, TESTEN1 form different test modes. {TESTEN, TESTEN1, NWPN} = 011: ARM Scan test mode 010: USB Analog Bits test mode others: refer to TESTEN and TESTEN1 pin description (factory reserved)
G15	USBCFG	I	USB port 2 configuration “1” = port 2 is host “0” = port 2 is device (port 1 is always host)
Test Pins Strapping Options			

ARM High-Performance Processor

The KSZ8692PB, KSZ8692PB-S is built around the 16/32-bit ARM922T RISC processor designed by Advanced RISC Machines. The ARM922T is a scalable, high-performance processor that was developed for highly integrated SoC applications. Its simple, elegant, and fully static design is particularly suitable for cost-effective and power-sensitive embedded systems. It also offers a separate 8KB D-cache and 8KB I-cache that reduces memory access latency.16-bit thumb instruction sets are supported to minimize memory footprint. The ARM processor core can be programmed to maximum of 250 MHz for highest possible performance.

The Advanced Microprocessor Bus Architecture/Advanced High Performance Bus (AMBA AHB) is a 32-bit wide ARM system bus to which is connected the processor, the register ports of the DDR memory controller, the FLASH/ROM/SRAM/External I/O controller, the NAND memory controller, the Ethernet MACs, the PCI bridge, the USB ports and the SDIO controller. The ARM processor is the master of AHB and responsible for configuring the operational characteristics of each AHB device via their individual register port. The AHB is programmable up to 166MHz for maximum system bus performance. AHB interfaces to devices are shown in functional block diagram.

Also connected to AHB is ARM Advanced Peripheral Bus or APB bridge which is attached the standard peripherals. The APB Bridge transparently converts the AHB accesses into slower APB accesses. The ARM processor is the master of APB bridge and responsible for configuring the operational characteristics and transfer of data for each APB attached peripheral. APB interfaces to standard peripherals are shown in functional block diagram.

- 250MHz ARM922T RISC processor core
- 166MHz AMBA Bus 2.0
- 16-bit thumb instruction sets
- 8KB D-cache and 8KB I-cache
- Supports Little-Endian mode
- Configurable MMU
- Power saving options include clock down of both processor core and AMBA AHB

FLASH/ROM/SRAM Memory and External I/O Interface

The KSZ8692PB, KSZ8692PB-S memory controller provides glueless interface for static memory, i.e. ROM, SRAM, and NOR Flash and three banks of external I/O. NOR Flash bank0 can be configured by power-up strap option to operate as boot bank from a 8 or 16 bit device.

- Glueless connection to two banks of FLASH/ROM/SRAM memory with programmable 8 or 16 bit data width and programmable access timing
- Support for AMD/Intel like Flash
- Automatic address line mapping for 8 or 16-bit accesses on Flash, ROM, and SRAM interfaces
- Supports three external I/O banks with programmable 8 or 16 bit data width and programmable access timing
- Total 64MB address space for two banks of FLASH/ROM/SRAM and and three banks of external I/O

The memory interface for the static memory has a special automatic address mapping feature. This allows the designer to connect address bit 0 on the memory to ADDR[0] on the KSZ8692PB, KSZ8692PB-S and address bit 1 on the memory to ADDR[1] on the KSZ8692PB, KSZ8692PB-S, regardless of whether the designer is trying to achieve half word or byte addressing. The KSZ8692PB, KSZ8692PB-S memory controller performs the address mapping internally. This gives the designer the flexibilty to use 8 or 16 bit data width devices interchangeably on the same PCB (see Figure 4). For external I/O, however, the designer still needs to resolve the address mapping (see Figure 5).

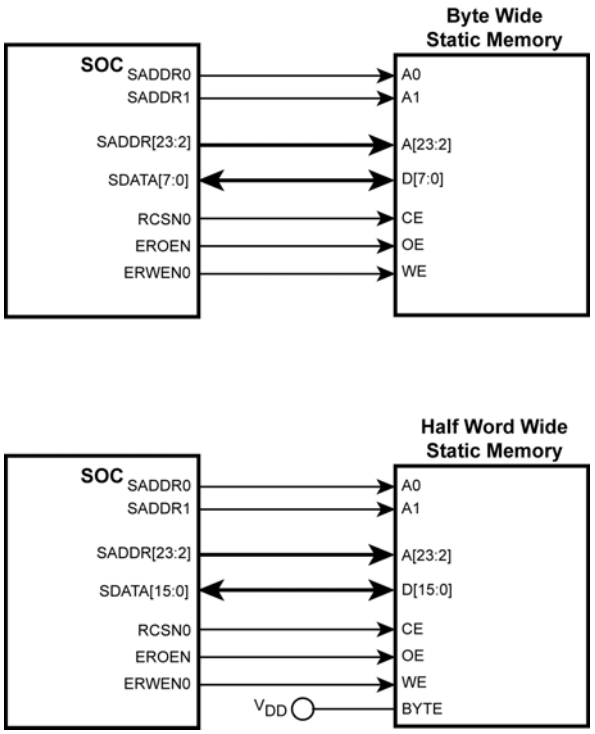

Figure 4. Static Memory Interface Examples

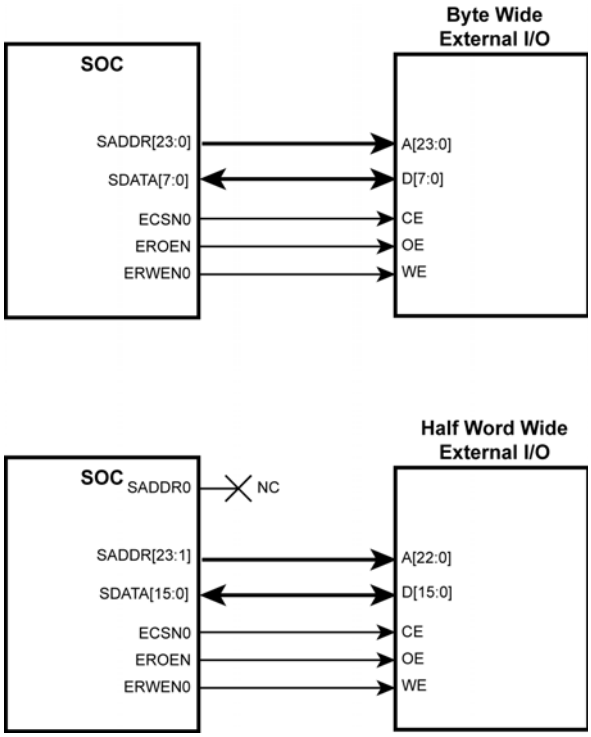

Figure 5. External I/O Interface Examples

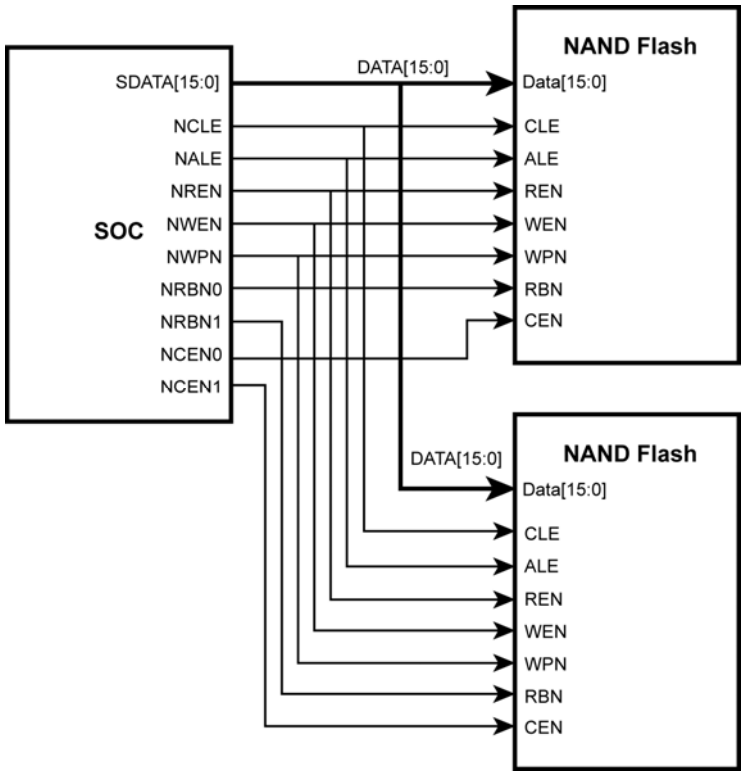

Figure 7. 16-bit NAND Interface Examples

DDR Controller

The KSZ8692PB, KSZ8692PB-S DDR memory controller provides interface for accessing external Double Data Rate Synchronous DRAM. In addition the KSZ8692PB, KSZ8692PB-S provides two integrated DDR differential clock drivers for a complete glueless DDR interface solution.

- Up to 200MHz clock frequency (400MHz data rate)
- Supports one 32-bit data width bank (16-bit optional)
- Up to 128 MB of addressable space is available with 12 columns and 14 row address lines
- Supports all DDR device densities up to 1Gb
- Supports all DDR device data width x8 and x16
- Configurable DDR RAS and CAS timing parameters
- Two integrated JEDEC Specification JESD82-1 compliant differential clock drivers for a glueless DDR interface solution
- JEDEC Specification SSTL_2 I/Os

SDIO/SD Host Controller

Integrated SDIO/SD host controller provides interface for removable mass storage memory card and I/O devices.

- Meets SD Host Controller Standard Specification Version 1.0
- Meets SD memory card spec 1.01 . MMC spec 3.31
- Meets SDIO card specification version 1.0
- 1or 4 bit mode supported
- Card detection-insertion/removal
- Line Status LED driver
- Password protection of cards
- Supports read wait control, suspend/resume operation
- Support multi block read and write
- Up to 12.5 Mbytes per second read and write rates using 4 parallel line for full speed card.
- Dedicated DMA or programmed I/O data transfer

IP Security Engine

Integrated hardware security engine performs complex encryption, decryption and authentication tasks with minimum ARM processor intervention to peak line rate of 100Mbps.

- ESP, AH mode
- Transport mode
- Tunnel mode
- IPv4
- Extended Sequence Numbers
- Data Descriptor Table (DDT)based packet memory
- AES-ECB/CBC; 128/192/256-bit keys
- DES/3DES-ECB/CBC
- RC4; 40/128 bit keys
- MD5, SHA-1, SHA-256
- HMAC-MD5
- HMAC-SHA1
- HMAC-SHA-256
- SSLMAC SHA-1
- SSLMAC MD5
- Dedicated DMA channel

USB 2.0 Interface

Integrated dual USB 2.0 interface can be configured as 2-port host, or host + device. Figures 12 and 13 illustrate examples of USB 2.0 interface applications.

- Compliant with USB Specification Revision 2.0
- Compliant with Open Host Controller Interface (OHCI) Specification Rev 1.0a
- Compliant with Enhanced Host Controller Interface (EHCI) Specification Rev 1.0
- Root hub with 2 (max) downstream facing ports which are shared by OHCI and EHCI host controller cores
- All downstream facing ports can handle High-Speed (480Mbps), Full-Speed (12Mbps), and Low-Speed (1.5Mbps) transaction
- OTG not supported
- Integrated 45-ohm termination, 1.5K pull-up and 15K pull-down resistors
- Support endpoint zero, and up to 6 configurable endpoints (IN/OUT, isochronous/ control/ interrupt/ bulk)
- One isochronous endpoint (IN or OUT)
- Dedicated DMA Channel for each port

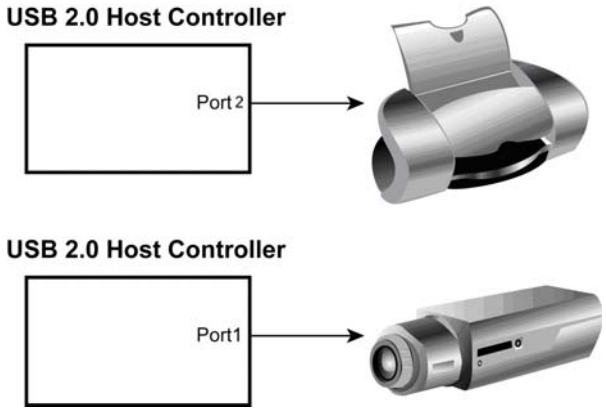

Figure 12. USB 2.0 Configuration as Two-Port Host

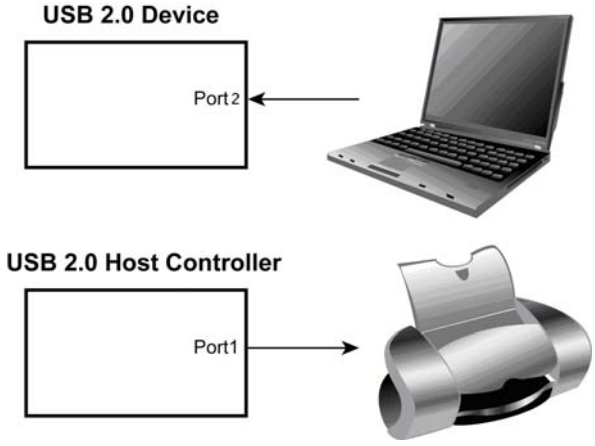

Figure 13. USB 2.0 Configuration as Host + Device

takes no further action. If the KSZ8692PB, KSZ8692PB-S controller detects the data sequence, however, it then alerts the device's power management circuitry to wake up the system.

IPv6 Support

The KSZ8692PB, KSZ8692PB-S provides the following IPv6 support in the hardware:

- Generates the checksum for IPv6 TCP/UDP packets based on register configuration (LAN MAC DMA Transmit Control Register and WAN MAC DMA Transmit Control Register) or Transmit Descriptor 1 (TDES1). The register setting is static configuration and the TDES1 setting is packet based configuration.
- Filters IPv6 packets with TCP/UDP errors (LAN MAC DMA Receive Control Register and WAN MAC DMA Receive Control Register).
- Supports up to 8 Source IP or Destination IP based filtering (LAN/WAN Access Control List)

Refer to the Register Description Document for more details.

DMA Controller

Integrated DMA controller connects data port of IP Security Engine, two Ethernet MACs, two USB 2.0 ports, PCI 2.3 bus interface, and SDIO interface via dedicated channels to DDR memory controller for moving large amounts of data without significant ARM processor intervention. A typical DMA channel usage is to move data from these interfaces into DDR memory. The data in the memory is processed by the ARM processor and driven back by the DMA channel to the external interface. Additionally, the ARM processor itself has a dedicated DMA channel to access the DDR memory controller. Flash/ROM/SRAM, NAND controller, and peripherals do not have dedicated DMA channel and therefore depend on the ARM processor for transfer of data to DDR memory. DMA channel interfaces are shown in functional block diagram.

The arbitration of all requests from DMA channels are handled by the DDR memory controller and pipelined for best performance. The memory controller supports programmable bandwidth allocation for each DMA channel, thus enabling the designer to optimize I/O resource utilization of memory.

UART Interface

The KSZ8692PB, KSZ8692PB-S support four independent high-speed UARTs: UART1, UART2, UART3 and UART4. The UART ports enhance the system availability for legacy serial communication application and console port display.

UART1, UART2, UART3 and UART4 support maximum baud rate of 5 Mbps including standard rates. The higher rates allow for Bluetooth and GSM applications.

UART1 supports CTSN, DSRN, DCDN modem control pins in addition to RXD and TXD data pins. For UART2, UART3, UART4 only CTSN and RTSN control pins in addition to RXD and TXD data pins are supported.

Timers and Watchdog

Two programmable 32-bit timers with one capable of watchdog timer function. These timers can operate in a very flexible way. The host can control the timeout period as well as the pulse duration. Both timers can be enabled with interrupt capability. When the watchdog timer is programmed and the timer setting expires, the KSZ8692PB, KSZ8692PB-S resets itself and also asserts WRSTO to reset other devices in the system.

GPIO

Twenty general purpose I/O (GPIO) are individually programmable as input or output. Some GPIO ports are programmable for alternate function as listed below:

- Four GPIO programmable as inputs for external interrupts
- Two GPIO programmable as 32-bit timers output
- Six GPIO programmable as CTSN and RTSN control pins for UART2, UART3, UART4
- One GPIO programmable as SDIO Line Status LED driver
- One GPIO programmable as ARM CPU interrupt line activity.

See Signal Description list for detailed GPIO map.

I2C

The I2C interface is a 2-pin (SCL & SDA) generic serial bus interface for both control and data. The KSZ8692PB,

KSZ8692PB-S supports master mode I2C interface. To increase the firmware efficiency, KSZ8692PB, KSZ8692PB-S is equipped with hardware assisted logic to take care I2C bus sequence and protocol.

- Supports one master (KSZ8692PB, KSZ8692PB-S) in the system
- 8-bit or 10-bit addressing
- Up to 8 byte burst for read and write
- Programmable SCL clock rate for up to 400kHz

The I2C interface shares the same pins with the SPI interface.

SPI

The Serial Peripheral Interface (SPI) is a synchronous serial data link that provides communication with external devices.

- 8- to 16-bit Programmable Data Length
- Programmable Serial Clock Phase and Polarity
- Programmable Active Level of Chip Select (CS)
- Programmable Delays between Two Active CS
- Programmable Delays between Consecutive Transfers without Removing CS
- Programmable Delays between Assertion CS and 1st SPCK
- Programmable SPI clock (SPCK) rate in the range of AMBA System Clock (SYSCLK) divided by a value between 16 and 65536

The SPI interface shares the same pins with the I2C interface.

I2S

I2S provides programmable 16-, 18-, 20-, 24-bit resolution audio for two (stereo) channels playback and recording.

Interrupt Controller

Interrupt controller handles external and internal interrupt sources.

- Normal or fast interrupt mode (IRQ, FIQ) supported
- Prioritized interrupt handling

Timing Specifications

Figure 16 provides power sequencing requirement with respect to system reset.

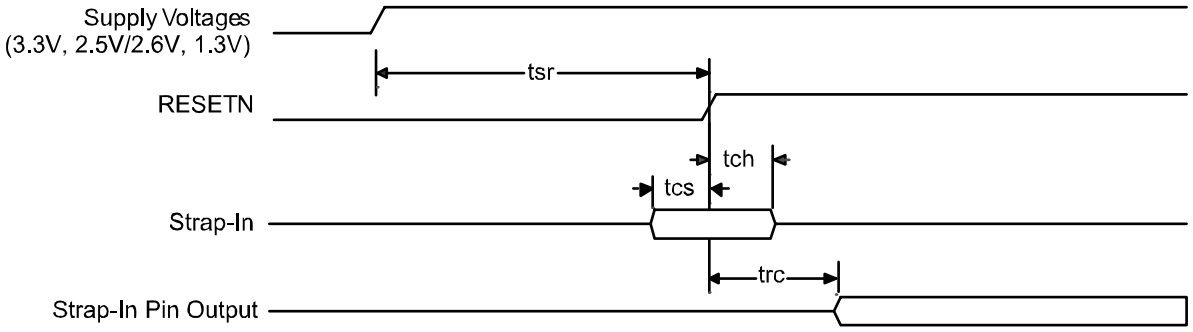

Figure 16. Reset Timing

Note: Power sequencing of supply voltages must be in order of 3.3V first, 2.5V/2.6V next and 1.3V last

Symbol	Parameter	Min	Typ	Max	Units
t_{SR}	Stable supply voltages to reset high	10			ms
t_{CS}	Configuration set-up time	50			ns
t_{CH}	Configuration hold time	50			ns
t_{RC}	Reset to strap-in pin output	50			ns

Table 1. Reset Timing Parameters

Figure 17 and Figure 18 provide NOR FLASH, ROM and SRAM interface timing.

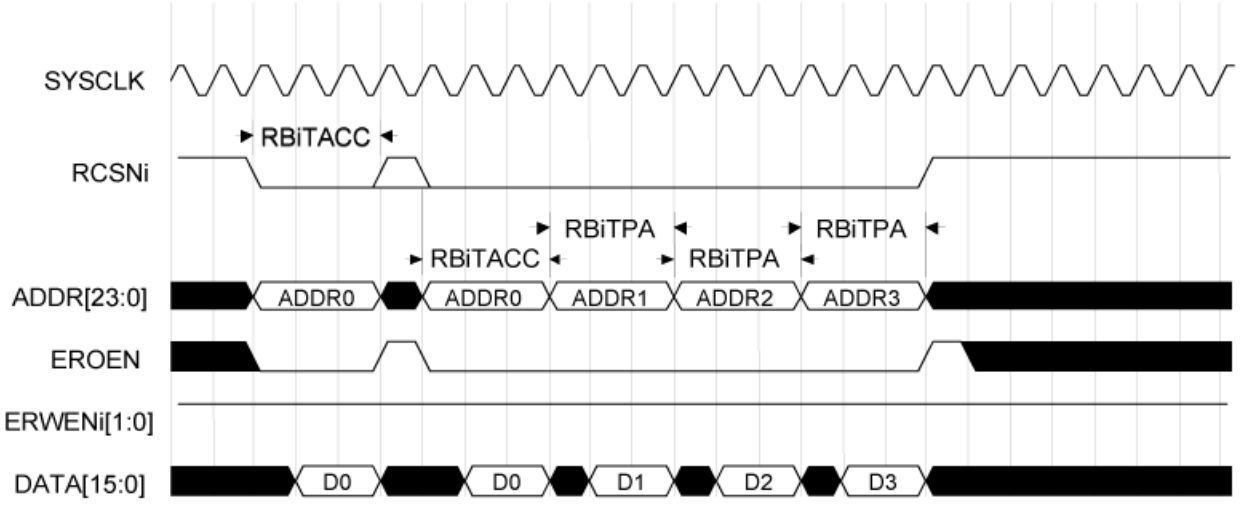

Figure 17. Static Memory Read Cycle

Symbol	Parameter	Min[1]	Typ[1]	Max[1]	Units
T_{cta}	Valid address to CS setup time	EBiTACS +0.8	EBiTACS +1.1	EBiTACS +1.3	ns
T_{cos}	OE valid to CS setup time	EBiTCOS +0.6	EBiTCOS +0.6	EBiTCOS +1.0	ns
T_{dsu}	Valid read data to OE setup time	2.0			ns
T_{cws}	WE valid to CS setup time	EBiTCOS +0.6	EBiTCOS +0.6	EBiTCOS +1.0	ns
T_{dh}	Write data to CS hold time	0			ns
T_{cah}	Address to CS hold time	EBiTCOH +1.0	EBiTCOH +1.0	EBiTCOH +1.4	ns
T_{oew}	OE/WE pulsewidth	EBiTACT		EBiTACT	ns
T_{ocs}, T_{csw}	Rising edge CS to OE/WE hold time	0			ns

Table 3. External I/O Memory Timing Parameters

Note:

1. Measurements for minimum were taken at 0°C, typical at 25°C, and maximum at 100°C.

Symbol	Parameter[1]	Registers
EBiTACS	Programmable bank i address setup time before chip select	0x5000, 0x5004, 0x5008
EBiTACT	Programmable bank i write enable/output enable access time	0x5000, 0x5004, 0x5008
EBiTCOS	Programmable bank i chip select setup time before OEN	0x5000, 0x5004, 0x5008
EBiTCOH	Programmable bank i chip select hold time	0x5000, 0x5004, 0x5008

Table 4. Programmable External I/O Timing Parameters

Note:

1. "i" Refers to chip select parameters 0, 1, or 2.

Signal Location Information

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	PMEN	PAD28	PAD26	PAD21	PAD20	CBEN3	CBEN2	CLKRUNN	DEVSELN	PERRN	PAD13	PAD10	PAD6	TRSTN	TDO	TDI	TMS	TCK	I2S_SDO	I2S_SDI
B	GNT1N	PCLK	PAD31	PAD27	PAD22	PAD19	IDSEL	IRDYN	STOPN	PAD14	PAD12	PAD7	PAD4	GPIO19	GPIO18	GPIO17	GPIO16	GPIO15	I2S_LRCLK	I2S_BCLK
C	REQ1N	MPCIACTN	PRSTN	M66EN	PAD24	PAD23	PAD17	PAR	SERRN	CBEN0	PAD11	PAD5	PAD2	KSDCDN	KDATA3	KDATA2	KDATA0	KCLK	I2S_MCLK	SCKIN
D	PCLKOUT2	PCLKOUT1	REQ3N	GNT2N	PMBS	PAD29	PAD25	PAD16	FRAMEN	PAD15	PAD8	PAD1	KSDWP	KCMD	SPICS	SPMISO	SPMOSI_SDA	GPIO14	GPIO12	SCKOUT
E	SADDR2	SADDR1	SADDR0	GNT3N	PCLKOUT0	REQ2N	PAD30	PAD18	TRDYN	CBEN1	PAD9	PAD0	KDATA1	SPCK_SCL	GPIO13	GPIO10	GPIO9	GPIO6	GPIO8	GPIO7
F	SADDR8	SADDR6	SADDR5	SADDR3	SADDR4	PCLKOUT3	VDD3.3	VDD3.3	VDD3.3	VDD3.3	VDD3.3	PAD3	SPIRDY	GPIO11	USBHOVC1	USBHPWR1	USBHPWR0	USBHOVC0	U2P	U2M
G	SADDR7	SADDR9	SADDR11	SADDR10	SADDR13	VDD3.3	VDD1.2	VDD1.2	VDD1.2	VDD3.3	VDD3.3	USB1VDDA3.3	USBCVDDA3.3	USB2VDDA3.3	USBCFG	USBTEST	USBXI	USBXO	U1P	U1M
H	SADDR12	SADDR14	SADDR16	SADDR18	SADDR19	VDD3.3	GND	GND	GND	GND	GND	USBVSS2	USBVSSA3.3	VDD3.3	USB2VDD1.2	USBREXT	MDIO	MDC	CLK25MHZ_1	P1_TXD3
J	SADDR15	SADDR17	SADDR20	ERWEN0	ERWEN1	VDD3.3	GND	GND	GND	GND	GND	USBVSS1	USBVSSA3.3	VDD3.3	USB1VDD1.2	P1_TXEN	P1_TXC	P1_TXD1	P1_TXD2	P1_TXD0
K	SADDR22	SADDR21	RCSN1	SDATA0	SDATA7	VDD3.3	GND	GND	GND	GND	GND	GND	USBVSSA3.3	VDD3.3	VDD3.3	P1_RXDV	P1_RXER	P1_CRS	P1_RXC	P1_COL
L	RCSN0	SADDR23	ECS2	SDATA3	SDATA13	PLLVDDA3.3	GND	PLLVSSISO	GND	GND	GND	GND	GND	GND	VDD3.3	P0_TXEN	P0_TXD3	P1_RXD1	P1_RXD2	P1_RXD3
M	EROEN	ECS0	SDATA2	SDATA8	PLLSVDD1.2	VDD1.2	VDD1.2	PLLVSSA3.3	GND	GND	GND	GND	GND	VDD1.2	VDD1.2	P0_RXC	P0_CRS	P0_TXC	P0_TXD2	P1_RXD0
N	ECS1	EWAITN	SDATA6	SDATA12	WRSTO	VDD1.2	PLLVSS1.2	PLLVSS1.2	GND	GND	GND	GND	GND	VDD1.2	U3TXD	P0_RXD0	P0_RXD2	P0_RXDV	P0_TXD0	P0_TXD1
P	SDATA1	SDATA5	SDATA11	NRBN1	SCANEN	PLLDVDD1.2	GND	GND	GND	GND	VDD1.2	VDD1.2	VDD1.2	VDD1.2	U1DSRN	U1RXD	P0_RXD1	P0_RXD3	P0_RXER	P0_COL
R	SDATA4	SDATA10	NCLE	NREN	RESETN	VDD2.5	VDD2.5	VDD2.5	VDD2.5	VDD2.5	VDD2.5	VDD2.5	VDD2.5	VDD2.5	U2RXD	U1TXD	U2TXD	U3RXD	U1CTSN	U1DCDN
T	SDATA9	SDATA15	NCEN1	NWEN	DATA3	DM0	VREF	VDD2.5	VDD2.5	VDD2.5	VDD2.5	DM3	BA1	RASN	ADDR2	ADDR10	ADDR13	GPIO2/EINT2	U4RXD	U4TXD
U	SDATA14	NALE	NWPN	NRBN0	DATA4	DQS0	VREF	DM1	DATA20	DATA24	DATA30	DQS3	CKE	CS0N	CASN	ADDR3	ADDR11	GPIO0/EINT0	GPIO4/TOUT0	GPIO5/TOUT1
V	TESTEN1	TESTEN	NCEN0	DATA1	DATA6	DATA8	DATA11	DQS1	DATA18	DATA23	DATA25	DATA29	DATA31	BA0	WEN	ADDR0	ADDR4	ADDR12	GPIO1/EINT1	GPIO3/EINT3
W	XCLK2	TEST2	SDOCLK	DATA0	DATA5	DATA9	DATA12	DATA15	DATA17	DATA21	DQS2	DATA26	DATA28	CLK0N	CLK1N	CLK2N	CLK3N	ADDR5	ADDR8	ADDR9
Y	XCLK1	TEST1	SDICLK	DATA2	DATA7	DATA10	DATA13	DATA14	DATA16	DATA19	DATA22	DM2	DATA27	CLK0	CLK1	CLK2	CLK3	ADDR1	ADDR6	ADDR7

Power - 1.2V (digital & analog)
PCI
Strap/Reset/XTAL Signals
ROM/SRAM/NAND
DDR

Power - 3.3V (digital & analog)
USB
GPIO
Ethernet

VDD2.5
UART
I2S
I2C/SPI
SDIO

JTAG
Test
GND

Figure 20. Ball Grid Array Map

Package Information

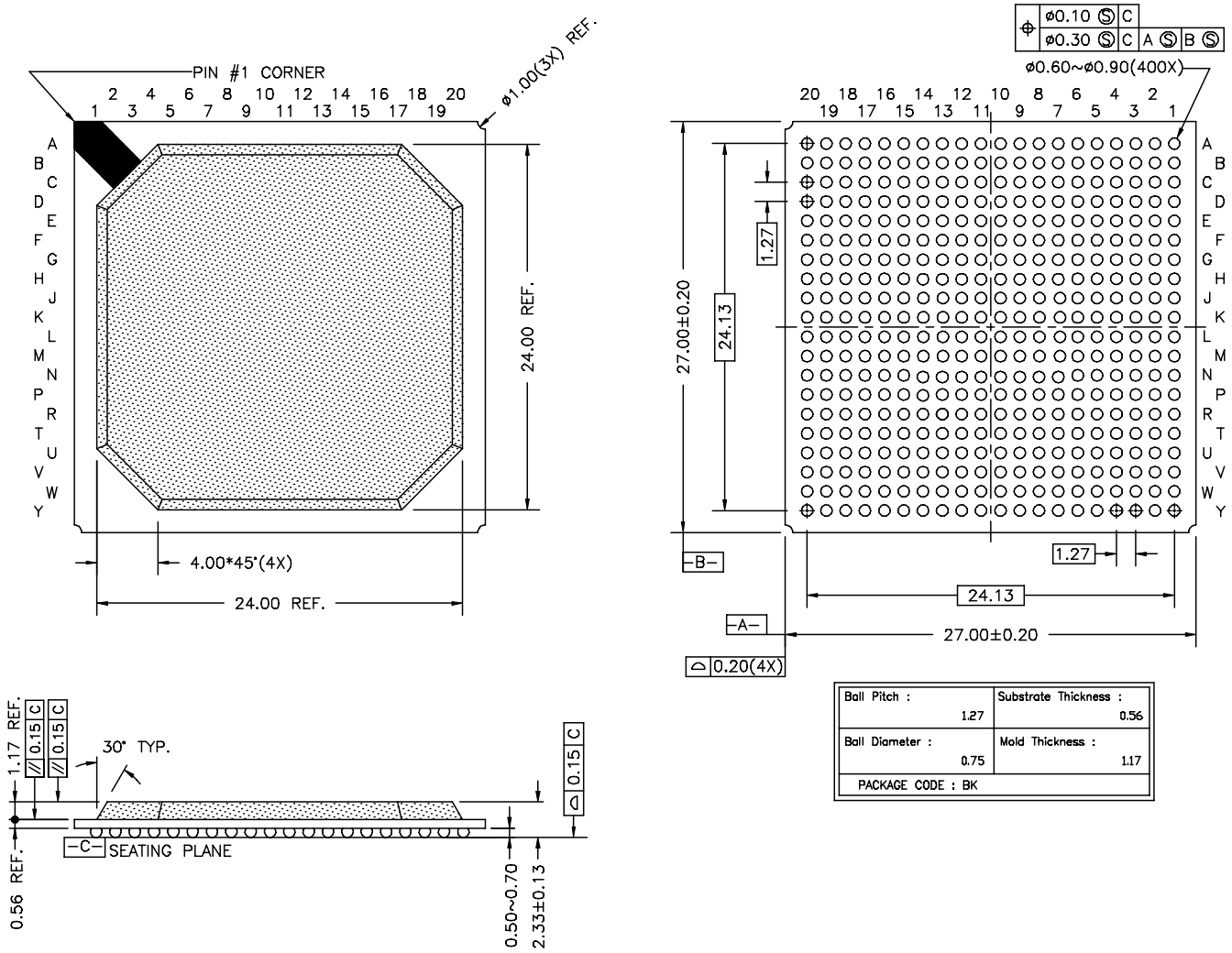

Figure 21. KSZ9692PB 400-Pin PBGA (24X24X2.33 MM)