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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	8375
Number of Logic Elements/Cells	67000
Total RAM Bits	4526080
Number of I/O	295
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-70e-6fn484i

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, please refer to TN1179, LatticeECP3 Memory Usage Guide.

Routing

There are many resources provided in the LatticeECP3 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The LatticeECP3 family has an enhanced routing architecture that produces a compact design. The ispLEVER design tool suite takes the output of the synthesis tool and places and routes the design.

sysCLOCK PLLs and DLLs

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. All the devices in the LatticeECP3 family support four to ten full-featured General Purpose PLLs.

General Purpose PLL

The architecture of the PLL is shown in Figure 2-4. A description of the PLL functionality follows.

CLKI is the reference frequency (generated either from the pin or from routing) for the PLL. CLKI feeds into the Input Clock Divider block. The CLKFB is the feedback signal (generated from CLKOP, CLKOS or from a user clock pin/logic). This signal feeds into the Feedback Divider. The Feedback Divider is used to multiply the reference frequency.

Both the input path and feedback signals enter the Voltage Controlled Oscillator (VCO) block. In this block the difference between the input path and feedback signals is used to control the frequency and phase of the oscillator. A LOCK signal is generated by the VCO to indicate that the VCO has locked onto the input clock signal. In dynamic mode, the PLL may lose lock after a dynamic delay adjustment and not relock until the t_{LOCK} parameter has been satisfied.

The output of the VCO then enters the CLKOP divider. The CLKOP divider allows the VCO to operate at higher frequencies than the clock output (CLKOP), thereby increasing the frequency range. The Phase/Duty Select block adjusts the phase and duty cycle of the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted. A secondary divider takes the CLKOP or CLKOS signal and uses it to derive lower frequency outputs (CLKOK).

The primary output from the CLKOP divider (CLKOP) along with the outputs from the secondary dividers (CLKOK and CLKOK2) and Phase/Duty select (CLKOS) are fed to the clock distribution network.

The PLL allows two methods for adjusting the phase of signal. The first is referred to as Fine Delay Adjustment. This inserts up to 16 nominal 125ps delays to be applied to the secondary PLL output. The number of steps may be set statically or from the FPGA logic. The second method is referred to as Coarse Phase Adjustment. This allows the phase of the rising and falling edge of the secondary PLL output to be adjusted in 22.5 degree steps. The number of steps may be set statically or from the FPGA logic.

Figure 2-20. Sources of Edge Clock (Left and Right Edges)
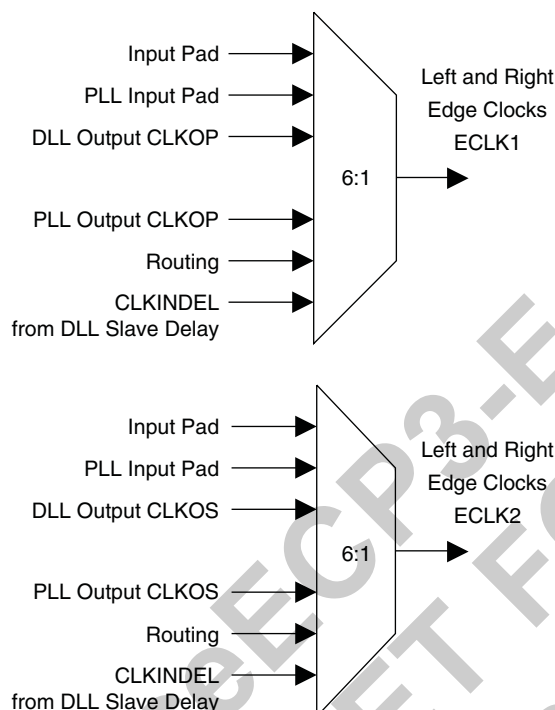
Figure 2-21. Sources of Edge Clock (Top Edge)
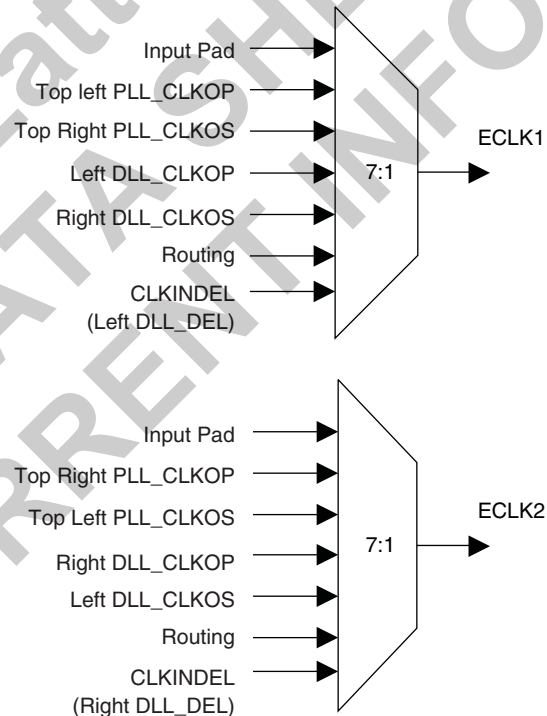
The edge clocks have low injection delay and low skew. They are used to clock the I/O registers and thus are ideal for creating I/O interfaces with a single clock signal and a wide data bus. They are also used for DDR Memory or Generic DDR interfaces.

Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports the following forms of write behavior for single port or dual port operation:

1. **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

2. **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.

3. **Read-Before-Write (EA devices only)** – When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2-22.

Figure 2-22. Memory Core Reset
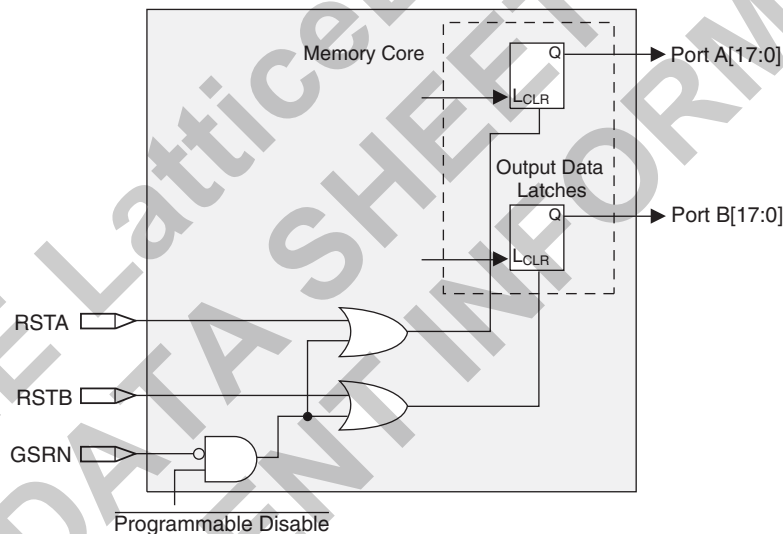
For further information on the sysMEM EBR block, please see the list of technical documentation at the end of this data sheet.

sysDSP™ Slice

The LatticeECP3 family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP3, on the other hand, has many DSP slices that support different data widths.

ALU Flags

The sysDSP slice provides a number of flags from the ALU including:

- Equal to zero (EQZ)

- Equal to zero with mask (EQZM)

- Equal to one with mask (EQOM)

- Equal to pattern with mask (EQPAT)

- Equal to bit inverted pattern with mask (EQPATB)

- Accumulator Overflow (OVER)

- Accumulator Underflow (UNDER)

- Either over or under flow supporting LatticeECP2 legacy designs (OVERUNDER)

Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every sysDSP slice. From four clock sources (CLK0, CLK1, CLK2, and CLK3) one clock is selected for each input register, pipeline register and output register. Similarly Clock Enable (CE) and Reset (RST) are selected at each input register, pipeline register and output register.

Resources Available in the LatticeECP3 Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP3 family. Table 2-10 shows the maximum available EBR RAM Blocks in each LatticeECP3 device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Table 2-9. Maximum Number of DSP Slices in the LatticeECP3 Family

Device	DSP Slices	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
ECP3-17	12	48	24	6
ECP3-35	32	128	64	16
ECP3-70	64	256	128	32
ECP3-95	64	256	128	32
ECP3-150	160	640	320	80

Table 2-10. Embedded SRAM in the LatticeECP3 Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
ECP3-17	38	700
ECP3-35	72	1327
ECP3-70	240	4420
ECP3-95	240	4420
ECP3-150	372	6850

The ispLEVER design tools from Lattice support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With ispLEVER, the user can define the mode for each quad in a design.

Popular standards such as 10Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), a single quad (Four SERDES channels and PCS) and some additional logic from the core.

The LatticeECP3 family also supports a wide range of primary and secondary protocols. Within the same quad, the LatticeECP3 family can support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. Table 2-15 lists the allowable combination of primary and secondary protocol combinations.

Flexible Quad SERDES Architecture

The LatticeECP3 family SERDES architecture is a quad-based architecture. For most SERDES settings and standards, the whole quad (consisting of four SERDES) is treated as a unit. This helps in silicon area savings, better utilization and overall lower cost.

However, for some specific standards, the LatticeECP3 quad architecture provides flexibility; more than one standard can be supported within the same quad.

Table 2-15 shows the standards can be mixed and matched within the same quad. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same quad. In Table 2-15, the Primary Protocol column refers to the standard that determines the reference clock and PLL settings. The Secondary Protocol column shows the other standard that can be supported within the same quad.

Furthermore, Table 2-15 also implies that more than two standards in the same quad can be supported, as long as they conform to the data rate and reference clock requirements. For example, a quad may contain PCI Express 1.1, SGMII, Serial RapidIO Type I and Serial RapidIO Type II, all in the same quad.

Table 2-15. LatticeECP3 Primary and Secondary Protocol Support

Primary Protocol	Secondary Protocol
PCI Express 1.1	SGMII
PCI Express 1.1	Gigabit Ethernet
PCI Express 1.1	Serial RapidIO Type I
PCI Express 1.1	Serial RapidIO Type II
Serial RapidIO Type I	SGMII
Serial RapidIO Type I	Gigabit Ethernet
Serial RapidIO Type II	SGMII
Serial RapidIO Type II	Gigabit Ethernet
Serial RapidIO Type II	Serial RapidIO Type I
CPRI-3	CPRI-2 and CPRI-1
3G-SDI	HD-SDI and SD-SDI

For further information on SERDES, please see TN1176, LatticeECP3 SERDES/PCS Usage Guide.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeECP3 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test

access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards.

For more information, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

Device Configuration

All LatticeECP3 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support dual-byte, byte and serial configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. The sysCONFIG port includes seven I/Os used as dedicated pins with the remaining pins used as dual-use pins. See TN1169, LatticeECP3 sysCONFIG Usage Guide for more information about using the dual-use pins as general purpose I/Os.

There are various ways to configure a LatticeECP3 device:

1. JTAG

2. Standard Serial Peripheral Interface (SPI and SPIm modes) - interface to boot PROM memory

3. System microprocessor to drive a x8 CPU port (PCM mode)

4. System microprocessor to drive a serial slave SPI port (SSPI mode)

5. Generic byte wide flash with a MachXO™ device, providing control and addressing

On power-up, the FPGA SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port.

LatticeECP3 devices also support the Slave SPI Interface. In this mode, the FPGA behaves like a SPI Flash device (slave mode) with the SPI port of the FPGA to perform read-write operations.

Enhanced Configuration Options

LatticeECP3 devices have enhanced configuration features such as: decryption support, TransFR™ I/O and dual-boot image support.

1. **TransFR (Transparent Field Reconfiguration)**
   TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. See TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

2. **Dual-Boot Image Support**
   Dual-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LatticeECP3 can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the LatticeECP3 device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

Soft Error Detect (SED) Support

LatticeECP3 devices have dedicated logic to perform Cycle Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, the LatticeECP3 device

can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode (normal operation) the device can be programmed to generate an error signal.

For further information on SED support, please see TN1184, LatticeECP3 Soft Error Detection (SED) Usage Guide.

External Resistor

LatticeECP3 devices require a single external, 10K ohm ±1% value between the XRES pin and ground. Device configuration will not be completed if this resistor is missing. There is no boundary scan register on the external resistor pad.

On-Chip Oscillator

Every LatticeECP3 device has an internal CMOS oscillator which is used to derive a Master Clock (MCLK) for configuration. The oscillator and the MCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCLK is nominally 2.5MHz. Table 2-16 lists all the available MCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 3.1MHz.

2. During configuration, users select a different master clock frequency.

3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.

4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.5MHz.

This internal CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

Table 2-16. Selectable Master Clock (MCLK) Frequencies During Configuration (Nominal)

MCLK (MHz)	MCLK (MHz)	MCLK (MHz)
2.5[1]	10	41
3.1	13	45
4.3	15	51
5.4	20	55
6.9	26	60
8.1	30	130
9.2	34	—

1. Software default MCLK frequency. Hardware default is 3.1MHz.

Density Shifting

The LatticeECP3 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same packge.

LatticeECP3 Maximum I/O Buffer Speed (Continued)[1, 2, 3, 4, 5, 6]

Over Recommended Operating Conditions

Buffer	Description	Max.	Units
PCI33	PCI, V_{CCIO} = 3.3V	66	MHz

1. These maximum speeds are characterized but not tested on every device.
2. Maximum I/O speed for differential output standards emulated with resistors depends on the layout.
3. LVCMOS timing is measured with the load specified in the Switching Test Conditions table of this document.
4. All speeds are measured at fast slew.
5. Actual system operation may vary depending on user logic implementation.
6. Maximum data rate equals 2 times the clock rate when utilizing DDR.

SERDES High-Speed Data Transmitter[1]

Table 3-6. Serial Output Timing and Levels

Symbol	Description	Frequency	Min.	Typ.	Max.	Units
$V_{TX-DIFF-P-P-1.44}$	Differential swing (1.44V setting)[1,2]	0.25 to 3.125 Gbps	1150	1440	1730	mV, p-p
$V_{TX-DIFF-P-P-1.35}$	Differential swing (1.35V setting)[1,2]	0.25 to 3.125 Gbps	1080	1350	1620	mV, p-p
$V_{TX-DIFF-P-P-1.26}$	Differential swing (1.26V setting)[1,2]	0.25 to 3.125 Gbps	1000	1260	1510	mV, p-p
$V_{TX-DIFF-P-P-1.13}$	Differential swing (1.13V setting)[1,2]	0.25 to 3.125 Gbps	840	1130	1420	mV, p-p
$V_{TX-DIFF-P-P-1.04}$	Differential swing (1.04V setting)[1,2]	0.25 to 3.125 Gbps	780	1040	1300	mV, p-p
$V_{TX-DIFF-P-P-0.92}$	Differential swing (0.92V setting)[1,2]	0.25 to 3.125 Gbps	690	920	1150	mV, p-p
$V_{TX-DIFF-P-P-0.87}$	Differential swing (0.87V setting)[1,2]	0.25 to 3.125 Gbps	650	870	1090	mV, p-p
$V_{TX-DIFF-P-P-0.78}$	Differential swing (0.78V setting)[1,2]	0.25 to 3.125 Gbps	585	780	975	mV, p-p
$V_{TX-DIFF-P-P-0.64}$	Differential swing (0.64V setting)[1,2]	0.25 to 3.125 Gbps	480	640	800	mV, p-p
V_{OCM}	Output common mode voltage	—	V_{CCOB} -0.75	V_{CCOB} -0.60	V_{CCOB} -0.45	V
T_{TX-R}	Rise time (20% to 80%)	—	145	185	265	ps
T_{TX-F}	Fall time (80% to 20%)	—	145	185	265	ps
$Z_{TX-OI-SE}$	Output Impedance 50/75/HiZ Ohms (single ended)	—	-20%	50/75/ Hi Z	+20%	Ohms
R_{LTX-RL}	Return loss (with package)	—	10			dB
$T_{TX-INTRASKEW}$	Lane-to-lane TX skew within a SERDES quad block (intra-quad)	—	—	—	200	ps
$T_{TX-INTERSKEW}$[3]	Lane-to-lane skew between SERDES quad blocks (inter-quad)	—	—	—	1UI +200	ps

1. All measurements are with 50 ohm impedance.
2. See TN1176, LatticeECP3 SERDES/PCS Usage Guide for actual binary settings and the min-max range.
3. Inter-quad skew is between all SERDES channels on the device and requires the use of a low skew internal reference clock.

Table 3-7. Channel Output Jitter

Description	Frequency	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	—	—	0.17	UI, p-p
Random	3.125 Gbps	—	—	0.25	UI, p-p
Total	3.125 Gbps	—	—	0.35	UI, p-p
Deterministic	2.5Gbps	—	—	0.17	UI, p-p
Random	2.5Gbps	—	—	0.20	UI, p-p
Total	2.5Gbps	—	—	0.35	UI, p-p
Deterministic	1.25 Gbps	—	—	0.10	UI, p-p
Random	1.25 Gbps	—	—	0.22	UI, p-p
Total	1.25 Gbps	—	—	0.24	UI, p-p
Deterministic	622 Mbps	—	—	0.10	UI, p-p
Random	622 Mbps	—	—	0.20	UI, p-p
Total	622 Mbps	—	—	0.24	UI, p-p
Deterministic	250 Mbps	—	—	0.10	UI, p-p
Random	250 Mbps	—	—	0.18	UI, p-p
Total	250 Mbps	—	—	0.24	UI, p-p

Note: Values are measured with PRBS 2^7-1, all channels operating, FPGA logic active, I/Os around SERDES pins quiet, reference clock @ 10X mode.

SERDES External Reference Clock

The external reference clock selection and its interface are a critical part of system applications for this product. Table 3-12 specifies reference clock requirements, over the full range of operating conditions.

Table 3-12. External Reference Clock Specification (refclkp/refclkn)

Symbol	Description	Min.	Typ.	Max.	Units
F_{REF}	Frequency range	15	—	320	MHz
$F_{REF-PPM}$	Frequency tolerance[4]	-1000	—	1000	ppm
$V_{REF-IN-SE}$	Input swing, single-ended clock[1]	200	—	V_{CCA}	mV, p-p
$V_{REF-IN-DIFF}$	Input swing, differential clock	200	—	$2*V_{CCA}$	mV, p-p differential
V_{REF-IN}	Input levels	0	—	$V_{CCA} + 0.3$	V
$V_{REF-CM-AC}$	Input common mode range (AC coupled)[2]	0.125	—	V_{CCA}	V
D_{REF}	Duty cycle[3]	40	—	60	%
T_{REF-R}	Rise time (20% to 80%)	200	500	1000	ps
T_{REF-F}	Fall time (80% to 20%)	200	500	1000	ps
$Z_{REF-IN-TERM-DIFF}$	Differential input termination	-20%	100/2K	+20%	Ohms
$C_{REF-IN-CAP}$	Input capacitance	—	—	7	pF

1. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.
2. When AC coupled, the input common mode range is determined by:
   (Min input level) + (Peak-to-peak input swing)/2 ≤ (Input common mode voltage) ≤ (Max input level) - (Peak-to-peak input swing)/2
3. Measured at 50% amplitude.
4. Depending on the application, the PLL_LOL_SET and CDR_LOL_SET control registers may be adjusted for other tolerance values as described in TN1176, LatticeECP3 SERDES/PCS Usage Guide.

Figure 3-13. SERDES External Reference Clock Waveforms
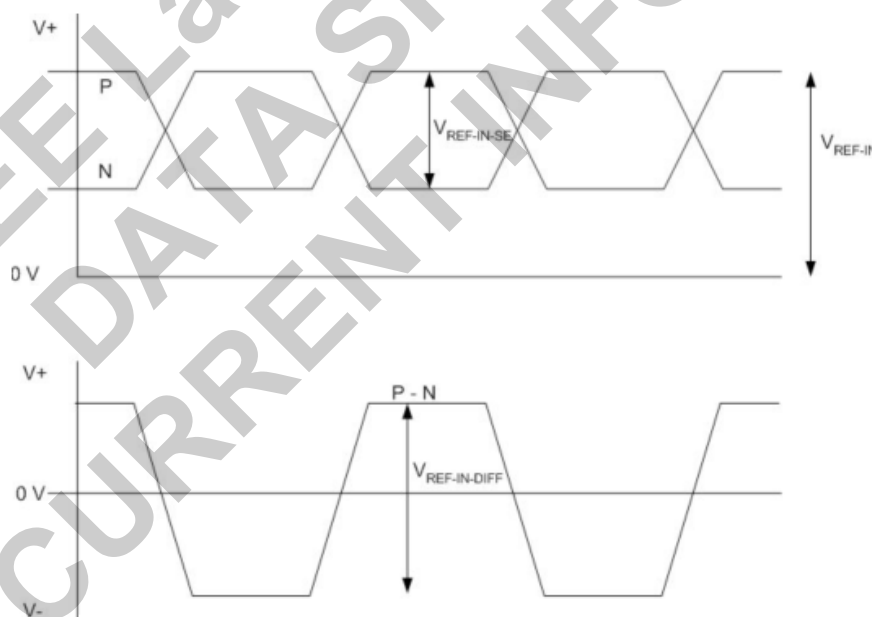
XAUI/Serial Rapid I/O Type 3 Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-13. Transmit

Over Recommended Operating Conditions

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
T_{RF}	Differential rise/fall time	20%-80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential impedance		80	100	120	Ohms
J_{TX_DDJ}[2, 3, 4]	Output data deterministic jitter		—	—	0.17	UI
J_{TX_TJ}[1, 2, 3, 4]	Total output data jitter		—	—	0.35	UI

1. Total jitter includes both deterministic jitter and random jitter.
2. Jitter values are measured with each CML output AC coupled into a 50-ohm impedance (100-ohm differential impedance).
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Values are measured at 2.5 Gbps.

Table 3-14. Receive and Jitter Tolerance

Over Recommended Operating Conditions

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
RL_{RX_DIFF}	Differential return loss	From 100 MHz to 3.125 GHz	10	—	—	dB
RL_{RX_CM}	Common mode return loss	From 100 MHz to 3.125 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential termination resistance		80	100	120	Ohms
J_{RX_DJ}[1, 2, 3]	Deterministic jitter tolerance (peak-to-peak)		—	—	0.37	UI
J_{RX_RJ}[1, 2, 3]	Random jitter tolerance (peak-to-peak)		—	—	0.18	UI
J_{RX_SJ}[1, 2, 3]	Sinusoidal jitter tolerance (peak-to-peak)		—	—	0.10	UI
J_{RX_TJ}[1, 2, 3]	Total jitter tolerance (peak-to-peak)		—	—	0.65	UI
T_{RX_EYE}	Receiver eye opening		0.35	—	—	UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-14.
2. Jitter values are measured with each high-speed input AC coupled into a 50-ohm impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance parameters are characterized when Full Rx Equalization is enabled.
5. Values are measured at 2.5 Gbps.

Figure 3-24. Master SPI Configuration Waveforms
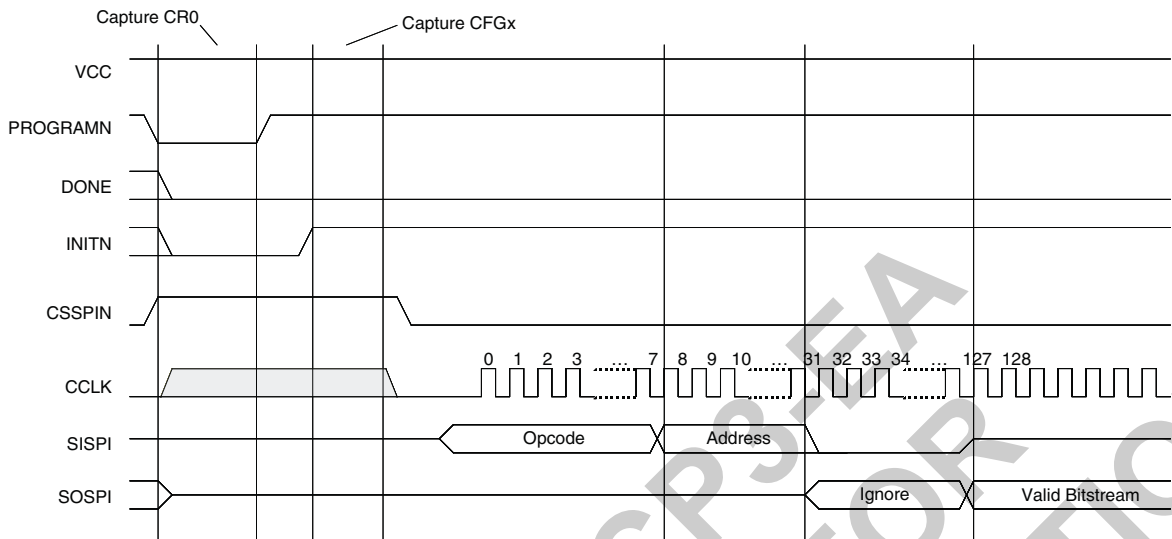
JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
f$_{MAX}$	TCK clock frequency	—	25	MHz
t$_{BTCP}$	TCK [BSCAN] clock pulse width	40	—	ns
t$_{BTCPH}$	TCK [BSCAN] clock pulse width high	20	—	ns
t$_{BTCPL}$	TCK [BSCAN] clock pulse width low	20	—	ns
t$_{BTS}$	TCK [BSCAN] setup time	10	—	ns
t$_{BTH}$	TCK [BSCAN] hold time	8	—	ns
t$_{BTRF}$	TCK [BSCAN] rise/fall time	50	—	mV/ns
t$_{BTCO}$	TAP controller falling edge of clock to valid output	—	10	ns
t$_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t$_{BTCOEN}$	TAP controller falling edge of clock to valid enable	—	10	ns
t$_{BTCRS}$	BSCAN test capture register setup time	8	—	ns
t$_{BTCRH}$	BSCAN test capture register hold time	25	—	ns
t$_{BUTCO}$	BSCAN test update register, falling edge of clock to valid output	—	25	ns
t$_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
t$_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Figure 3-25. JTAG Port Timing Waveforms
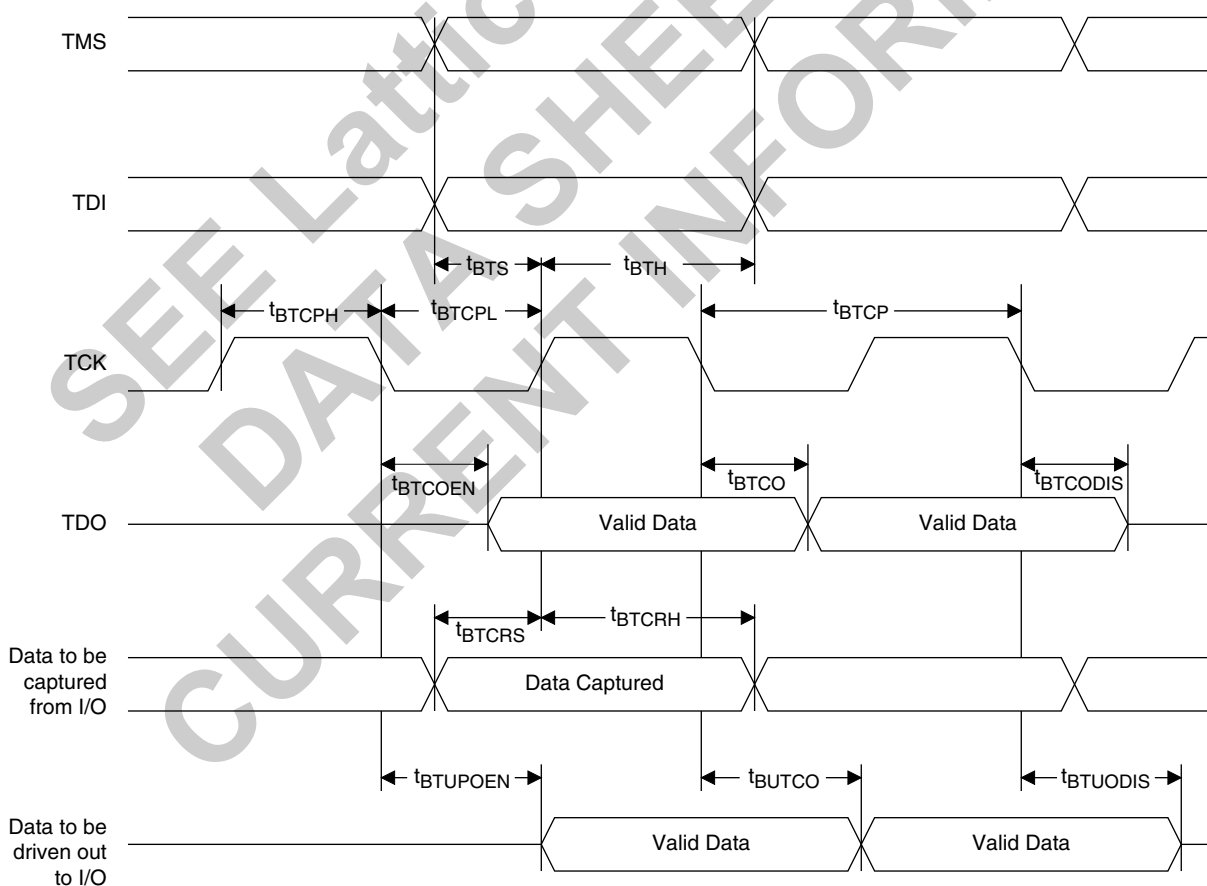
Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number]_[A/B]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or B (Bottom), only need to specify Column Number. When Edge is L (Left) or R (Right), only need to specify Row Number. [A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
P[Edge][Row Number]E_[A/B/C/D]	I	These general purpose signals are input-only pins and are located near the PLLs.
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
RESERVED	—	This pin is reserved and should not be connected to anything on the board.
GND	—	Ground. Dedicated pins.
V_{CC}	—	Power supply pins for core logic. Dedicated pins.
V_{CCAUX}	—	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers.
V_{CCIOx}	—	Dedicated power supply pins for I/O bank x.
V_{CCA}	—	SERDES, transmit, receive, PLL and reference clock buffer power supply.
$V_{CCPLL\_[LOC]}$	—	General purpose PLL supply pins where LOC=L (left) or R (right).
V_{REF1_x}, V_{REF2_x}	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V_{REF} inputs. When not used, they may be used as I/O pins.
VTTx	—	Power supply for on-chip termination of I/Os (Required for DDR3 and LVDS at 1.25Gbps).
XRES[1]	—	10K ohm +/-1% resistor must be connected between this pad and ground.
PLL, DLL and Clock Functions		
[LOC][num]_GPLL[T, C]_IN_[index]	I	General Purpose PLL (GPLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_GPLL[T, C]_FB_[index]	I	Optional feedback GPLL input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC]0_GDLLT_IN_[index]	I/O	General Purpose DLL (GDLL) input pads where LOC=RUM or LUM, T is True Complement, index is A or B.
[LOC]0_GDLLT_FB_[index]	I/O	Optional feedback GDLL input pads where LOC=RUM or LUM, T is True Complement, index is A or B.
PCLK[T, C][n:0]_[3:0]	I	Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0, 1, 2, 3 within bank.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
D7/SPID0	I/O	Parallel configuration I/O. SPI/SPIm data input. Open drain during configuration.
DI/CSSPI0N/CEN	I/O	Serial data input for slave serial mode. SPI/SPIm mode chip select.
Dedicated SERDES Signals[2]		
PCS[Index]_HDINNm	I	High-speed input, negative channel m
PCS[Index]_HDOUTNm	O	High-speed output, negative channel m
PCS[Index]_REFCLKN	I	Negative Reference Clock Input
PCS[Index]_HDINPm	I	High-speed input, positive channel m
PCS[Index]_HDOUTPm	O	High-speed output, positive channel m
PCS[Index]_REFCLKP	I	Positive Reference Clock Input
PCS[Index]_VCCOBm	—	Output buffer power supply, channel m (1.2V/1.5)
PCS[Index]_VCCIBm	—	Input buffer power supply, channel m (1.2V/1.5V)

1. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given.
2. m defines the associated channel in the quad.

Pin Information Summary

Pin Information Summary		ECP3-17EA		ECP3-35EA			ECP3-70E/EA		
Pin Type		256 ftBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA	1156 fpBGA
General Purpose Inputs/Outputs per Bank	Bank 0	26	36	26	42	48	42	60	86
	Bank 1	14	24	14	36	36	36	48	78
	Bank 2	6	12	6	24	24	24	34	36
	Bank 3	18	44	16	54	59	54	59	86
	Bank 6	20	44	18	63	61	63	67	86
	Bank 7	19	32	19	36	42	36	48	54
	Bank 8	24	24	24	24	24	24	24	24
General Purpose Inputs per Bank	Bank 0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0
	Bank 2	2	2	2	4	4	4	8	8
	Bank 3	0	0	2	4	4	4	12	12
	Bank 6	0	0	2	4	4	4	12	12
	Bank 7	4	4	4	4	4	4	8	8
	Bank 8	0	0	0	0	0	0	0	0
General Purpose Outputs per Bank	Bank 0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0
	Bank 2	0	0	0	0	0	0	0	0
	Bank 3	0	0	0	0	0	0	0	0
	Bank 6	0	0	0	0	0	0	0	0
	Bank 7	0	0	0	0	0	0	0	0
	Bank 8	0	0	0	0	0	0	0	0
Total Single-Ended User I/O		133	222	133	295	310	295	380	490
VCC		6	16	6	16	32	16	32	32
VCCAUX		4	8	4	8	12	8	12	16
VTT		4	4	4	4	4	4	4	8
VCCA		4	4	4	4	8	4	8	16
VCCPLL		2	4	2	4	4	4	4	4
VCCIO	Bank 0	2	2	2	2	4	2	4	4
	Bank 1	2	2	2	2	4	2	4	4
	Bank 2	2	2	2	2	4	2	4	4
	Bank 3	2	2	2	2	4	2	4	4
	Bank 6	2	2	2	2	4	2	4	4
	Bank 7	2	2	2	2	4	2	4	4
	Bank 8	2	2	2	2	2	2	2	2
VCCJ		1	1	1	1	1	1	1	1
TAP		4	4	4	4	4	4	4	4
GND, GNDIO		50	98	50	98	139	98	139	233
NC		0	73	0	0	96	0	0	238
Reserved[1]		0	2	0	2	2	2	2	2
SERDES		26	26	26	26	26	26	52	78
Miscellaneous Pins		8	8	8	8	8	8	8	8
Total Bonded Pins		256	484	256	484	672	484	672	1156

Pin Information Summary (Cont.)

Pin Information Summary		ECP3-70E			ECP3-70EA		
Pin Type		484 fpBGA	672 fpBGA	1156 fpBGA	484 fpBGA	672 fpBGA	1156 fpBGA
Emulated Differential I/O per Bank	Bank 0	21	30	43	21	30	43
	Bank 1	18	24	39	18	24	39
	Bank 2	10	15	16	8	12	13
	Bank 3	23	27	39	20	23	33
	Bank 6	26	30	39	22	25	33
	Bank 7	14	20	22	11	16	18
	Bank 8	12	12	12	12	12	12
High-Speed Differential I/O per Bank	Bank 0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0
	Bank 2	4	6	6	6	9	9
	Bank 3	6	8	10	9	12	16
	Bank 6	7	9	10	11	14	16
	Bank 7	6	8	9	9	12	13
	Bank 8	0	0	0	0	0	0
Total Single-Ended/ Total Differential I/O per Bank	Bank 0	42/21	60/30	86/43	42/21	60/30	86/43
	Bank 1	36/18	48/24	78/39	36/18	48/24	78/39
	Bank 2	28/14	42/21	44/22	28/14	42/21	44/22
	Bank 3	58/29	71/35	98/49	58/29	71/35	98/49
	Bank 6	67/33	79/38	98/49	67/33	78/39	98/49
	Bank 7	40/20	56/28	62/31	40/20	56/28	62/31
	Bank 8	24/12	24/12	24/12	24/12	24/12	24/12
DDR Groups Bonded per Bank	Bank 0	3	5	7	3	5	7
	Bank 1	3	4	7	3	4	7
	Bank 2	2	3	3	2	3	3
	Bank 3	3	4	5	3	4	5
	Bank 6	4	4	5	4	4	5
	Bank 7	3	4	4	3	4	4
	Configuration Bank 8	0	0	0	0	0	0
SERDES Quads		1	2	3	1	2	3

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-70E-6FN484C[1]	1.2V	-6	Lead-Free fpBGA	484	COM	67
LFE3-70E-7FN484C[1]	1.2V	-7	Lead-Free fpBGA	484	COM	67
LFE3-70E-8FN484C[1]	1.2V	-8	Lead-Free fpBGA	484	COM	67
LFE3-70E-6FN672C[1]	1.2V	-6	Lead-Free fpBGA	672	COM	67
LFE3-70E-7FN672C[1]	1.2V	-7	Lead-Free fpBGA	672	COM	67
LFE3-70E-8FN672C[1]	1.2V	-8	Lead-Free fpBGA	672	COM	67
LFE3-70E-6FN1156C[1]	1.2V	-6	Lead-Free fpBGA	1156	COM	67
LFE3-70E-7FN1156C[1]	1.2V	-7	Lead-Free fpBGA	1156	COM	67
LFE3-70E-8FN1156C[1]	1.2V	-8	Lead-Free fpBGA	1156	COM	67

1.This device has associated errata. View www.latticesemi.com/documents/ds1021.zip for a description of the errata.

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-95EA-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	92
LFE3-95EA-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	92
LFE3-95EA-8FN484C	1.2V	-8	Lead-Free fpBGA	484	COM	92
LFE3-95EA-6FN672C	1.2V	-6	Lead-Free fpBGA	672	COM	92
LFE3-95EA-7FN672C	1.2V	-7	Lead-Free fpBGA	672	COM	92
LFE3-95EA-8FN672C	1.2V	-8	Lead-Free fpBGA	672	COM	92
LFE3-95EA-6FN1156C	1.2V	-6	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-7FN1156C	1.2V	-7	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-8FN1156C	1.2V	-8	Lead-Free fpBGA	1156	COM	92

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-95E-6FN484C[1]	1.2V	-6	Lead-Free fpBGA	484	COM	92
LFE3-95E-7FN484C[1]	1.2V	-7	Lead-Free fpBGA	484	COM	92
LFE3-95E-8FN484C[1]	1.2V	-8	Lead-Free fpBGA	484	COM	92
LFE3-95E-6FN672C[1]	1.2V	-6	Lead-Free fpBGA	672	COM	92
LFE3-95E-7FN672C[1]	1.2V	-7	Lead-Free fpBGA	672	COM	92
LFE3-95E-8FN672C[1]	1.2V	-8	Lead-Free fpBGA	672	COM	92
LFE3-95E-6FN1156C[1]	1.2V	-6	Lead-Free fpBGA	1156	COM	92
LFE3-95E-7FN1156C[1]	1.2V	-7	Lead-Free fpBGA	1156	COM	92
LFE3-95E-8FN1156C[1]	1.2V	-8	Lead-Free fpBGA	1156	COM	92

1.This device has associated errata. View www.latticesemi.com/documents/ds1021.zip for a description of the errata.

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672C	1.2V	-6	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7FN672C	1.2V	-7	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8FN672C	1.2V	-8	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6FN1156C	1.2V	-6	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7FN1156C	1.2V	-7	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8FN1156C	1.2V	-8	Lead-Free fpBGA	1156	COM	149

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672I	1.2V	-6	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672I	1.2V	-7	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672I	1.2V	-8	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156I	1.2V	-6	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156I	1.2V	-7	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156I	1.2V	-8	Lead-Free fpBGA	1156	IND	149

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672ITW*	1.2V	-6	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672ITW*	1.2V	-7	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672ITW*	1.2V	-8	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156ITW*	1.2V	-6	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156ITW*	1.2V	-7	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156ITW*	1.2V	-8	Lead-Free fpBGA	1156	IND	149

*Note: Specifications for the LFE3-150EA-*sp*FN*pkg*CTW and LFE3-150EA-*sp*FN*pkg*ITW devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*sp*FN*pkg*C and LFE3-150EA-*sp*FN*pkg*I devices respectively, except as specified below.

- The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.
- The SERDES XRES pin on the TW device passes CDM testing at 250V.

Date	Version	Section	Change Summary
February 2009	01.0	—	Initial release.
May 2009	01.1	All	Removed references to Parallel burst mode Flash.
		Introduction	Features - Changed 250 Mbps to 230 Mbps in Embedded SERDES bulleted section and added a footnote to indicate 230 Mbps applies to 8b10b and 10b12b applications.
			Updated data for ECP3-17 in LatticeECP3 Family Selection Guide table.
			Changed embedded memory from 552 to 700 Kbits in LatticeECP3 Family Selection Guide table.
		Architecture	Updated description for CLKFB in General Purpose PLL Diagram.
			Corrected Primary Clock Sources text section.
			Corrected Secondary Clock/Control Sources text section.
			Corrected Secondary Clock Regions table.
			Corrected note below Detailed sysDSP Slice Diagram.
			Corrected Clock, Clock Enable, and Reset Resources text section.
			Corrected ECP3-17 EBR number in Embedded SRAM in the LatticeECP3 Family table.
			Added On-Chip Termination Options for Input Modes table.
			Updated Available SERDES Quads per LatticeECP3 Devices table.
			Updated Simplified Channel Block Diagram for SERDES/PCS Block diagram.
			Updated Device Configuration text section.
			Corrected software default value of MCLK to be 2.5 MHz.
		DC and Switching Characteristics	Updated VCCOB Min/Max data in Recommended Operating Conditions table.
			Corrected footnote 2 in sysIO Recommended Operating Conditions table.
			Added added footnote 7 for t_{SKEW_PRIB} to External Switching Characteristics table.
			Added 2-to-1 Gearing text section and table.
			Updated External Reference Clock Specification (refclkp/refclkn) table.
			LatticeECP3 sysCONFIG Port Timing Specifications - updated t_{DINIT} information.
			Added sysCONFIG Port Timing waveform.
			Serial Input Data Specifications table, delete Typ data for $V_{RX-DIFF-S}$.
			Added footnote 4 to sysCLOCK PLL Timing table for t_{PFD}.
			Added SERDES/PCS Block Latency Breakdown table.
			External Reference Clock Specifications table, added footnote 4, add symbol name vREF-IN-DIFF.
			Added SERDES External Reference Clock Waveforms.
			Updated Serial Output Timing and Levels table.
			Pin-to-pin performance table, changed "typically 3% slower" to "typically slower".