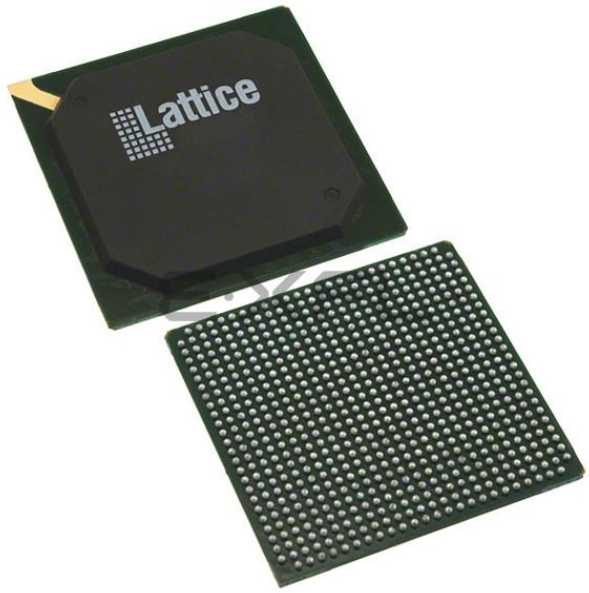


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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 8375 |
| Number of Logic Elements/Cells | 67000 |
| Total RAM Bits | 4526080 |
| Number of I/O | 380 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 672-BBGA |
| Supplier Device Package | 672-FPBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-70e-6fn672i |

# Introduction

The LatticeECP3™ (EConomy Plus Third generation) family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES and high speed source synchronous interfaces in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 65nm technology making the devices suitable for high-volume, high-speed, low-cost applications.

The LatticeECP3 device family expands look-up-table (LUT) capacity to 149K logic elements and supports up to 486 user I/Os. The LatticeECP3 device family also offers up to 320 18x18 multipliers and a wide range of parallel I/O standards.

The LatticeECP3 FPGA fabric is optimized with high performance and low cost in mind. The LatticeECP3 devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the LatticeECP3 device family supports a broad range of interface standards, including DDR3, XGMII and 7:1 LVDS.

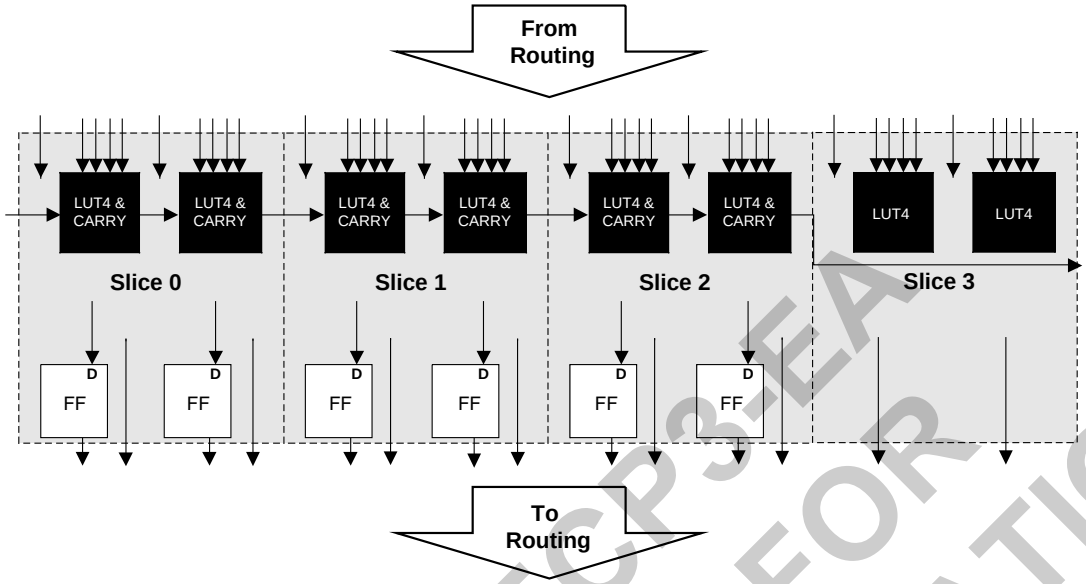
The LatticeECP3 device family also features high speed SERDES with dedicated PCS functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, SMPTE, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit Pre-emphasis and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The LatticeECP3 devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

The ispLEVER® design tool suite from Lattice allows large complex designs to be efficiently implemented using the LatticeECP3 FPGA family. Synthesis library support for LatticeECP3 is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP3 device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) ispLeverCORE™ modules for the LatticeECP3 family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

*Figure 2-2. PFU Diagram*




## Slice

Slice 0 through Slice 2 contain two LUT4s feeding two registers, whereas Slice 3 contains two LUT4s only. For PFUs, Slice 0 through Slice 2 can be configured as distributed memory, a capability not available in the PFF. Table 2-1 shows the capability of the slices in both PFF and PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

*Table 2-1. Resources and Modes Available per Slice*

| Slice | PFU BLock | | PFF Block | |
|---|---|---|---|---|
| | Resources | Modes | Resources | Modes |
| Slice 0 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |
| Slice 1 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |
| Slice 2 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |
| Slice 3 | 2 LUT4s | Logic, ROM | 2 LUT4s | Logic, ROM |

Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

Slices 0, 1 and 2 have 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to the adjacent PFU). Slice 3 has 10 input signals from routing and four signals to routing. Table 2-2 lists the signals associated with Slice 0 to Slice 2.

*Table 2-5. DLL Signals*

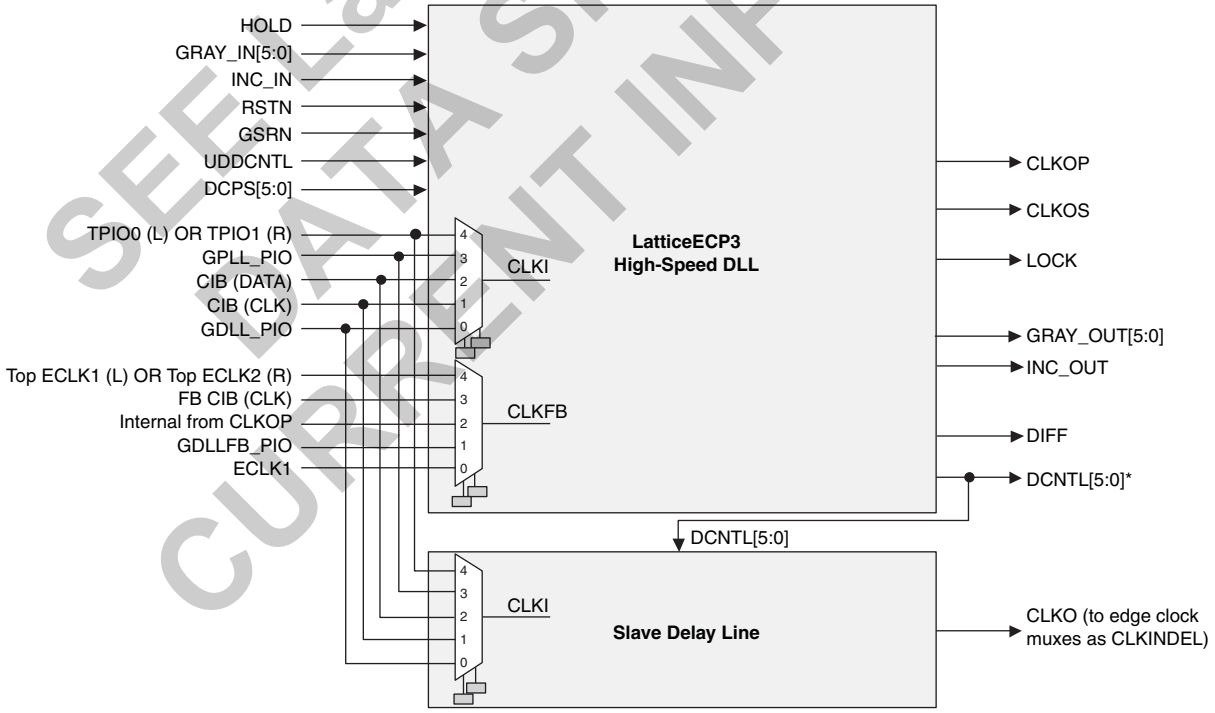
| Signal | I/O | Description |
|---|---|---|
| CLKI | I | Clock input from external pin or routing |
| CLKFB | I | DLL feed input from DLL output, clock net, routing or external pin |
| RSTN | I | Active low synchronous reset |
| ALUHOLD | I | Active high freezes the ALU |
| UDDCNTL | I | Synchronous enable signal (hold high for two cycles) from routing |
| CLKOP | O | The primary clock output |
| CLKOS | O | The secondary clock output with fine delay shift and/or division by 2 or by 4 |
| LOCK | O | Active high phase lock indicator |
| INCI | I | Incremental indicator from another DLL via CIB. |
| GRAYI[5:0] | I | Gray-coded digital control bus from another DLL in time reference mode. |
| DIFF | O | Difference indicator when DCNTL is difference than the internal setting and update is needed. |
| INCO | O | Incremental indicator to other DLLs via CIB. |
| GRAYO[5:0] | O | Gray-coded digital control bus to other DLLs via CIB |

LatticeECP3 devices have two general DLLs and four Slave Delay lines, two per DLL. The DLLs are in the lowest EBR row and located adjacent to the EBR. Each DLL replaces one EBR block. One Slave Delay line is placed adjacent to the DLL and the duplicate Slave Delay line (in Figure 2-6) for the DLL is placed in the I/O ring between Banks 6 and 7 and Banks 2 and 3.

The outputs from the DLL and Slave Delay lines are fed to the clock distribution network.

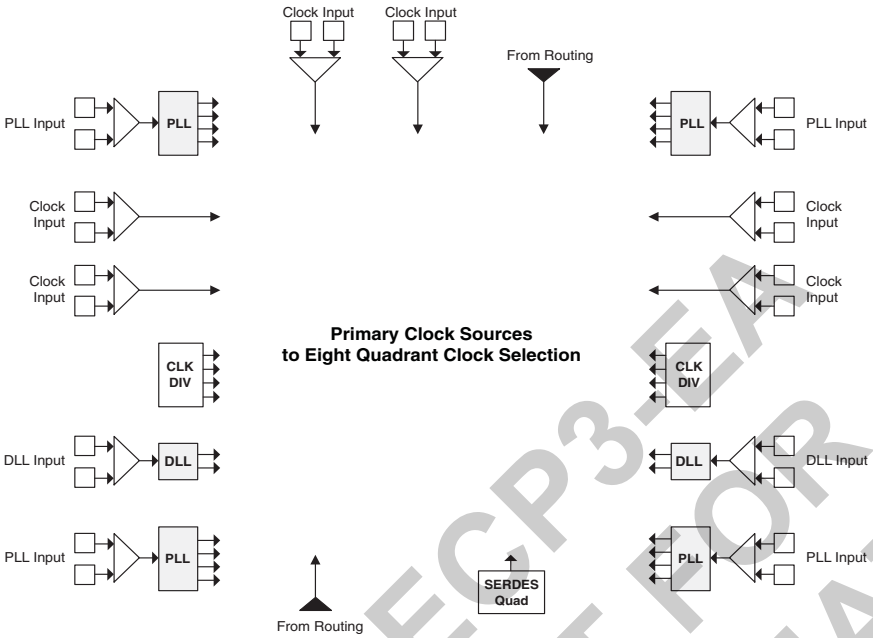
For more information, please see TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide.

*Figure 2-6. Top-Level Block Diagram, High-Speed DLL and Slave Delay Line*



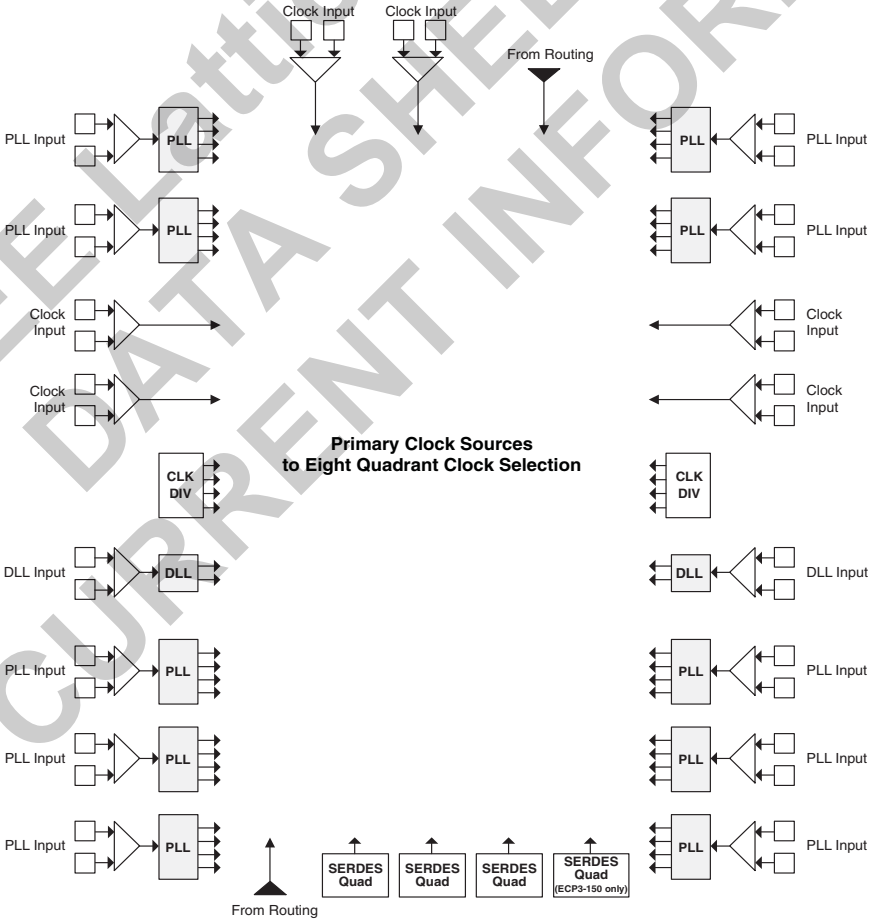

* This signal is not user accessible. It can only be used to feed the slave delay line.

*Figure 2-10. Primary Clock Sources for LatticeECP3-35*




Note: Clock inputs can be configured in differential or single-ended mode.

*Figure 2-11. Primary Clock Sources for LatticeECP3-70, -95, -150*

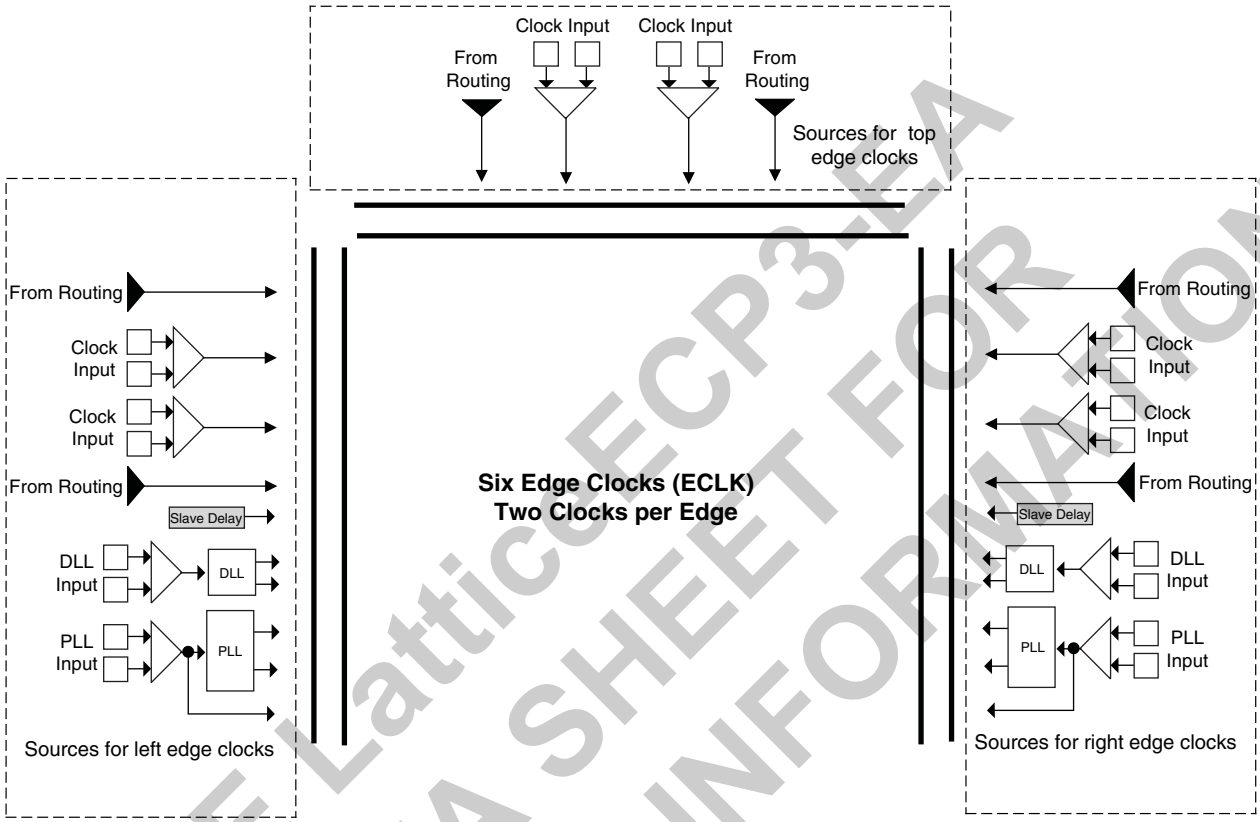



Note: Clock inputs can be configured in differential or single-ended mode.

## Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs, DLLs, Slave Delay and clock dividers as shown in Figure 2-19.

***Figure 2-19. Edge Clock Sources***



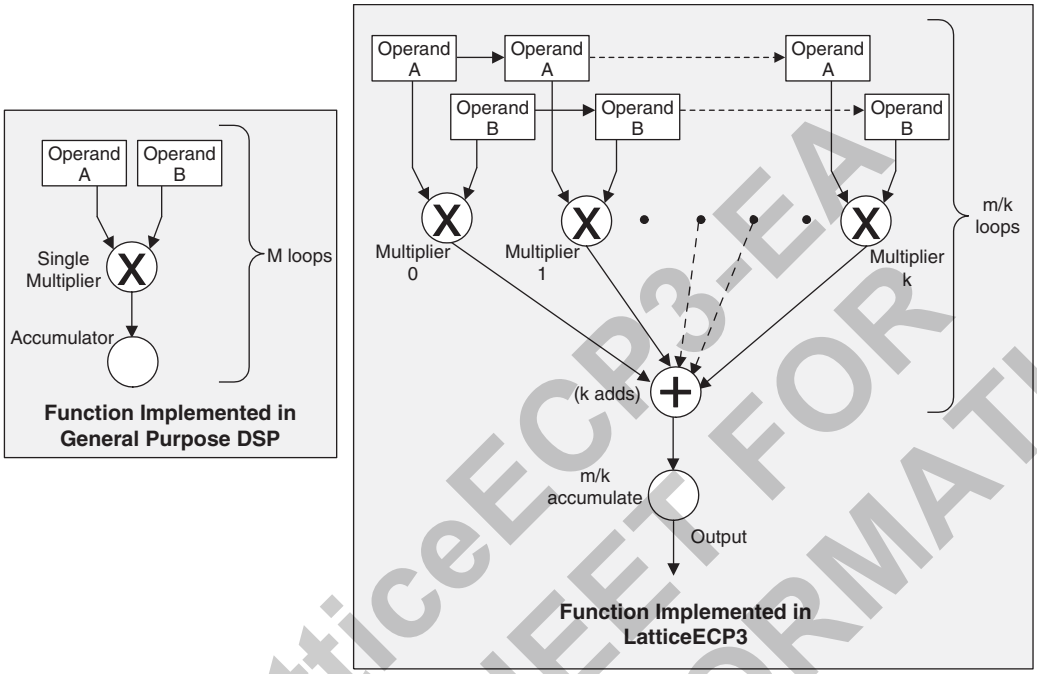

Notes:
1. Clock inputs can be configured in differential or single ended mode.
2. The two DLLs can also drive the two top edge clocks.
3. The top left and top right PLL can also drive the two top edge clocks.

## Edge Clock Routing

LatticeECP3 devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are six edge clocks per device: two edge clocks on each of the top, left, and right edges. Different PLL and DLL outputs are routed to the two muxes on the left and right sides of the device. In addition, the CLKINDEL signal (generated from the DLL Slave Delay Line block) is routed to all the edge clock muxes on the left and right sides of the device. Figure 2-20 shows the selection muxes for these clocks.

This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2-23 compares the fully serial implementation to the mixed parallel and serial implementation.

***Figure 2-23. Comparison of General DSP and LatticeECP3 Approaches***






## LatticeECP3 sysDSP Slice Architecture Features

The LatticeECP3 sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

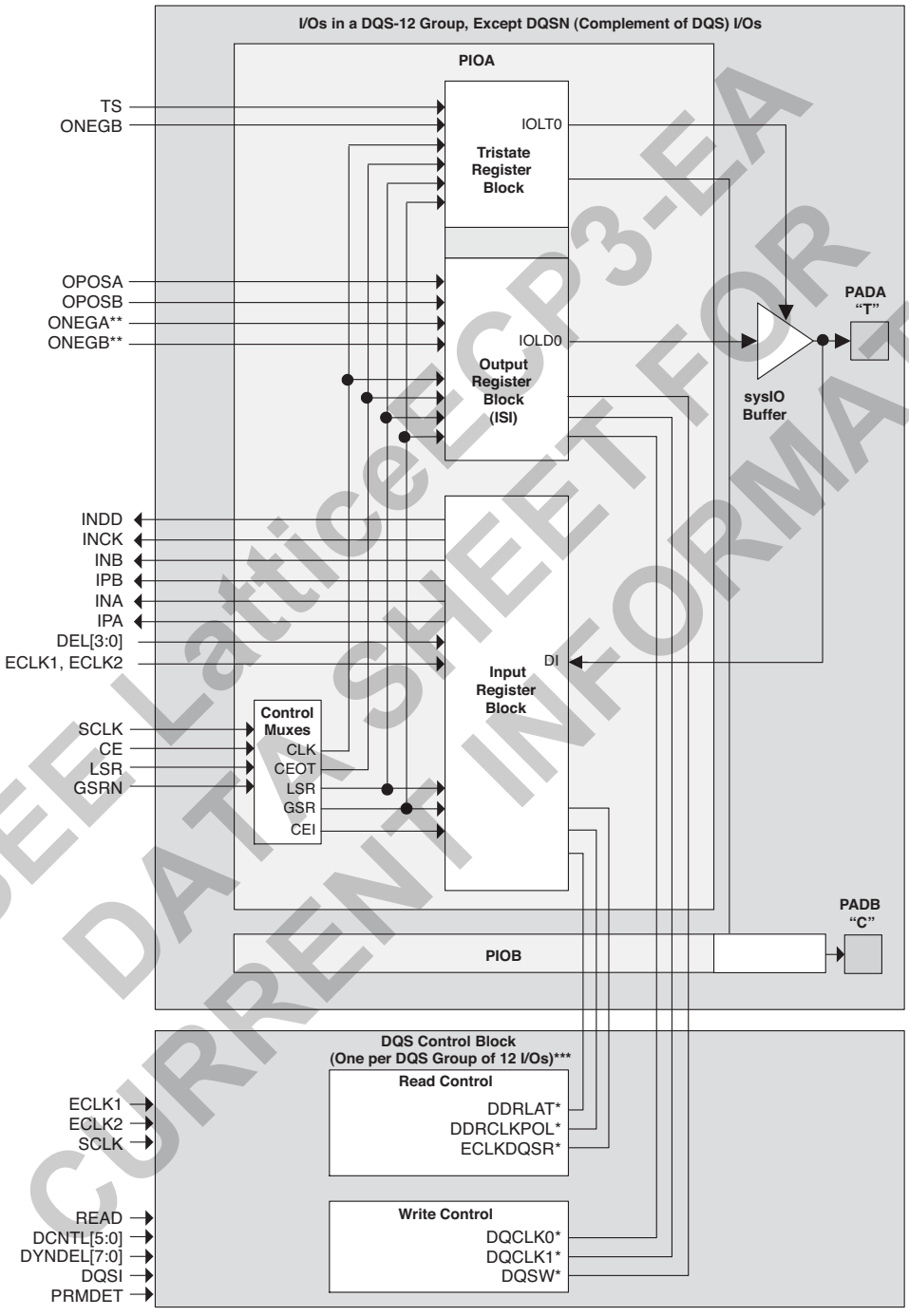
The LatticeECP3 sysDSP Slice supports many functions that include the following:

- Multiply (one 18x36, two 18x18 or four 9x9 Multiplies per Slice)
- Multiply (36x36 by cascading across two sysDSP slices)
- Multiply Accumulate (up to 18x36 Multipliers feeding an Accumulator that can have up to 54-bit resolution)
- Two Multiplies feeding one Accumulate per cycle for increased processing with lower latency (two 18x18 Multiplies feed into an accumulator that can accumulate up to 52 bits)
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
  - Minimizes fabric use for common DSP and ALU functions
  - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
  - Provides matching pipeline registers
  - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) Supports:
  - Dynamically selectable ALU OPCODE
  - Ternary arithmetic (addition/subtraction of three inputs)
  - Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
  - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such

## Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O buffers as shown in Figure 2-32. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysI/O buffer and receives input from the buffer. Table 2-11 provides the PIO signal list.

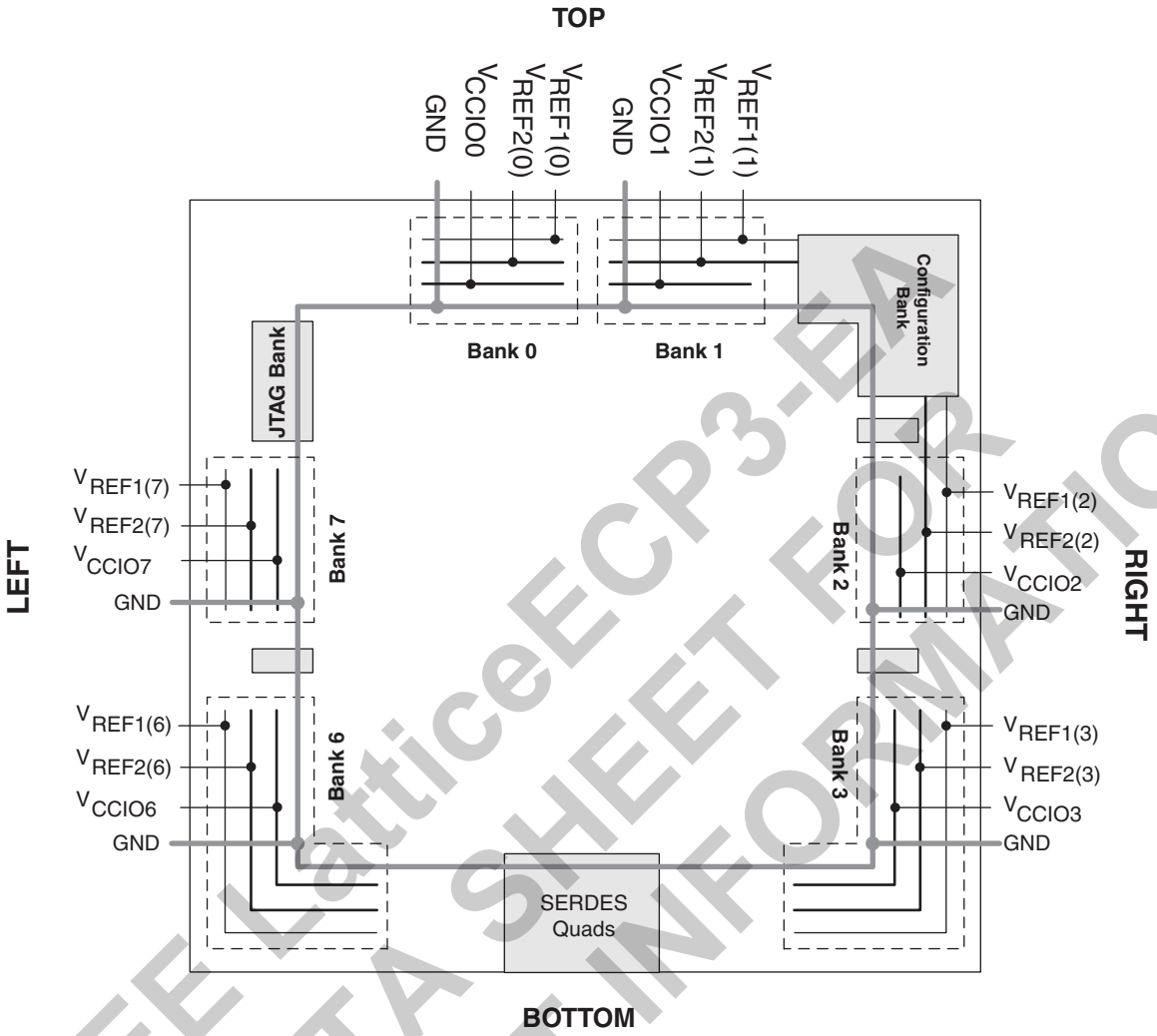
***Figure 2-32. PIC Diagram***






* Signals are available on left/right/top edges only.
** Signals are available on the left and right sides only
*** Selected PIO.

*Figure 2-38. LatticeECP3 Banks*






LatticeECP3 devices contain two types of sysI/O buffer pairs.

1. **Top (Bank 0 and Bank 1) and Bottom sysI/O Buffer Pairs (Single-Ended Outputs Only)**
   The sysI/O buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input. Only the top edge buffers have a programmable PCI clamp.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

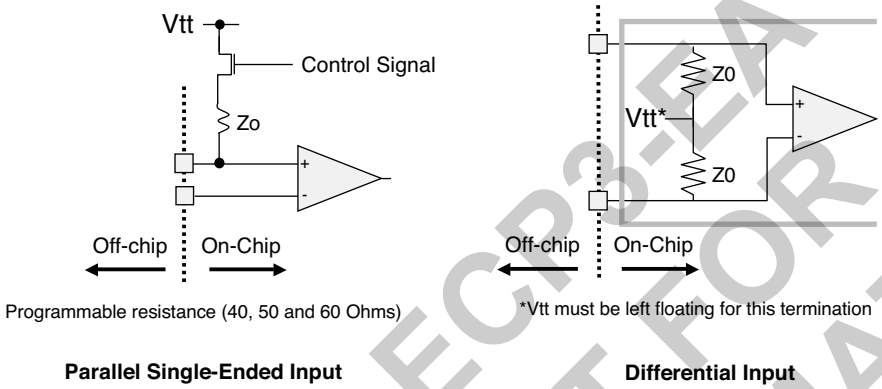
   On the top and bottom sides, there is no support for programmable on-chip input termination, which is required for DQ and DQS pins for DDR3 interface. This side is ideal for ADDR/CMD signals of DDR3, general purpose I/O, PCI, TR-LVDS (transition reduced LVDS) or LVDS inputs. Only the top I/O banks support hot socketing with $I_{DK}$ specified under the Hot Socketing Specifications. The configuration bank is not hot-socketable.

## On-Chip Programmable Termination

The LatticeECP3 supports a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single Ended Termination for SSTL15 inputs with programmable resistor values of 40, 50, or 60 ohms. This is particularly useful for low power JEDEC compliant DDR3 memory controller implementations. External termination to Vtt should be used for DDR2 memory controller implementation.
- Common mode termination of 80, 100, 120 ohms for differential inputs

***Figure 2-39. On-Chip Termination***




See Table 2-12 for termination options for input modes.

***Table 2-12. On-Chip Termination Options for Input Modes***

| IO_TYPE | TERMINATE to VTT[1, 2] | DIFFRENTIAL TERMINATION RESISTOR[1] |
|---|---|---|
| LVDS25 | þ | 80, 100, 120 |
| BLVDS25 | þ | 80, 100, 120 |
| MLVDS | þ | 80, 100, 120 |
| HSTL18_I | 40, 50, 60 | þ |
| HSTL18_II | 40, 50, 60 | þ |
| HSTL18D_I | 40, 50, 60 | þ |
| HSTL18D_II | 40, 50, 60 | þ |
| HSTL15_I | 40, 50, 60 | þ |
| HSTL15D_I | 40, 50, 60 | þ |
| SSTL25_I | 40, 50, 60 | þ |
| SSTL25_II | 40, 50, 60 | þ |
| SSTL25D_I | 40, 50, 60 | þ |
| SSTL25D_II | 40, 50, 60 | þ |
| SSTL18_I | 40, 50, 60 | þ |
| SSTL18_II | 40, 50, 60 | þ |
| SSTL18D_I | 40, 50, 60 | þ |
| SSTL18D_II | 40, 50, 60 | þ |
| SSTL15 | 40, 50, 60 | þ |
| SSTL15D | 40, 50, 60 | þ |

1. TERMINATE to VTT and DIFFRENTIAL TERMINATION RESISTOR when turn on can only have one setting per bank. Only left and right banks have this feature.
   Use of TERMINATE to VTT and DIFFRENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank.
   On-chip termination tolerance +/- 20%
2. External termination to VTT should be used when implementing DDR2 memory controller.

## Hot Socketing Specifications[1, 3, 4]

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| IDK_HS[2] | Input or I/O Leakage Current | $0 \le V_{IN} \le V_{IH}$ (Max.) | — | — | +/-1 | mA |
| IDK[5] | Input or I/O Leakage Current | $0 \le V_{IN} < V_{CCIO}$ | — | — | +/-1 | mA |
| | | $V_{CCIO} \le V_{IN} \le V_{CCIO}$ + 0.5V | — | 18 | — | mA |

1. $V_{CC}$, $V_{CCAUX}$ and $V_{CCIO}$ should rise/fall monotonically.
2. Applicable to general purpose I/O pins in top I/O banks only.
3. $I_{DK}$ is additive to $I_{PU}$, $I_{PW}$ or $I_{BH}$.
4. LVCMOS and LVTTL only.
5. Applicable to general purpose I/O pins in left and right I/O banks only.

## Hot Socketing Requirements[1, 2]

| Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Input current per SERDES I/O pin when device is powered down and inputs driven. | — | — | 8 | mA |

1. Assumes the device is powered down, all supplies grounded, both P and N inputs driven by CML driver with maximum allowed VCCOB (1.575V), 8b10b data, internal AC coupling.
2. Each P and N input must have less than the specified maximum input current. For a 16-channel device, the total input current would be 8mA*16 channels *2 input pins per channel = 256mA

## ESD Performance

| Pin Group | ESD Stress | Min. | Units |
|---|---|---|---|
| All pins | HBM | 1000 | V |
| All pins except high-speed serial and XRES[1] | CDM | 500 | V |
| High-speed serial inputs | CDM | 400 | V |

1. The XRES pin on the TW device passes CDM testing at 250V.

## LatticeECP3 Supply Current (Standby)[1, 2, 3, 4, 5, 6]

**Over Recommended Operating Conditions**

| Symbol | Parameter | Device | Typical | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply Current | ECP-17EA | 89.30 | mA |
| | | ECP3-35EA | 89.30 | mA |
| | | ECP3-70E | 226.30 | mA |
| | | ECP3-70EA | 230.60 | mA |
| | | ECP3-95E | 226.30 | mA |
| | | ECP3-95EA | 230.60 | mA |
| | | ECP3-150EA | 370.80 | mA |
| $I_{CCAUX}$ | Auxiliary Power Supply Current | ECP-17EA | 28.20 | mA |
| | | ECP3-35EA | 28.20 | mA |
| | | ECP3-70E | 30.60 | mA |
| | | ECP3-70EA | 30.60 | mA |
| | | ECP3-95E | 30.60 | mA |
| | | ECP3-95EA | 30.60 | mA |
| | | ECP3-150EA | 45.70 | mA |
| $I_{CCPLL}$ | PLL Power Supply Current (Per PLL) | ECP-17EA | 0.05 | mA |
| | | ECP3-35EA | 0.03 | mA |
| | | ECP3-70E | 0.02 | mA |
| | | ECP3-70EA | 0.02 | mA |
| | | ECP3-95E | 0.02 | mA |
| | | ECP3-95EA | 0.02 | mA |
| | | ECP3-150EA | 0.02 | mA |
| $I_{CCIO}$ | Bank Power Supply Current (Per Bank) | ECP-17EA | 1.38 | mA |
| | | ECP3-35EA | 1.38 | mA |
| | | ECP3-70E | 1.43 | mA |
| | | ECP3-70EA | 1.43 | mA |
| | | ECP3-95E | 1.43 | mA |
| | | ECP3-95EA | 1.43 | mA |
| | | ECP3-150EA | 1.46 | mA |
| $I_{CCJ}$ | JTAG Power Supply Current | All Devices | 2.50 | mA |
| $I_{CCA}$ | Transmit, Receive, PLL and Reference Clock Buffer Power Supply | ECP-17EA | 5.90 | mA |
| | | ECP3-35EA | 5.90 | mA |
| | | ECP3-70E | 17.80 | mA |
| | | ECP3-70EA | 17.80 | mA |
| | | ECP3-95E | 17.80 | mA |
| | | ECP3-95EA | 17.80 | mA |
| | | ECP3-150EA | 23.80 | mA |

1. For further information on supply current, please see the list of technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the $V_{CCIO}$ or GND.
3. Frequency 0 MHz.
4. Pattern represents a “blank” configuration data file.
5. $T_J$ = 85°C, power supplies at nominal voltage.
6. To determine the LatticeECP3 peak start-up current data, use the Power Calculator tool in ispLEVER.

## BLVDS25

The LatticeECP3 devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

***Figure 3-2. BLVDS25 Multi-point Output Example***

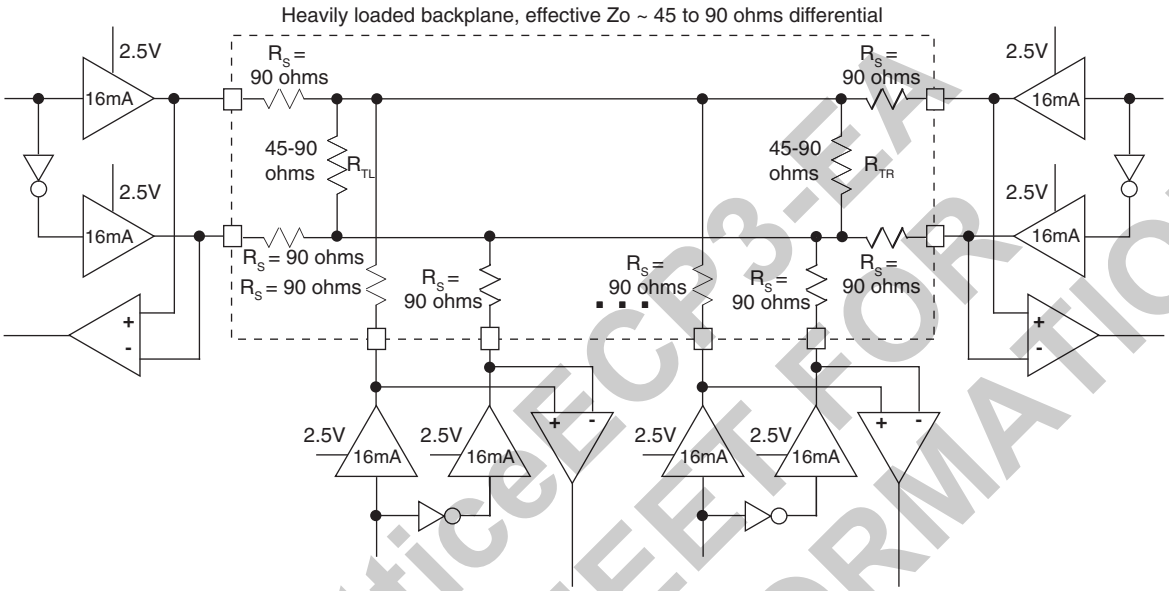



***Table 3-2. BLVDS25 DC Conditions[1]***

**Over Recommended Operating Conditions**

| Parameter | Description | Typical | | Units |
|---|---|---|---|---|
| | | Zo = 45Ω | Zo = 90Ω | |
| $V_{CCIO}$ | Output Driver Supply (+/- 5%) | 2.50 | 2.50 | V |
| $Z_{OUT}$ | Driver Impedance | 10.00 | 10.00 | Ω |
| $R_S$ | Driver Series Resistor (+/- 1%) | 90.00 | 90.00 | Ω |
| $R_{TL}$ | Driver Parallel Resistor (+/- 1%) | 45.00 | 90.00 | Ω |
| $R_{TR}$ | Receiver Termination (+/- 1%) | 45.00 | 90.00 | Ω |
| $V_{OH}$ | Output High Voltage | 1.38 | 1.48 | V |
| $V_{OL}$ | Output Low Voltage | 1.12 | 1.02 | V |
| $V_{OD}$ | Output Differential Voltage | 0.25 | 0.46 | V |
| $V_{CM}$ | Output Common Mode Voltage | 1.25 | 1.25 | V |
| $I_{DC}$ | DC Output Current | 11.24 | 10.20 | mA |

1. For input buffer, see LVDS table.

# LatticeECP3 External Switching Characteristics (Continued)[1, 2]

**Over Recommended Commercial Operating Conditions**

| Parameter | Description | Device | -8 | | -7 | | -6 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $f_{MAX\_IO}$ | Clock Frequency of I/O and PFU Register | ECP3-70E/95E | — | 500 | — | 420 | — | 375 | Mhz |
| **General I/O Pin Parameters Using Dedicated Clock Input Primary Clock with PLL with Clock Injection Removal Setting[2]** | | | | | | | | | |
| $t_{COPLL}$ | Clock to Output - PIO Output Register | ECP3-150EA | — | 2.5 | — | 2.7 | — | 3.1 | ns |
| $t_{SUPLL}$ | Clock to Data Setup - PIO Input Register | ECP3-150EA | 0.6 | — | 0.6 | — | 0.7 | — | ns |
| $t_{HPLL}$ | Clock to Data Hold - PIO Input Register | ECP3-150EA | 0.9 | — | 1.0 | — | 1.1 | — | ns |
| $t_{SU\_DELPLL}$ | Clock to Data Setup - PIO Input Register with Data Input Delay | ECP3-150EA | 1.5 | — | 1.6 | — | 1.8 | — | ns |
| $t_{H\_DELPLL}$ | Clock to Data Hold - PIO Input Register with Input Data Delay | ECP3-150EA | — | 0.1 | — | 0.1 | — | 0.1 | ns |
| $t_{COPLL}$ | Clock to Output - PIO Output Register | ECP3-70E/95E | — | 2.2 | — | 2.3 | — | 2.5 | ns |
| $t_{SUPLL}$ | Clock to Data Setup - PIO Input Register | ECP3-70E/95E | 0.6 | — | 0.7 | — | 0.8 | — | ns |
| $t_{HPLL}$ | Clock to Data Hold - PIO Input Register | ECP3-70E/95E | 0.9 | — | 1.1 | — | 1.3 | — | ns |
| $t_{SU\_DELPLL}$ | Clock to Data Setup - PIO Input Register with Data Input Delay | ECP3-70E/95E | 1.6 | — | 1.9 | — | 2.1 | — | ns |
| $t_{H\_DELPLL}$ | Clock to Data Hold - PIO Input Register with Input Data Delay | ECP3-70E/95E | 0.0 | — | 0.0 | — | 0.0 | — | ns |

| Parameter | Description | Device | -8 | | -7 | | -6 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Generic DDR** | | | | | | | | | |
| **Generic DDRX1 Inputs with Clock and Data (>10 Bits Wide) Centered at Pin (GDDRX1_RX.SCLK.Centered) Using PCLK Pin for Clock Input** | | | | | | | | | |
| **Data Left, Right and Top Sides & Clock Left, Right and Top Sides** | | | | | | | | | |
| $t_{SUGDDR}$ | Data Setup Before CLK | ECP3-150EA | | — | | — | | — | ps |
| $t_{HGDDR}$ | Data Hold After CLK | ECP3-150EA | | — | | — | | — | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-150EA | — | | — | | — | | MHz |
| **Generic DDRX1 Inputs with Clock in the Center of Data Window, without DLL (GDDRX1_RX.ECLK.Centered)** | | | | | | | | | |
| $t_{SUGDDR}$ | Data Setup Before CLK | ECP3-70E/95E | 515 | — | 515 | — | 515 | — | ps |
| $t_{HOGDDR}$ | Data Hold After CLK | ECP3-70E/95E | 515 | — | 515 | — | 515 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-70E/95E | — | 250 | — | 250 | — | 250 | MHz |
| **Generic DDRX1 Inputs with Clock and Data (> 10 Bits Wide) Aligned at Pin (GDDRX1_RX.SCLK.Aligned) using DLL-CLKIN Pin for Clock Input** | | | | | | | | | |
| **Data Left, Right and Top Sides & Clock Left and Right Sides** | | | | | | | | | |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | ECP3-150EA | — | | — | | — | | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | ECP3-150EA | | — | | — | | — | UI |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-150EA | — | | — | | — | | MHz |
| **Generic DDRX1 Inputs with Clock and Data Aligned, with DLL (GDDRX1_RX.ECLK.Aligned)** | | | | | | | | | |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | ECP3-70E/95E | — | 0.235 | — | 0.235 | — | 0.235 | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | ECP3-70E/95E | 0.765 | — | 0.765 | — | 0.765 | — | UI |

## SERDES External Reference Clock

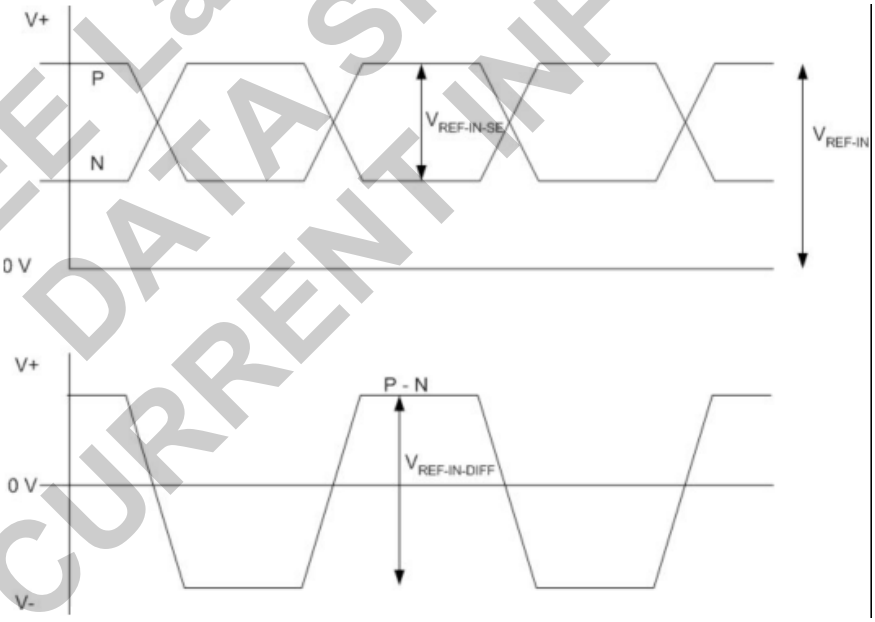
The external reference clock selection and its interface are a critical part of system applications for this product. Table 3-12 specifies reference clock requirements, over the full range of operating conditions.

***Table 3-12. External Reference Clock Specification (refclkp/refclkn)***

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $F_{REF}$ | Frequency range | 15 | — | 320 | MHz |
| $F_{REF-PPM}$ | Frequency tolerance[4] | -1000 | — | 1000 | ppm |
| $V_{REF-IN-SE}$ | Input swing, single-ended clock[1] | 200 | — | $V_{CCA}$ | mV, p-p |
| $V_{REF-IN-DIFF}$ | Input swing, differential clock | 200 | — | $2*V_{CCA}$ | mV, p-p differential |
| $V_{REF-IN}$ | Input levels | 0 | — | $V_{CCA}$ + 0.3 | V |
| $V_{REF-CM-AC}$ | Input common mode range (AC coupled)[2] | 0.125 | — | $V_{CCA}$ | V |
| $D_{REF}$ | Duty cycle[3] | 40 | — | 60 | % |
| $T_{REF-R}$ | Rise time (20% to 80%) | 200 | 500 | 1000 | ps |
| $T_{REF-F}$ | Fall time (80% to 20%) | 200 | 500 | 1000 | ps |
| $Z_{REF-IN-TERM-DIFF}$ | Differential input termination | -20% | 100/2K | +20% | Ohms |
| $C_{REF-IN-CAP}$ | Input capacitance | — | — | 7 | pF |

1. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.
2. When AC coupled, the input common mode range is determined by:
(Min input level) + (Peak-to-peak input swing)/2 ≤ (Input common mode voltage) ≤ (Max input level) - (Peak-to-peak input swing)/2
3. Measured at 50% amplitude.
4. Depending on the application, the PLL_LOL_SET and CDR_LOL_SET control registers may be adjusted for other tolerance values as described in TN1176, LatticeECP3 SERDES/PCS Usage Guide.

***Figure 3-13. SERDES External Reference Clock Waveforms***



# Gigabit Ethernet/Serial Rapid I/O Type 1/SGMII Electrical and Timing Characteristics

## AC and DC Characteristics

***Table 3-17. Transmit***

| Symbol | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $T_{RF}$ | Differential rise/fall time | 20%-80% | — | 80 | — | ps |
| $Z_{TX\_DIFF\_DC}$ | Differential impedance | | 80 | 100 | 120 | Ohms |
| $J_{TX\_DDJ}$[3, 4, 5] | Output data deterministic jitter | | — | — | 0.10 | UI |
| $J_{TX\_TJ}$[2, 3, 4, 5] | Total output data jitter | | — | — | 0.24 | UI |

1. Rise and fall times measured with board trace, connector and approximately 2.5pf load.
2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
3. Jitter values are measured with each CML output AC coupled into a 50-ohm impedance (100-ohm differential impedance).
4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
5. Values are measured at 1.25 Gbps.

***Table 3-18. Receive and Jitter Tolerance***

| Symbol | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $RL_{RX\_DIFF}$ | Differential return loss | From 100 MHz to 1.25 GHz | 10 | — | — | dB |
| $RL_{RX\_CM}$ | Common mode return loss | From 100 MHz to 1.25 GHz | 6 | — | — | dB |
| $Z_{RX\_DIFF}$ | Differential termination resistance | | 80 | 100 | 120 | Ohms |
| $J_{RX\_DJ}$[1, 2, 3, 4, 5] | Deterministic jitter tolerance (peak-to-peak) | | — | — | 0.34 | UI |
| $J_{RX\_RJ}$[1, 2, 3, 4, 5] | Random jitter tolerance (peak-to-peak) | | — | — | 0.26 | UI |
| $J_{RX\_SJ}$[1, 2, 3, 4, 5] | Sinusoidal jitter tolerance (peak-to-peak) | | — | — | 0.11 | UI |
| $J_{RX\_TJ}$[1, 2, 3, 4, 5] | Total jitter tolerance (peak-to-peak) | | — | — | 0.71 | UI |
| $T_{RX\_EYE}$ | Receiver eye opening | | 0.29 | — | — | UI |

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-14.
2. Jitter values are measured with each high-speed input AC coupled into a 50-ohm impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.
5. Values are measured at 1.25 Gbps.

## Pin Information Summary

| Pin Information Summary | | ECP3-17EA | | ECP3-35EA | | | ECP3-70E/EA | | |
|---|---|---|---|---|---|---|---|---|---|
| Pin Type | | 256 ftBGA | 484 fpBGA | 256 ftBGA | 484 fpBGA | 672 fpBGA | 484 fpBGA | 672 fpBGA | 1156 fpBGA |
| General Purpose Inputs/Outputs per Bank | Bank 0 | 26 | 36 | 26 | 42 | 48 | 42 | 60 | 86 |
| | Bank 1 | 14 | 24 | 14 | 36 | 36 | 36 | 48 | 78 |
| | Bank 2 | 6 | 12 | 6 | 24 | 24 | 24 | 34 | 36 |
| | Bank 3 | 18 | 44 | 16 | 54 | 59 | 54 | 59 | 86 |
| | Bank 6 | 20 | 44 | 18 | 63 | 61 | 63 | 67 | 86 |
| | Bank 7 | 19 | 32 | 19 | 36 | 42 | 36 | 48 | 54 |
| | Bank 8 | 24 | 24 | 24 | 24 | 24 | 24 | 24 | 24 |
| General Purpose Inputs per Bank | Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 2 | 2 | 2 | 2 | 4 | 4 | 4 | 8 | 8 |
| | Bank 3 | 0 | 0 | 2 | 4 | 4 | 4 | 12 | 12 |
| | Bank 6 | 0 | 0 | 2 | 4 | 4 | 4 | 12 | 12 |
| | Bank 7 | 4 | 4 | 4 | 4 | 4 | 4 | 8 | 8 |
| | Bank 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| General Purpose Outputs per Bank | Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 6 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Total Single-Ended User I/O | | 133 | 222 | 133 | 295 | 310 | 295 | 380 | 490 |
| VCC | | 6 | 16 | 6 | 16 | 32 | 16 | 32 | 32 |
| VCCAUX | | 4 | 8 | 4 | 8 | 12 | 8 | 12 | 16 |
| VTT | | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 8 |
| VCCA | | 4 | 4 | 4 | 4 | 8 | 4 | 8 | 16 |
| VCCPLL | | 2 | 4 | 2 | 4 | 4 | 4 | 4 | 4 |
| VCCIO | Bank 0 | 2 | 2 | 2 | 2 | 4 | 2 | 4 | 4 |
| | Bank 1 | 2 | 2 | 2 | 2 | 4 | 2 | 4 | 4 |
| | Bank 2 | 2 | 2 | 2 | 2 | 4 | 2 | 4 | 4 |
| | Bank 3 | 2 | 2 | 2 | 2 | 4 | 2 | 4 | 4 |
| | Bank 6 | 2 | 2 | 2 | 2 | 4 | 2 | 4 | 4 |
| | Bank 7 | 2 | 2 | 2 | 2 | 4 | 2 | 4 | 4 |
| | Bank 8 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| VCCJ | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| TAP | | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| GND, GNDIO | | 50 | 98 | 50 | 98 | 139 | 98 | 139 | 233 |
| NC | | 0 | 73 | 0 | 0 | 96 | 0 | 0 | 238 |
| Reserved[1] | | 0 | 2 | 0 | 2 | 2 | 2 | 2 | 2 |
| SERDES | | 26 | 26 | 26 | 26 | 26 | 26 | 52 | 78 |
| Miscellaneous Pins | | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| Total Bonded Pins | | 256 | 484 | 256 | 484 | 672 | 484 | 672 | 1156 |

## Logic Signal Connections

Package pinout information can be found under “Data Sheets” on the LatticeECP3 product pages on the Lattice website at www.latticesemi.com/products/fpga/ecp3 and in the Lattice ispLEVER Design Planner software. To create pinout information from within Design Planner, select **View -> Package View**. Then select **Select File -> Export** and choose a type of output file. See Design Planner help for more information.

## Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

### For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1181, Power Consumption and Management for LatticeECP3 Devices
- Power Calculator tool included with the Lattice ispLEVER design tool, or as a standalone download from www.latticesemi.com/software

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|
| LFE3-150EA-6FN672CTW* | 1.2V | -6 | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-7FN672CTW* | 1.2V | -7 | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-8FN672CTW* | 1.2V | -8 | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-6FN1156CTW* | 1.2V | -6 | Lead-Free fpBGA | 1156 | COM | 149 |
| LFE3-150EA-7FN1156CTW* | 1.2V | -7 | Lead-Free fpBGA | 1156 | COM | 149 |
| LFE3-150EA-8FN1156CTW* | 1.2V | -8 | Lead-Free fpBGA | 1156 | COM | 149 |

*Note: Specifications for the LFE3-150EA-*sp*FN*pkg*CTW and LFE3-150EA-*sp*FN*pkg*ITW devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*sp*FN*pkg*C and LFE3-150EA-*sp*FN*pkg*I devices respectively, except as specified below.

- The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.
- The SERDES XRES pin on the TW device passes CDM testing at 250V.

# LatticeECP3 Family Data Sheet Supplemental Information



## For Further Information

A variety of technical notes for the LatticeECP3 family are available on the Lattice website at www.latticesemi.com.

- TN1169, LatticeECP3 sysCONFIG Usage Guide
- TN1176, LatticeECP3 SERDES/PCS Usage Guide
- TN1177, LatticeECP3 sysIO Usage Guide
- TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide
- TN1179, LatticeECP3 Memory Usage Guide
- TN1180, LatticeECP3 High-Speed I/O Interface
- TN1181, Power Consumption and Management for LatticeECP3 Devices
- TN1182, LatticeECP3 sysDSP Usage Guide
- TN1184, LatticeECP3 Soft Error Detection (SED) Usage Guide
- TN1189, LatticeECP3 Hardware Checklist

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com

# LatticeECP3 Family Data Sheet Revision History



| Date | Version | Section | Change Summary |
|---|---|---|---|
| February 2009 | 01.0 | — | Initial release. |
| May 2009 | 01.1 | All | Removed references to Parallel burst mode Flash. |
| | | Introduction | Features - Changed 250 Mbps to 230 Mbps in Embedded SERDES bulleted section and added a footnote to indicate 230 Mbps applies to 8b10b and 10b12b applications. |
| | | | Updated data for ECP3-17 in LatticeECP3 Family Selection Guide table. |
| | | | Changed embedded memory from 552 to 700 Kbits in LatticeECP3 Family Selection Guide table. |
| | | Architecture | Updated description for CLKFB in General Purpose PLL Diagram. |
| | | | Corrected Primary Clock Sources text section. |
| | | | Corrected Secondary Clock/Control Sources text section. |
| | | | Corrected Secondary Clock Regions table. |
| | | | Corrected note below Detailed sysDSP Slice Diagram. |
| | | | Corrected Clock, Clock Enable, and Reset Resources text section. |
| | | | Corrected ECP3-17 EBR number in Embedded SRAM in the LatticeECP3 Family table. |
| | | | Added On-Chip Termination Options for Input Modes table. |
| | | | Updated Available SERDES Quads per LatticeECP3 Devices table. |
| | | | Updated Simplified Channel Block Diagram for SERDES/PCS Block diagram. |
| | | | Updated Device Configuration text section. |
| | | | Corrected software default value of MCLK to be 2.5 MHz. |
| | | DC and Switching Characteristics | Updated VCCOB Min/Max data in Recommended Operating Conditions table. |
| | | | Corrected footnote 2 in sysIO Recommended Operating Conditions table. |
| | | | Added added footnote 7 for $t_{SKEW\_PRIB}$ to External Switching Characteristics table. |
| | | | Added 2-to-1 Gearing text section and table. |
| | | | Updated External Reference Clock Specification (refclkp/refclkn) table. |
| | | | LatticeECP3 sysCONFIG Port Timing Specifications - updated $t_{DINIT}$ information. |
| | | | Added sysCONFIG Port Timing waveform. |
| | | | Serial Input Data Specifications table, delete Typ data for $V_{RX\text{-}DIFF\text{-}S}$. |
| | | | Added footnote 4 to sysCLOCK PLL Timing table for $t_{PFD}$. |
| | | | Added SERDES/PCS Block Latency Breakdown table. |
| | | | External Reference Clock Specifications table, added footnote 4, add symbol name vREF-IN-DIFF. |
| | | | Added SERDES External Reference Clock Waveforms. |
| | | | Updated Serial Output Timing and Levels table. |
| | | | Pin-to-pin performance table, changed "typically 3% slower" to "typically slower". |