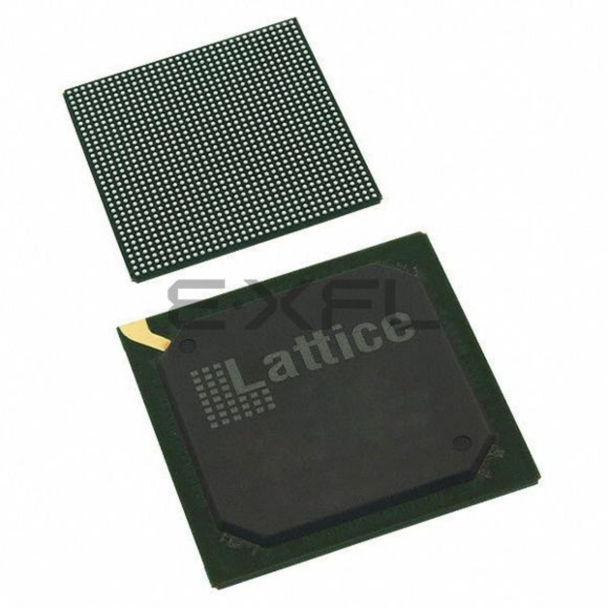

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8375
Number of Logic Elements/Cells	67000
Total RAM Bits	4526080
Number of I/O	490
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-70e-7fn1156i

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, please refer to TN1179, LatticeECP3 Memory Usage Guide.

Routing

There are many resources provided in the LatticeECP3 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The LatticeECP3 family has an enhanced routing architecture that produces a compact design. The ispLEVER design tool suite takes the output of the synthesis tool and places and routes the design.

sysCLOCK PLLs and DLLs

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. All the devices in the LatticeECP3 family support four to ten full-featured General Purpose PLLs.

General Purpose PLL

The architecture of the PLL is shown in Figure 2-4. A description of the PLL functionality follows.

CLKI is the reference frequency (generated either from the pin or from routing) for the PLL. CLKI feeds into the Input Clock Divider block. The CLKFB is the feedback signal (generated from CLKOP, CLKOS or from a user clock pin/logic). This signal feeds into the Feedback Divider. The Feedback Divider is used to multiply the reference frequency.

Both the input path and feedback signals enter the Voltage Controlled Oscillator (VCO) block. In this block the difference between the input path and feedback signals is used to control the frequency and phase of the oscillator. A LOCK signal is generated by the VCO to indicate that the VCO has locked onto the input clock signal. In dynamic mode, the PLL may lose lock after a dynamic delay adjustment and not relock until the t_{LOCK} parameter has been satisfied.

The output of the VCO then enters the CLKOP divider. The CLKOP divider allows the VCO to operate at higher frequencies than the clock output (CLKOP), thereby increasing the frequency range. The Phase/Duty Select block adjusts the phase and duty cycle of the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted. A secondary divider takes the CLKOP or CLKOS signal and uses it to derive lower frequency outputs (CLKOK).

The primary output from the CLKOP divider (CLKOP) along with the outputs from the secondary dividers (CLKOK and CLKOK2) and Phase/Duty select (CLKOS) are fed to the clock distribution network.

The PLL allows two methods for adjusting the phase of signal. The first is referred to as Fine Delay Adjustment. This inserts up to 16 nominal 125ps delays to be applied to the secondary PLL output. The number of steps may be set statically or from the FPGA logic. The second method is referred to as Coarse Phase Adjustment. This allows the phase of the rising and falling edge of the secondary PLL output to be adjusted in 22.5 degree steps. The number of steps may be set statically or from the FPGA logic.

Table 2-5. DLL Signals

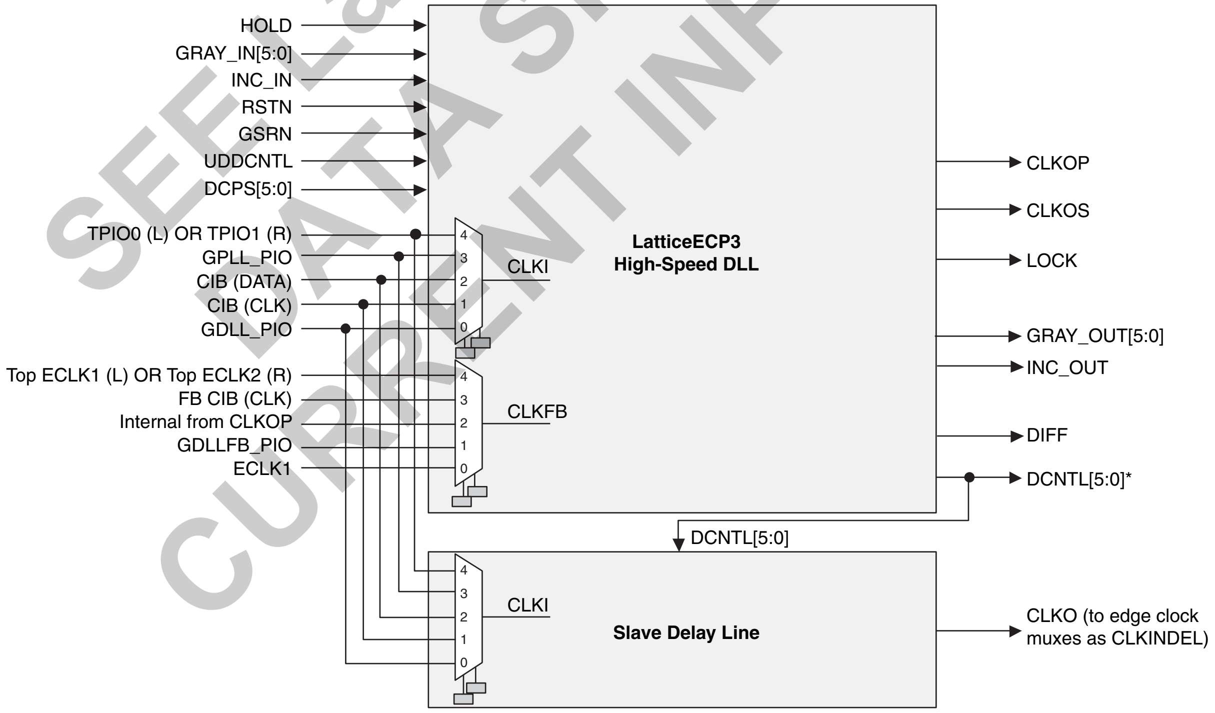
Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	DLL feed input from DLL output, clock net, routing or external pin
RSTN	I	Active low synchronous reset
ALUHOLD	I	Active high freezes the ALU
UDDCNTL	I	Synchronous enable signal (hold high for two cycles) from routing
CLKOP	O	The primary clock output
CLKOS	O	The secondary clock output with fine delay shift and/or division by 2 or by 4
LOCK	O	Active high phase lock indicator
INCI	I	Incremental indicator from another DLL via CIB.
GRAYI[5:0]	I	Gray-coded digital control bus from another DLL in time reference mode.
DIFF	O	Difference indicator when DCNTL is difference than the internal setting and update is needed.
INCO	O	Incremental indicator to other DLLs via CIB.
GRAYO[5:0]	O	Gray-coded digital control bus to other DLLs via CIB

LatticeECP3 devices have two general DLLs and four Slave Delay lines, two per DLL. The DLLs are in the lowest EBR row and located adjacent to the EBR. Each DLL replaces one EBR block. One Slave Delay line is placed adjacent to the DLL and the duplicate Slave Delay line (in Figure 2-6) for the DLL is placed in the I/O ring between Banks 6 and 7 and Banks 2 and 3.

The outputs from the DLL and Slave Delay lines are fed to the clock distribution network.

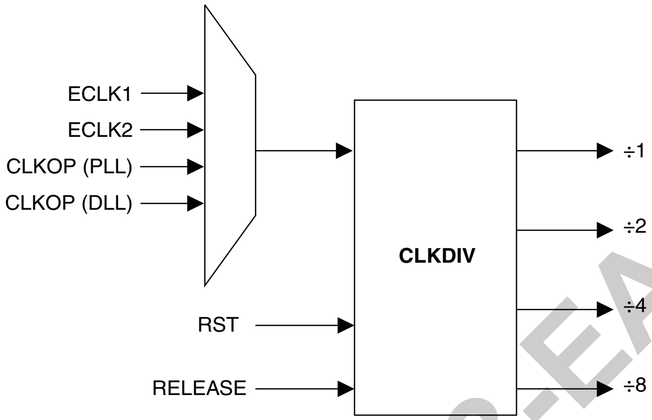
For more information, please see TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide.

Figure 2-6. Top-Level Block Diagram, High-Speed DLL and Slave Delay Line



* This signal is not user accessible. It can only be used to feed the slave delay line.

Figure 2-8. Clock Divider Connections



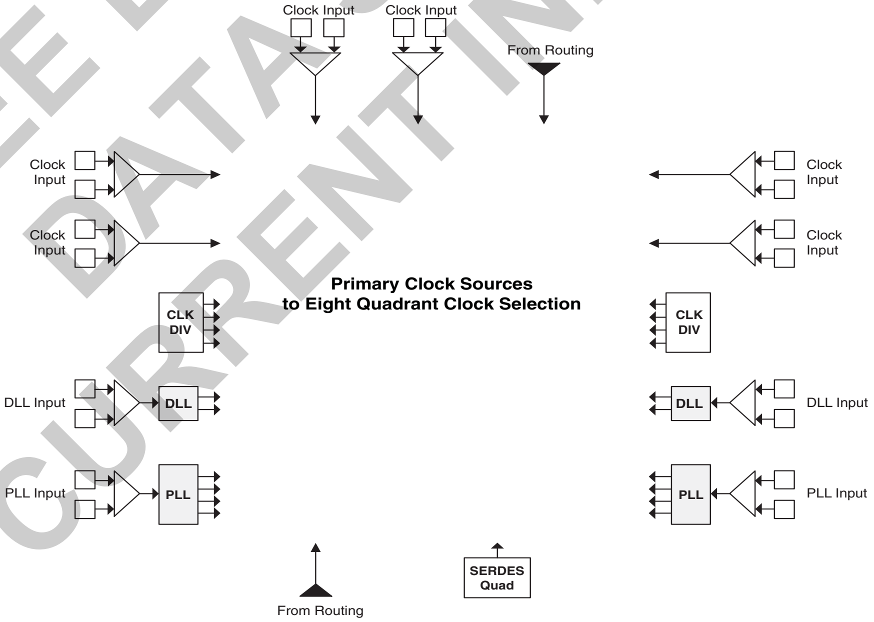
Clock Distribution Network

LatticeECP3 devices have eight quadrant-based primary clocks and eight secondary clock/control sources. Two high performance edge clocks are available on the top, left, and right edges of the device to support high speed interfaces. These clock sources are selected from external I/Os, the sysCLOCK PLLs, DLLs or routing. These clock sources are fed throughout the chip via a clock distribution system.

Primary Clock Sources

LatticeECP3 devices derive clocks from six primary source types: PLL outputs, DLL outputs, CLKDIV outputs, dedicated clock inputs, routing and SERDES Quads. LatticeECP3 devices have two to ten sysCLOCK PLLs and two DLLs, located on the left and right sides of the device. There are six dedicated clock inputs: two on the top side, two on the left side and two on the right side of the device. Figures 2-9, 2-10 and 2-11 show the primary clock sources for LatticeECP3 devices.

Figure 2-9. Primary Clock Sources for LatticeECP3-17

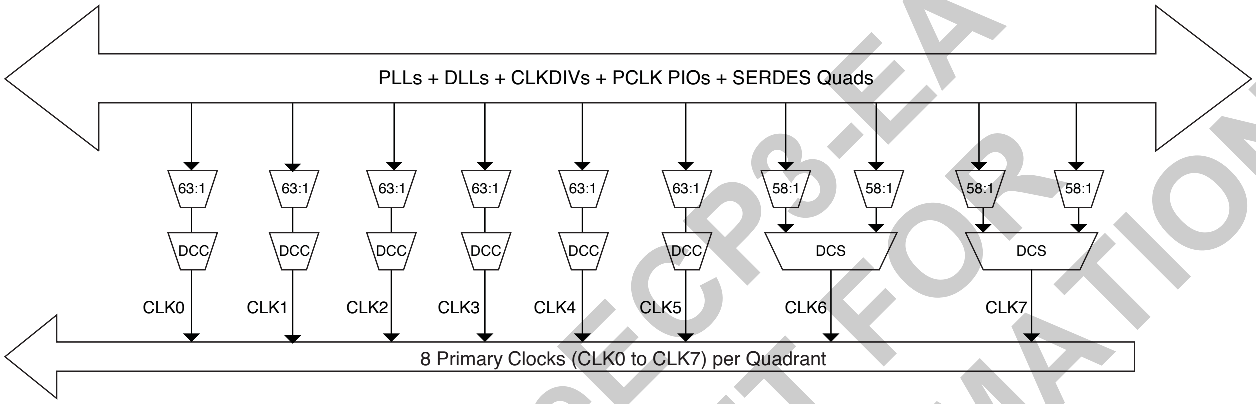


Note: Clock inputs can be configured in differential or single-ended mode.

Primary Clock Routing

The purpose of the primary clock routing is to distribute primary clock sources to the destination quadrants of the device. A global primary clock is a primary clock that is distributed to all quadrants. The clock routing structure in LatticeECP3 devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 2-12 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally.

Figure 2-12. Per Quadrant Primary Clock Selection



Dynamic Clock Control (DCC)

The DCC (Quadrant Clock Enable/Disable) feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, all the logic fed by that clock does not toggle, reducing the overall power consumption of the device.

Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved regardless of when the select signal is toggled. There are two DCS blocks per quadrant; in total, there are eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 2-12).

Figure 2-13 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, please see the list of technical documentation at the end of this data sheet.

Figure 2-13. DCS Waveforms

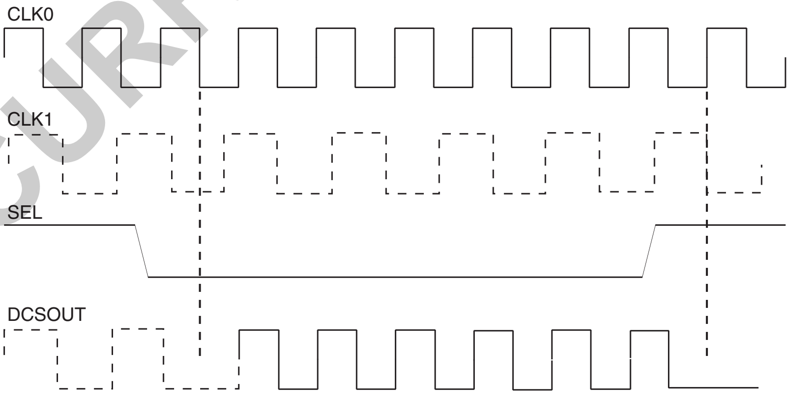
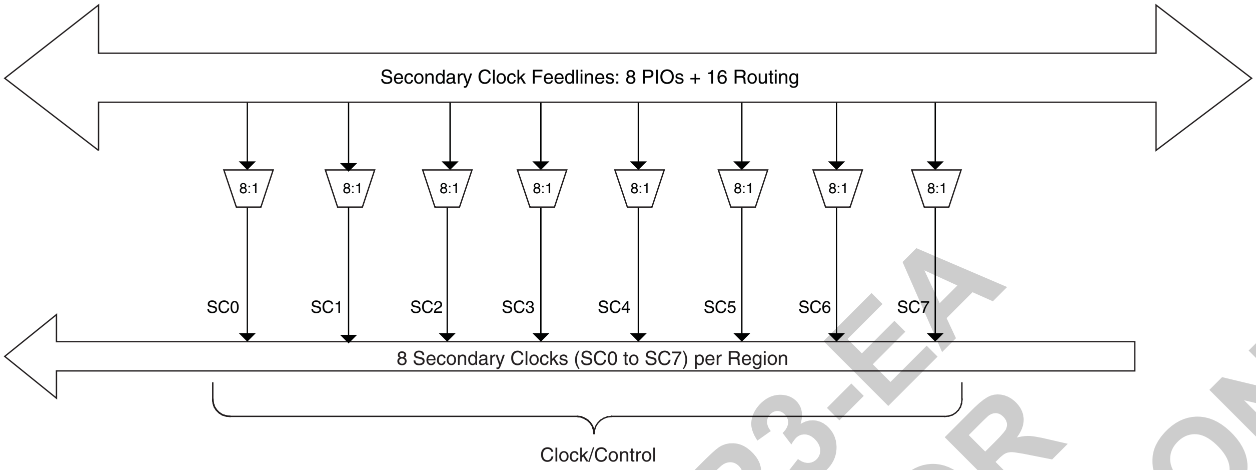


Figure 2-16. Per Region Secondary Clock Selection



Slice Clock Selection

Figure 2-17 shows the clock selections and Figure 2-18 shows the control selections for Slice0 through Slice2. All the primary clocks and seven secondary clocks are routed to this clock selection mux. Other signals can be used as a clock input to the slices via routing. Slice controls are generated from the secondary clocks/controls or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-17. Slice0 through Slice2 Clock Selection

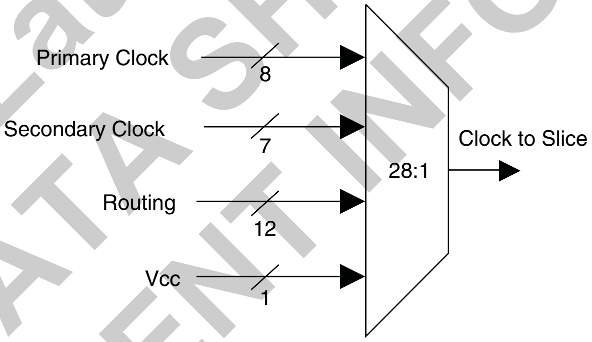


Figure 2-18. Slice0 through Slice2 Control Selection

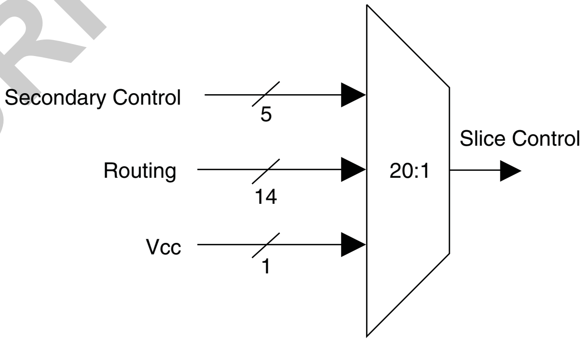


Figure 2-20. Sources of Edge Clock (Left and Right Edges)

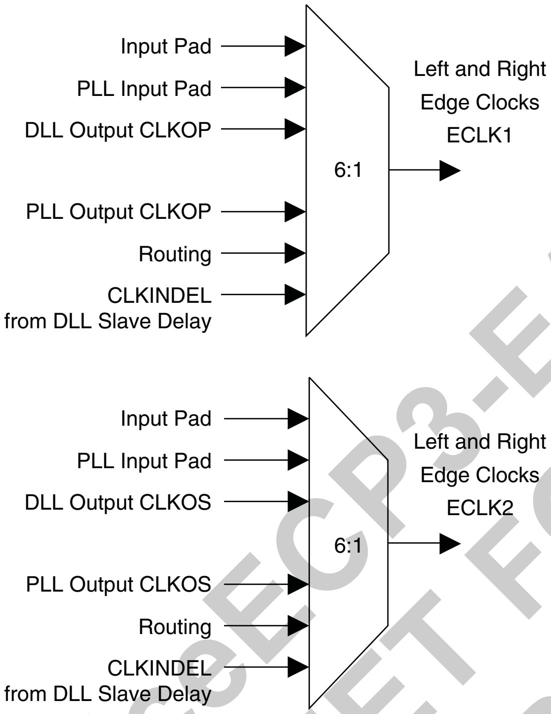
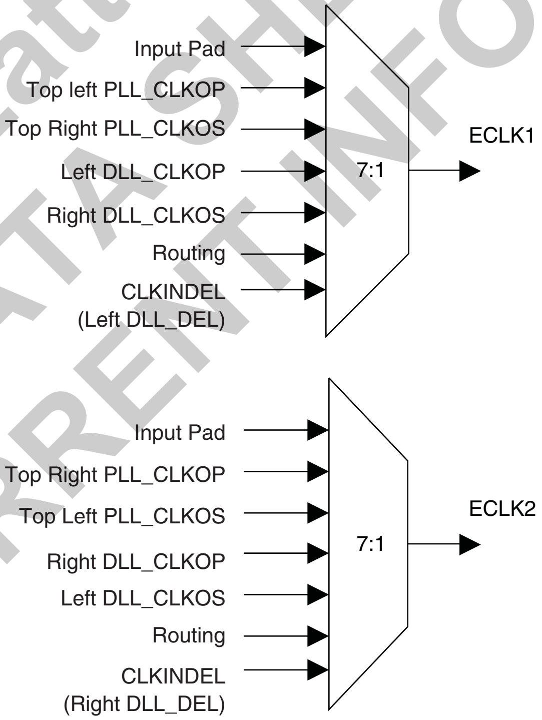
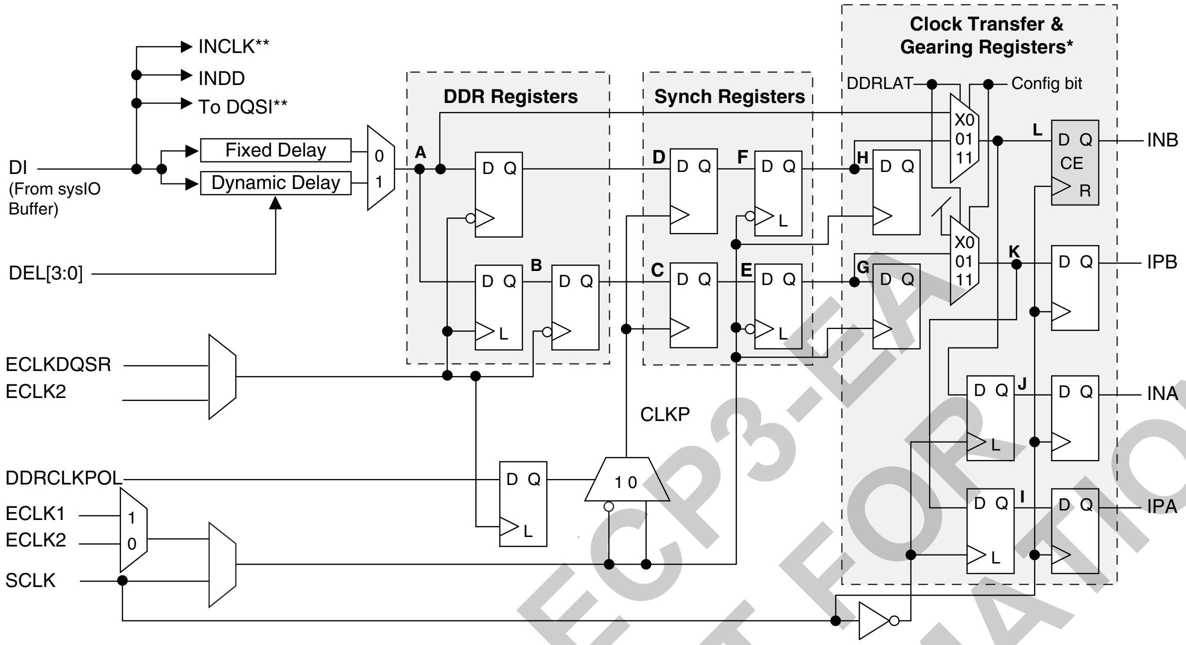


Figure 2-21. Sources of Edge Clock (Top Edge)



The edge clocks have low injection delay and low skew. They are used to clock the I/O registers and thus are ideal for creating I/O interfaces with a single clock signal and a wide data bus. They are also used for DDR Memory or Generic DDR interfaces.

Figure 2-33. ECP3-70/95 (E or EA) Input Register Block for Left, Right and Top Edges



* Only on the left and right sides.
** Selected PIO.
Note: Simplified diagram does not show CE/SET/REST details.

Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysI/O buffers. The blocks on the left and right PIOs contain registers for SDR and full DDR operation. The topside PIO block is the same as the left and right sides except it does not support ODDRX2 gearing of output logic. ODDRX2 gearing is used in DDR3 memory interfaces.The PIO blocks on the bottom contain the SDR registers and generic DDR interface without gearing.

Figure 2-34 shows the Output Register Block for PIOs on the left and right edges.

In SDR mode, OPOSA feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a Dtype or latch. In DDR mode, two of the inputs are fed into registers on the positive edge of the clock. At the next clock cycle, one of the registered outputs is also latched.

A multiplexer running off the same clock is used to switch the mux between the 11 and 01 inputs that will then feed the output.

A gearbox function can be implemented in the output register block that takes four data streams: OPOSA, ONEGA, OPOSB and ONEGB. All four data inputs are registered on the positive edge of the system clock and two of them are also latched. The data is then output at a high rate using a multiplexer that runs off the DQCLK0 and DQCLK1 clocks. DQCLK0 and DQCLK1 are used in this case to transfer data from the system clock to the edge clock domain. These signals are generated in the DQS Write Control Logic block. See Figure 2-37 for an overview of the DQS write control logic.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.

Further discussion on using the DQS strobe in this module is discussed in the DDR Memory section of this data sheet.

(referred to as DQS) is not free-running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The delay required for the DQS signal is generated by two dedicated DLLs (DDR DLL) on opposite side of the device. Each DLL creates DQS delays in its half of the device as shown in Figure 2-36. The DDR DLL on the left side will generate delays for all the DQS Strobe pins on Banks 0, 7 and 6 and DDR DLL on the right will generate delays for all the DQS pins on Banks 1, 2 and 3. The DDR DLL loop compensates for temperature, voltage and process variations by using the system clock and DLL feedback loop. DDR DLL communicates the required delay to the DQS delay block using a 7-bit calibration bus (DCNTL[6:0])

The DQS signal (selected PIOs only, as shown in Figure 2-35) feeds from the PAD through a DQS control logic block to a dedicated DQS routing resource. The DQS control logic block consists of DQS Read Control logic block that generates control signals for the read side and DQS Write Control logic that generates the control signals required for the write side. A more detailed DQS control diagram is shown in Figure 2-37, which shows how the DQS control blocks interact with the data paths.

The DQS Read control logic receives the delay generated by the DDR DLL on its side and delays the incoming DQS signal by 90 degrees. This delayed ECLKDQSR is routed to 10 or 11 DQ pads covered by that DQS signal. This block also contains a polarity control logic that generates a DDRCLKPOL signal, which controls the polarity of the clock to the sync registers in the input register blocks. The DQS Read control logic also generates a DDRLAT signal that is in the input register block to transfer data from the first set of DDR register to the second set of DDR registers when using the DDRX2 gearbox mode for DDR3 memory interface.

The DQS Write control logic block generates the DQCLK0 and DQCLK1 clocks used to control the output gearing in the Output register block which generates the DDR data output and the DQS output. They are also used to control the generation of the DQS output through the DQS output register block. In addition to the DCNTL [6:0] input from the DDR DLL, the DQS Write control block also uses a Dynamic Delay DYN DEL [7:0] attribute which is used to further delay the DQS to accomplish the write leveling found in DDR3 memory. Write leveling is controlled by the DDR memory controller implementation. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock. This will generate the DQSW signal used to generate the DQS output in the DQS output register block.

Figure 2-36 and Figure 2-37 show how the DQS transition signals that are routed to the PIOs.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.

Please see TN1177, LatticeECP3 sysIO Usage Guide for on-chip termination usage and value ranges.

Equalization Filter

Equalization filtering is available for single-ended inputs on both true and complementary I/Os, and for differential inputs on the true I/Os on the left, right, and top sides. Equalization is required to compensate for the difficulty of sampling alternating logic transitions with a relatively slow slew rate. It is considered the most useful for the Input DDRX2 modes, used in DDR3 memory, LVDS, or TRLVDS signaling. Equalization filter acts as a tunable filter with settings to determine the level of correction. In the LatticeECP3 devices, there are four settings available: 0 (none), 1, 2 and 3. The default setting is 0. The equalization logic resides in the sysI/O buffers, the two bits of setting is set uniquely in each input IOLOGIC block. Therefore, each sysI/O can have a unique equalization setting within a DQS-12 group.

Hot Socketing

LatticeECP3 devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. Please refer to the Hot Socketing Specifications in the DC and Switching Characteristics in this data sheet.

SERDES and PCS (Physical Coding Sublayer)

LatticeECP3 devices feature up to 16 channels of embedded SERDES/PCS arranged in quads at the bottom of the devices supporting up to 3.2Gbps data rate. Figure 2-40 shows the position of the quad blocks for the LatticeECP3-150 devices. Table 2-14 shows the location of available SERDES Quads for all devices.

The LatticeECP3 SERDES/PCS supports a range of popular serial protocols, including:

- PCI Express 1.1
- Ethernet (XAUI, GbE - 1000 Base CS/SX/LX and SGMII)
- Serial RapidIO
- SMPTE SDI (3G, HD, SD)
- CPRI
- SONET/SDH (STS-3, STS-12, STS-48)

Each quad contains four dedicated SERDES for high speed, full duplex serial data transfer. Each quad also has a PCS block that interfaces to the SERDES channels and contains protocol specific digital logic to support the standards listed above. The PCS block also contains interface logic to the FPGA fabric. All PCS logic for dedicated protocol support can also be bypassed to allow raw 8-bit or 10-bit interfaces to the FPGA fabric.

Even though the SERDES/PCS blocks are arranged in quads, multiple baud rates can be supported within a quad with the use of dedicated, per channel ÷1, ÷2 and ÷11 rate dividers. Additionally, multiple quads can be arranged together to form larger data pipes.

For information on how to use the SERDES/PCS blocks to support specific protocols, as well on how to combine multiple protocols and baud rates within a device, please refer to TN1176, LatticeECP3 SERDES/PCS Usage Guide.

The ispLEVER design tools from Lattice support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With ispLEVER, the user can define the mode for each quad in a design.

Popular standards such as 10Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), a single quad (Four SERDES channels and PCS) and some additional logic from the core.

The LatticeECP3 family also supports a wide range of primary and secondary protocols. Within the same quad, the LatticeECP3 family can support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. Table 2-15 lists the allowable combination of primary and secondary protocol combinations.

Flexible Quad SERDES Architecture

The LatticeECP3 family SERDES architecture is a quad-based architecture. For most SERDES settings and standards, the whole quad (consisting of four SERDES) is treated as a unit. This helps in silicon area savings, better utilization and overall lower cost.

However, for some specific standards, the LatticeECP3 quad architecture provides flexibility; more than one standard can be supported within the same quad.

Table 2-15 shows the standards can be mixed and matched within the same quad. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same quad. In Table 2-15, the Primary Protocol column refers to the standard that determines the reference clock and PLL settings. The Secondary Protocol column shows the other standard that can be supported within the same quad.

Furthermore, Table 2-15 also implies that more than two standards in the same quad can be supported, as long as they conform to the data rate and reference clock requirements. For example, a quad may contain PCI Express 1.1, SGMII, Serial RapidIO Type I and Serial RapidIO Type II, all in the same quad.

Table 2-15. LatticeECP3 Primary and Secondary Protocol Support

Primary Protocol	Secondary Protocol
PCI Express 1.1	SGMII
PCI Express 1.1	Gigabit Ethernet
PCI Express 1.1	Serial RapidIO Type I
PCI Express 1.1	Serial RapidIO Type II
Serial RapidIO Type I	SGMII
Serial RapidIO Type I	Gigabit Ethernet
Serial RapidIO Type II	SGMII
Serial RapidIO Type II	Gigabit Ethernet
Serial RapidIO Type II	Serial RapidIO Type I
CPRI-3	CPRI-2 and CPRI-1
3G-SDI	HD-SDI and SD-SDI

For further information on SERDES, please see TN1176, LatticeECP3 SERDES/PCS Usage Guide.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeECP3 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode (normal operation) the device can be programmed to generate an error signal.

For further information on SED support, please see TN1184, LatticeECP3 Soft Error Detection (SED) Usage Guide.

External Resistor

LatticeECP3 devices require a single external, 10K ohm ±1% value between the XRES pin and ground. Device configuration will not be completed if this resistor is missing. There is no boundary scan register on the external resistor pad.

On-Chip Oscillator

Every LatticeECP3 device has an internal CMOS oscillator which is used to derive a Master Clock (MCLK) for configuration. The oscillator and the MCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCLK is nominally 2.5MHz. Table 2-16 lists all the available MCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 3.1MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.5MHz.

This internal CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

Table 2-16. Selectable Master Clock (MCLK) Frequencies During Configuration (Nominal)

MCLK (MHz)	MCLK (MHz)	MCLK (MHz)
2.5[1]	10	41
3.1	13	45
4.3	15	51
5.4	20	55
6.9	26	60
8.1	30	130
9.2	34	—

1. Software default MCLK frequency. Hardware default is 3.1MHz.

Density Shifting

The LatticeECP3 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same packge.

LVDS25E

The top and bottom sides of LatticeECP3 devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.

Figure 3-1. LVDS25E Output Termination Example

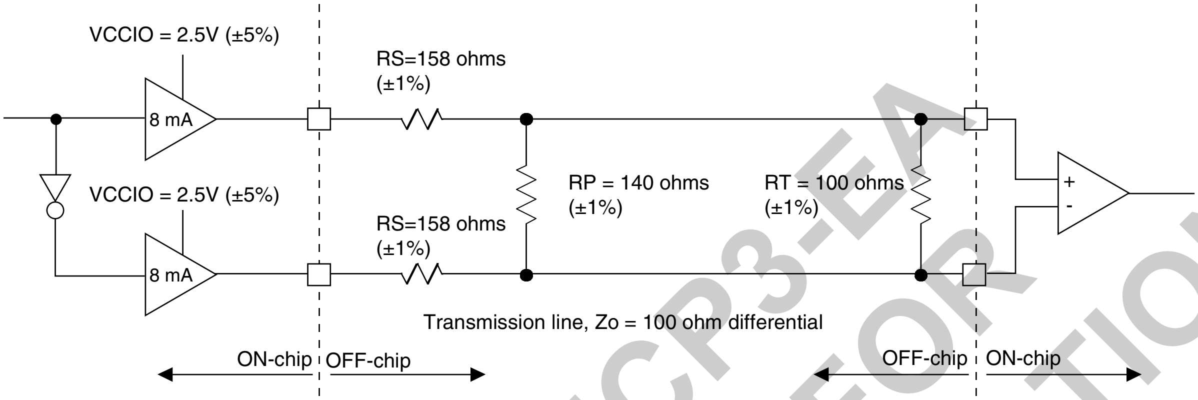


Table 3-1. LVDS25E DC Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (+/-1%)	158	Ω
R_P	Driver Parallel Resistor (+/-1%)	140	Ω
R_T	Receiver Termination (+/-1%)	100	Ω
V_{OH}	Output High Voltage	1.43	V
V_{OL}	Output Low Voltage	1.07	V
V_{OD}	Output Differential Voltage	0.35	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	6.03	mA

LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3V V_{CCIO}. The default drive current for LVCMOS33D output is 12mA with the option to change the device strength to 4mA, 8mA, 16mA or 20mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.

RSDS25E

The LatticeECP3 devices support differential RSDS and RSDSE standards. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS25E (Reduced Swing Differential Signaling)

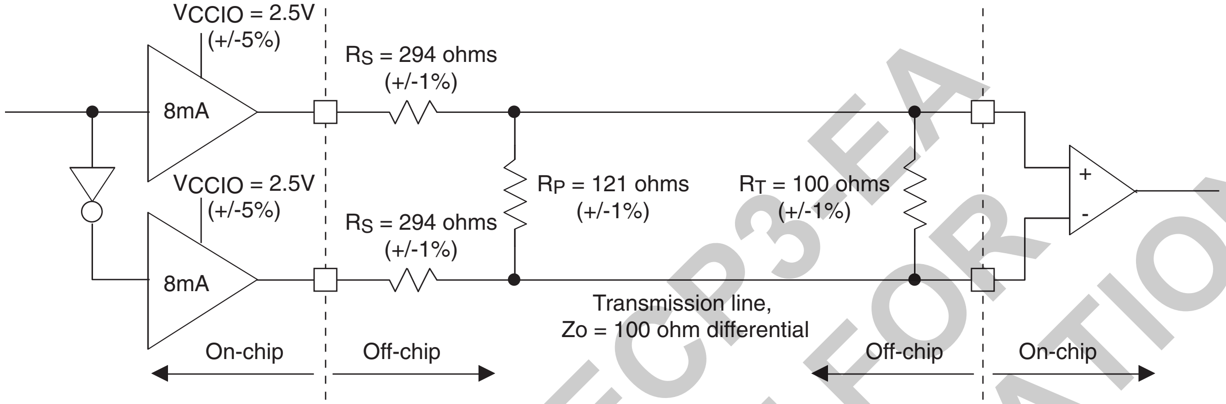


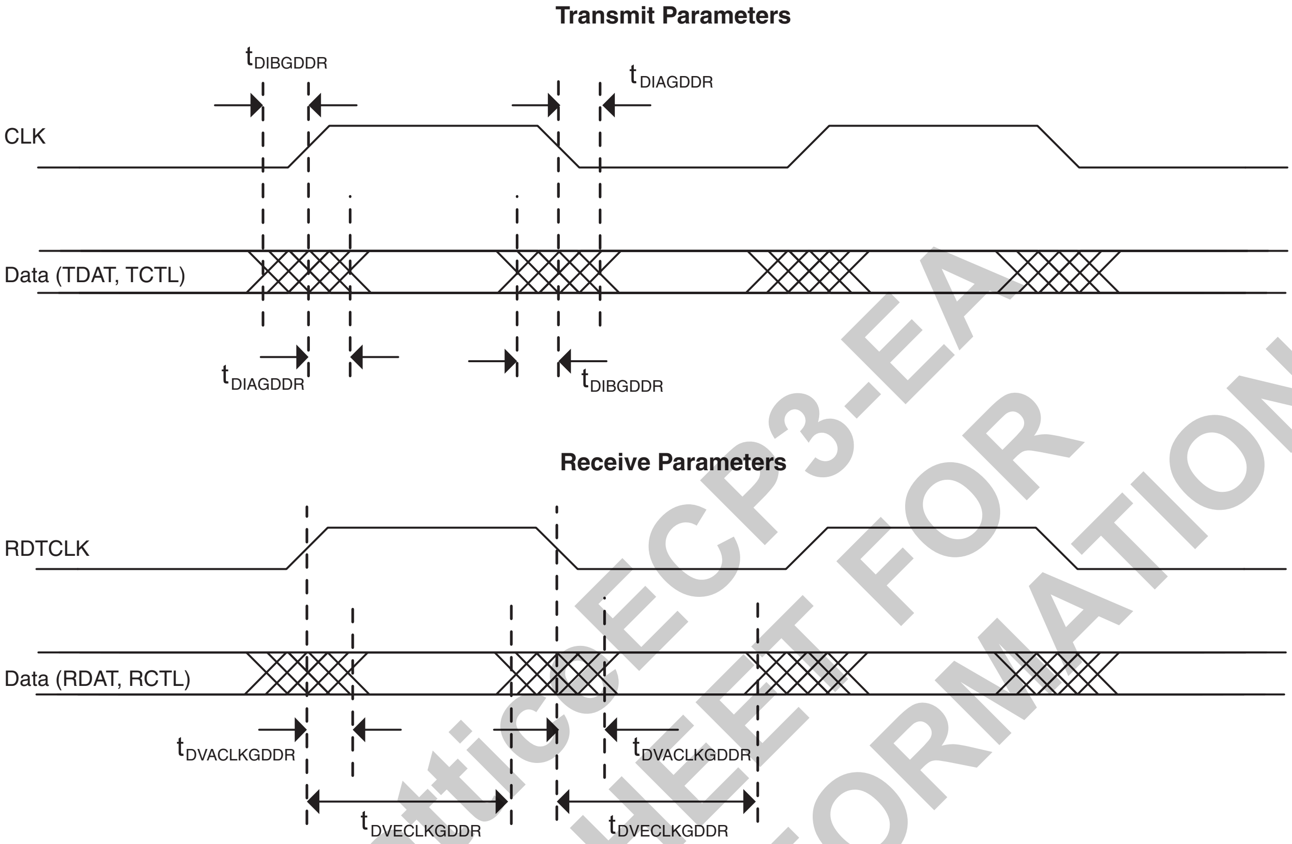
Table 3-4. RSDS25E DC Conditions[1]

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (+/-1%)	294	Ω
R_P	Driver Parallel Resistor (+/-1%)	121	Ω
R_T	Receiver Termination (+/-1%)	100	Ω
V_{OH}	Output High Voltage	1.35	V
V_{OL}	Output Low Voltage	1.15	V
V_{OD}	Output Differential Voltage	0.20	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	101.5	Ω
I_{DC}	DC Output Current	3.66	mA

1. For input buffer, see LVDS table.

Figure 3-6. Generic DDR/DDR2 (With Clock and Data Edges Aligned)



LatticeECP3 Internal Switching Characteristics[1, 2] (Continued)

Over Recommended Commercial Operating Conditions

Parameter	Description	-8		-7		-6		Units.
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{HWREN_EBR}	Hold Write/Read Enable to PFU Memory	0.141	—	0.145	—	0.149	—	ns
t_{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.087		0.096		0.104		ns
t_{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.066		-0.080		-0.094		ns
t_{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	-0.071		-0.070		-0.068		ns
t_{HBE_EBR}	Byte Enable Hold Time to EBR Output Register	0.118		0.098		0.077		ns
DSP Block Timing[3]								
t_{SUI_DSP}	Input Register Setup Time	0.32	—	0.36	—	0.39	—	ns
t_{HI_DSP}	Input Register Hold Time	-0.17	—	-0.19	—	-0.21	—	ns
t_{SUP_DSP}	Pipeline Register Setup Time	2.23	—	2.30	—	2.37	—	ns
t_{HP_DSP}	Pipeline Register Hold Time	-1.02	—	-1.09	—	-1.15	—	ns
t_{SUO_DSP}	Output Register Setup Time	3.09	—	3.22	—	3.34	—	ns
t_{HO_DSP}	Output Register Hold Time	-1.67	—	-1.76	—	-1.84	—	ns
t_{COI_DSP}	Input Register Clock to Output Time	—	3.68	—	4.03	—	4.38	ns
t_{COP_DSP}	Pipeline Register Clock to Output Time	—	1.30	—	1.47	—	1.64	ns
t_{COO_DSP}	Output Register Clock to Output Time	—	0.58	—	0.60	—	0.62	ns
t_{SUOPT_DSP}	Opcode Register Setup Time	0.31	—	0.35	—	0.39	—	ns
t_{HOPT_DSP}	Opcode Register Hold Time	-0.20	—	-0.24	—	-0.27	—	ns
t_{SUDATA_DSP}	Cascade_data through ALU to Output Register Setup Time	1.55	—	1.67	—	1.78	—	ns
t_{HPDATA_DSP}	Cascade_data through ALU to Output Register Hold Time	-0.44	—	-0.53	—	-0.61	—	ns

1. Internal parameters are characterized but not tested on every device.
2. Commercial timing numbers are shown. Industrial timing numbers are typically slower and can be extracted from the ispLEVER software.
3. DSP slice is configured in Multiply Add/Sub 18x18 mode.
4. The output register is in Flip-flop mode.

LatticeECP3 Family Timing Adders[1, 2, 3, 4, 5] (Continued)

Over Recommended Commercial Operating Conditions

Buffer Type	Description	-8	-7	-6	Units
RSDS25	RSDS, VCCIO = 2.5V	0.05	0.10	0.16	ns
PPLVDS	Point-to-Point LVDS, Emulated, VCCIO = 2.5V	-0.10	-0.05	0.01	ns
LVPECL33	LVPECL, Emulated, VCCIO = 3.0V	-0.02	-0.04	-0.06	ns
HSTL18_I	HSTL_18 class I 8mA drive, VCCIO = 1.8V	-0.19	-0.16	-0.12	ns
HSTL18_II	HSTL_18 class II, VCCIO = 1.8V	-0.30	-0.28	-0.25	ns
HSTL18D_I	Differential HSTL 18 class I 8mA drive	-0.19	-0.16	-0.12	ns
HSTL18D_II	Differential HSTL 18 class II	-0.30	-0.28	-0.25	ns
HSTL15_I	HSTL_15 class I 4mA drive, VCCIO = 1.5V	-0.22	-0.19	-0.16	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	-0.22	-0.19	-0.16	ns
SSTL33_I	SSTL_3 class I, VCCIO = 3.0V	0.08	0.13	0.19	ns
SSTL33_II	SSTL_3 class II, VCCIO = 3.0V	-0.20	-0.17	-0.14	ns
SSTL33D_I	Differential SSTL_3 class I	0.08	0.13	0.18	ns
SSTL33D_II	Differential SSTL_3 class II	-0.20	-0.17	-0.14	ns
SSTL25_I	SSTL_2 class I 8mA drive, VCCIO = 2.5V	-0.06	-0.02	0.02	ns
SSTL25_II	SSTL_2 class II 16mA drive, VCCIO = 2.5V	-0.19	-0.15	-0.12	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.06	-0.02	0.02	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.19	-0.15	-0.12	ns
SSTL18_I	SSTL_1.8 class I, VCCIO = 1.8V	-0.14	-0.10	-0.07	ns
SSTL18_II	SSTL_1.8 class II 8mA drive, VCCIO = 1.8V	-0.20	-0.17	-0.14	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.14	-0.10	-0.07	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.20	-0.17	-0.14	ns
SSTL15	SSTL_1.5, VCCIO = 1.5V	0.07	0.08	0.08	ns
SSTL15D	Differential SSTL_15	0.07	0.08	0.08	ns
LVTTL33_4mA	LVTTL 4mA drive, VCCIO = 3.0V	0.21	0.23	0.25	ns
LVTTL33_8mA	LVTTL 8mA drive, VCCIO = 3.0V	0.09	0.09	0.10	ns
LVTTL33_12mA	LVTTL 12mA drive, VCCIO = 3.0V	0.02	0.03	0.03	ns
LVTTL33_16mA	LVTTL 16mA drive, VCCIO = 3.0V	0.12	0.13	0.13	ns
LVTTL33_20mA	LVTTL 20mA drive, VCCIO = 3.0V	0.08	0.08	0.09	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, fast slew rate	0.21	0.23	0.25	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, fast slew rate	0.09	0.09	0.10	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, fast slew rate	0.02	0.03	0.03	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, fast slew rate	0.12	0.13	0.13	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, fast slew rate	0.08	0.08	0.09	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, fast slew rate	0.12	0.12	0.12	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, fast slew rate	0.05	0.05	0.05	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, fast slew rate	0.08	0.08	0.08	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, fast slew rate	0.04	0.04	0.04	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, fast slew rate	0.08	0.09	0.09	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, fast slew rate	0.02	0.01	0.01	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, fast slew rate	-0.03	-0.03	-0.03	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, fast slew rate	0.03	0.03	0.03	ns

SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-19. Transmit

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
BR_{SDO}	Serial data rate		270	—	2975	Mbps
$T_{JALIGNMENT}$ [2]	Serial output jitter, alignment	270 Mbps	—	—	0.20	UI
$T_{JALIGNMENT}$ [2]	Serial output jitter, alignment	1485 Mbps	—	—	0.20	UI
$T_{JALIGNMENT}$ [1, 2]	Serial output jitter, alignment	2970Mbps	—	—	0.30	UI
$T_{JTIMING}$	Serial output jitter, timing	270 Mbps	—	—	0.20	UI
$T_{JTIMING}$	Serial output jitter, timing	1485 Mbps	—	—	1.0	UI
$T_{JTIMING}$	Serial output jitter, timing	2970 Mbps	—	—	2.0	UI

Notes:

1. Timing jitter is measured in accordance with SMPTE RP 184-1996, SMPTE RP 192-1996 and the applicable serial data transmission standard, SMPTE 259M-1997 or SMPTE 292M (proposed). A color bar test pattern is used.The value of f_{SCLK} is 270 MHz or 360 MHz for SMPTE 259M, 540 MHz for SMPTE 344M or 1485 MHz for SMPTE 292M serial data rates. See the Timing Jitter Bandpass section.
2. Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.
3. All Tx jitter is measured at the output of an industry standard cable driver; connection to the cable driver is via a 50 ohm impedance differential signal from the Lattice SERDES device.
4. The cable driver drives: RL=75 ohm, AC-coupled at 270, 1485, or 2970 Mbps, RREFLVL=RREFPRE=4.75kohm 1%.

Table 3-20. Receive

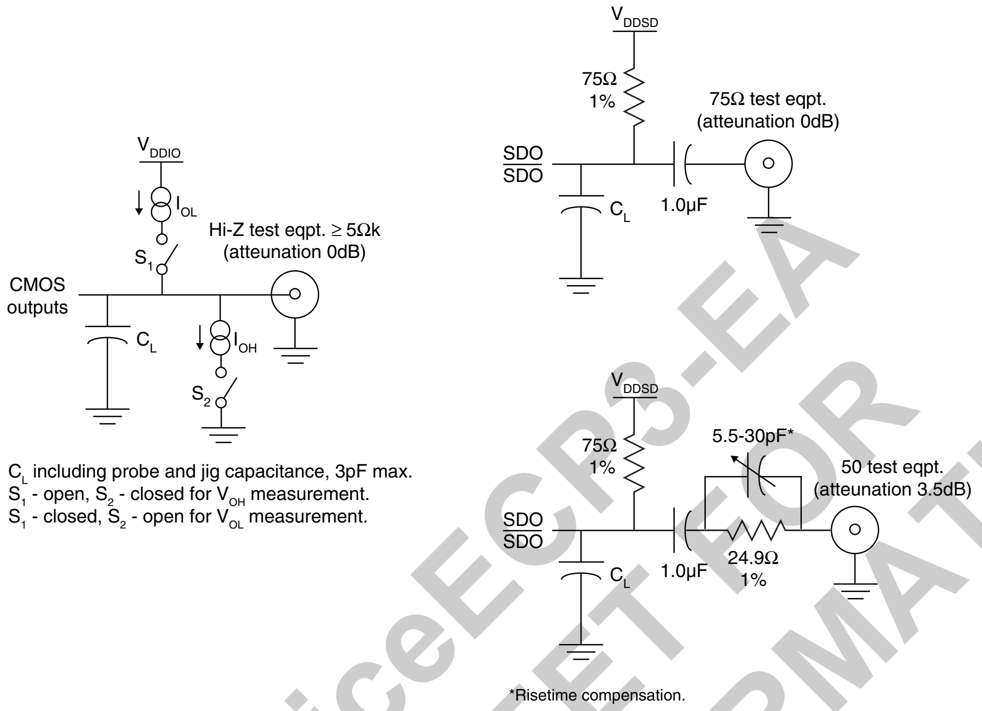
Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
BR_{SDI}	Serial input data rate		270	—	2970	Mbps
CID	Stream of non-transitions (=Consecutive Identical Digits)		7(3G)/26(SMPTE Triple rates) @ 10-12 BER	—	—	Bits

Table 3-21. Reference Clock

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
F_{VCLK}	Video output clock frequency		27	—	74.25	MHz
DC_V	Duty cycle, video clock		45	50	55	%

Figure 3-15. Test Loads

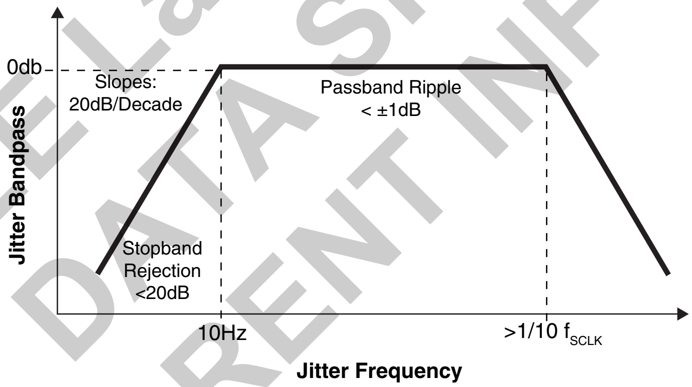
Test Loads



C_L including probe and jig capacitance, 3pF max.
S_1 - open, S_2 - closed for V_{OH} measurement.
S_1 - closed, S_2 - open for V_{OL} measurement.

*Risetime compensation.

Timing Jitter Bandpass



Pin Information Summary

Pin Information Summary		ECP3-17EA		ECP3-35EA			ECP3-70E/EA		
Pin Type		256 ftBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA	1156 fpBGA
General Purpose Inputs/Outputs per Bank	Bank 0	26	36	26	42	48	42	60	86
	Bank 1	14	24	14	36	36	36	48	78
	Bank 2	6	12	6	24	24	24	34	36
	Bank 3	18	44	16	54	59	54	59	86
	Bank 6	20	44	18	63	61	63	67	86
	Bank 7	19	32	19	36	42	36	48	54
	Bank 8	24	24	24	24	24	24	24	24
General Purpose Inputs per Bank	Bank 0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0
	Bank 2	2	2	2	4	4	4	8	8
	Bank 3	0	0	2	4	4	4	12	12
	Bank 6	0	0	2	4	4	4	12	12
	Bank 7	4	4	4	4	4	4	8	8
	Bank 8	0	0	0	0	0	0	0	0
General Purpose Outputs per Bank	Bank 0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0
	Bank 2	0	0	0	0	0	0	0	0
	Bank 3	0	0	0	0	0	0	0	0
	Bank 6	0	0	0	0	0	0	0	0
	Bank 7	0	0	0	0	0	0	0	0
	Bank 8	0	0	0	0	0	0	0	0
Total Single-Ended User I/O		133	222	133	295	310	295	380	490
VCC		6	16	6	16	32	16	32	32
VCCAUX		4	8	4	8	12	8	12	16
VTT		4	4	4	4	4	4	4	8
VCCA		4	4	4	4	8	4	8	16
VCCPLL		2	4	2	4	4	4	4	4
VCCIO	Bank 0	2	2	2	2	4	2	4	4
	Bank 1	2	2	2	2	4	2	4	4
	Bank 2	2	2	2	2	4	2	4	4
	Bank 3	2	2	2	2	4	2	4	4
	Bank 6	2	2	2	2	4	2	4	4
	Bank 7	2	2	2	2	4	2	4	4
	Bank 8	2	2	2	2	2	2	2	2
VCCJ		1	1	1	1	1	1	1	1
TAP		4	4	4	4	4	4	4	4
GND, GNDIO		50	98	50	98	139	98	139	233
NC		0	73	0	0	96	0	0	238
Reserved[1]		0	2	0	2	2	2	2	2
SERDES		26	26	26	26	26	26	52	78
Miscellaneous Pins		8	8	8	8	8	8	8	8
Total Bonded Pins		256	484	256	484	672	484	672	1156

Logic Signal Connections

Package pinout information can be found under “Data Sheets” on the LatticeECP3 product pages on the Lattice website at www.latticesemi.com/products/fpga/ecp3 and in the Lattice ispLEVER Design Planner software. To create pinout information from within Design Planner, select **View -> Package View**. Then select **Select File -> Export** and choose a type of output file. See Design Planner help for more information.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1181, Power Consumption and Management for LatticeECP3 Devices
- Power Calculator tool included with the Lattice ispLEVER design tool, or as a standalone download from www.latticesemi.com/software