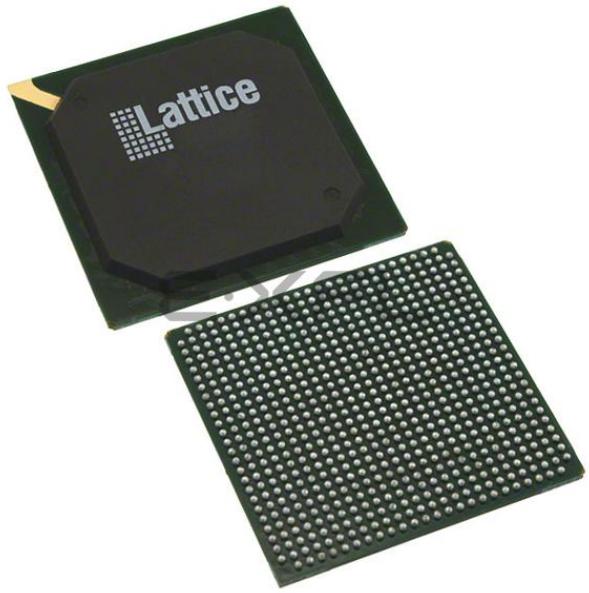

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8375
Number of Logic Elements/Cells	67000
Total RAM Bits	4526080
Number of I/O	380
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-70e-7fn672i

LatticeECP3 Family Data Sheet Introduction

November 2009 Preliminary Data Sheet DS1021

Features

- **Higher Logic Density for Increased System Integration**
  - 17K to 149K LUTs
  - 133 to 586 I/Os
- **Embedded SERDES**
  - 150 Mbps to 3.2 Gbps for Generic 8b10b, 10-bit SERDES, and 8-bit SERDES modes
  - Data Rates 230 Mbps to 3.2 Gbps per channel for all other protocols
  - Up to 16 channels per device: PCI Express, SONET/SDH, Ethernet (1GbE, SGMII, XAUI), CPRI, SMPTE 3G and Serial RapidIO
- **sysDSP™**
  - Fully cascadable slice architecture
  - 12 to 160 slices for high performance multiply and accumulate
  - Powerful 54-bit ALU operations
  - Time Division Multiplexing MAC Sharing
  - Rounding and truncation
  - Each slice supports
    - Half 36x36, two 18x18 or four 9x9 multipliers
    - Advanced 18x36 MAC and 18x18 Multiply-Multiply-Accumulate (MMAC) operations
- **Flexible Memory Resources**
  - Up to 6.85Mbits sysMEM™ Embedded Block RAM (EBR)
  - 36K to 303K bits distributed RAM
- **sysCLOCK Analog PLLs and DLLs**
  - Two DLLs and up to ten PLLs per device
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
  - Dedicated read/write levelling functionality
  - Dedicated gearing logic
  - Source synchronous standards support
    - ADC/DAC, 7:1 LVDS, XGMII
    - High Speed ADC/DAC devices
  - Dedicated DDR/DDR2/DDR3 memory with DQS support
  - Optional Inter-Symbol Interference (ISI) correction on outputs
- **Programmable sysI/O™ Buffer Supports Wide Range of Interfaces**
  - On-chip termination
  - Optional equalization filter on inputs
  - LVTTL and LVCMOS 33/25/18/15/12
  - SSTL 33/25/18/15 I, II
  - HSTL15 I and HSTL18 I, II
  - PCI and Differential HSTL, SSTL
  - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS
- **Flexible Device Configuration**
  - Dedicated bank for configuration I/Os
  - SPI boot flash interface
  - Dual-boot images supported
  - Slave SPI
  - TransFR™ I/O for simple field updates
  - Soft Error Detect embedded macro
- **System Level Support**
  - IEEE 1149.1 and IEEE 1532 compliant
  - Reveal Logic Analyzer
  - ORCAstra FPGA configuration utility
  - On-chip oscillator for initialization & general use
  - 1.2V core power supply

Table 1-1. LatticeECP3™ Family Selection Guide

Device	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
LUTs (K)	17	33	67	92	149
sysMEM Blocks (18Kbits)	38	72	240	240	372
Embedded Memory (Kbits)	700	1327	4420	4420	6850
Distributed RAM Bits (Kbits)	36	68	145	188	303
18X18 Multipliers	24	64	128	128	320
SERDES (Quad)	1	1	3	3	4
PLLs/DLLs	2 / 2	4 / 2	10 / 2	10 / 2	10 / 2
Packages and SERDES Channels/ I/O Combinations					
256 ftBGA (17x17 mm)	4 / 133	4 / 133			
484 fpBGA (23x23 mm)	4 / 222	4 / 295	4 / 295	4 / 295	
672 fpBGA (27x27 mm)		4 / 310	8 / 380	8 / 380	8 / 380
1156 fpBGA (35x35 mm)			12 / 490	12 / 490	16 / 586

ROM Mode
ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, please refer to TN1179, LatticeECP3 Memory Usage Guide.

Routing

There are many resources provided in the LatticeECP3 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The LatticeECP3 family has an enhanced routing architecture that produces a compact design. The ispLEVER design tool suite takes the output of the synthesis tool and places and routes the design.

sysCLOCK PLLs and DLLs

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. All the devices in the LatticeECP3 family support four to ten full-featured General Purpose PLLs.

General Purpose PLL

The architecture of the PLL is shown in Figure 2-4. A description of the PLL functionality follows.

CLKI is the reference frequency (generated either from the pin or from routing) for the PLL. CLKI feeds into the Input Clock Divider block. The CLKFB is the feedback signal (generated from CLKOP, CLKOS or from a user clock pin/logic). This signal feeds into the Feedback Divider. The Feedback Divider is used to multiply the reference frequency.

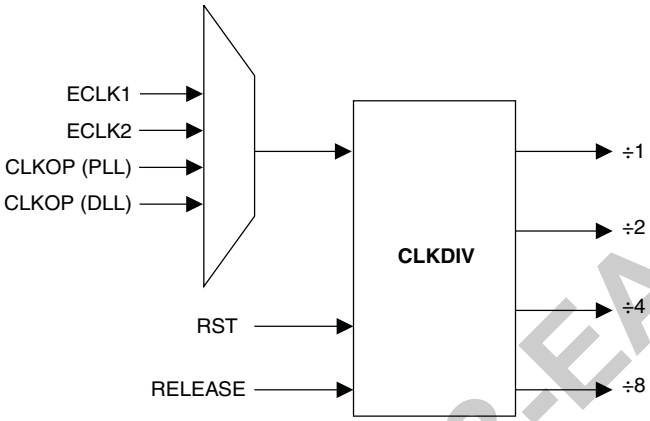
Both the input path and feedback signals enter the Voltage Controlled Oscillator (VCO) block. In this block the difference between the input path and feedback signals is used to control the frequency and phase of the oscillator. A LOCK signal is generated by the VCO to indicate that the VCO has locked onto the input clock signal. In dynamic mode, the PLL may lose lock after a dynamic delay adjustment and not relock until the t_{LOCK} parameter has been satisfied.

The output of the VCO then enters the CLKOP divider. The CLKOP divider allows the VCO to operate at higher frequencies than the clock output (CLKOP), thereby increasing the frequency range. The Phase/Duty Select block adjusts the phase and duty cycle of the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted. A secondary divider takes the CLKOP or CLKOS signal and uses it to derive lower frequency outputs (CLKOK).

The primary output from the CLKOP divider (CLKOP) along with the outputs from the secondary dividers (CLKOK and CLKOK2) and Phase/Duty select (CLKOS) are fed to the clock distribution network.

The PLL allows two methods for adjusting the phase of signal. The first is referred to as Fine Delay Adjustment. This inserts up to 16 nominal 125ps delays to be applied to the secondary PLL output. The number of steps may be set statically or from the FPGA logic. The second method is referred to as Coarse Phase Adjustment. This allows the phase of the rising and falling edge of the secondary PLL output to be adjusted in 22.5 degree steps. The number of steps may be set statically or from the FPGA logic.

Figure 2-8. Clock Divider Connections



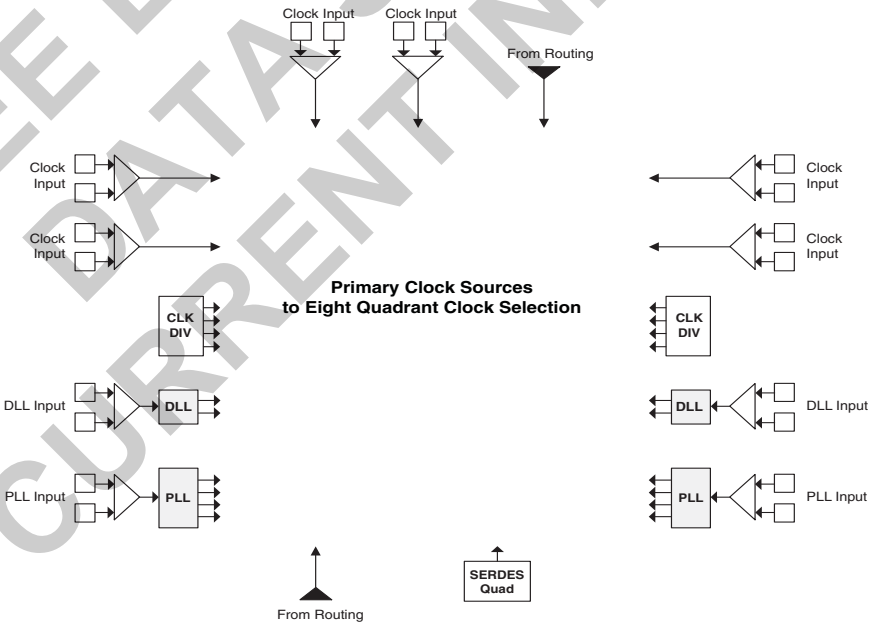
Clock Distribution Network

LatticeECP3 devices have eight quadrant-based primary clocks and eight secondary clock/control sources. Two high performance edge clocks are available on the top, left, and right edges of the device to support high speed interfaces. These clock sources are selected from external I/Os, the sysCLOCK PLLs, DLLs or routing. These clock sources are fed throughout the chip via a clock distribution system.

Primary Clock Sources

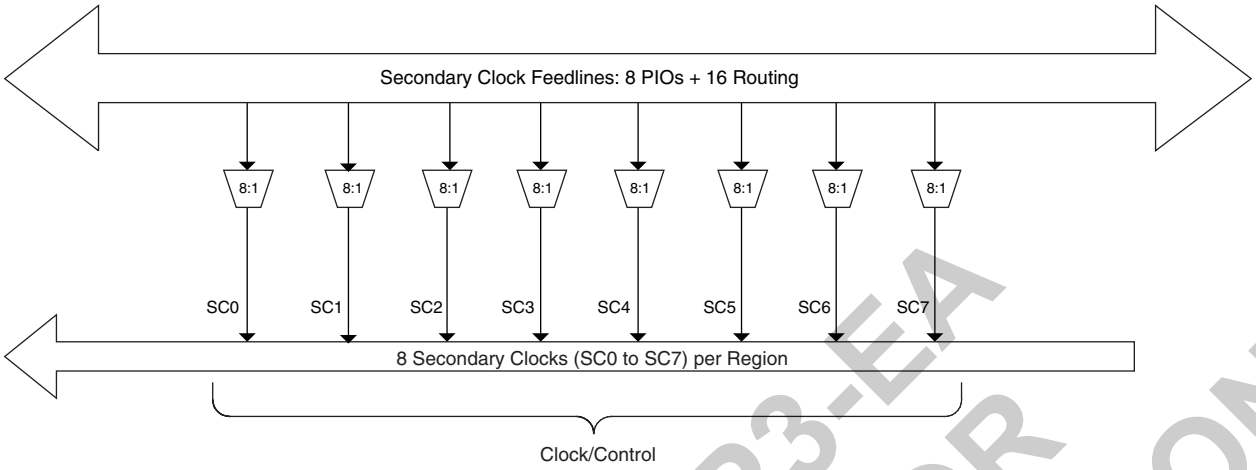
LatticeECP3 devices derive clocks from six primary source types: PLL outputs, DLL outputs, CLKDIV outputs, dedicated clock inputs, routing and SERDES Quads. LatticeECP3 devices have two to ten sysCLOCK PLLs and two DLLs, located on the left and right sides of the device. There are six dedicated clock inputs: two on the top side, two on the left side and two on the right side of the device. Figures 2-9, 2-10 and 2-11 show the primary clock sources for LatticeECP3 devices.

Figure 2-9. Primary Clock Sources for LatticeECP3-17



Note: Clock inputs can be configured in differential or single-ended mode.

Figure 2-16. Per Region Secondary Clock Selection



Slice Clock Selection

Figure 2-17 shows the clock selections and Figure 2-18 shows the control selections for Slice0 through Slice2. All the primary clocks and seven secondary clocks are routed to this clock selection mux. Other signals can be used as a clock input to the slices via routing. Slice controls are generated from the secondary clocks/controls or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-17. Slice0 through Slice2 Clock Selection

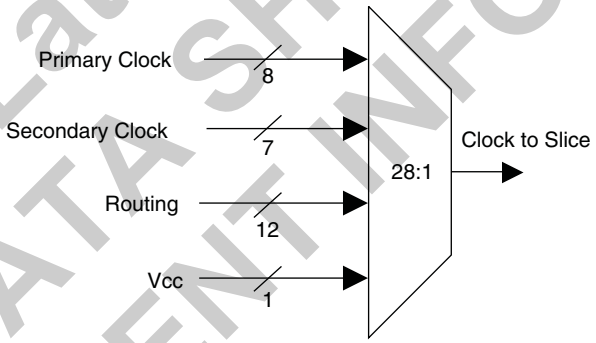


Figure 2-18. Slice0 through Slice2 Control Selection

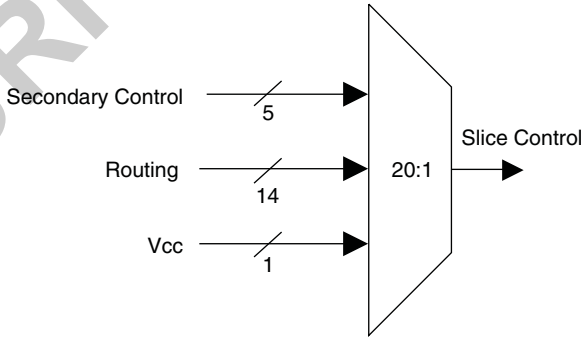
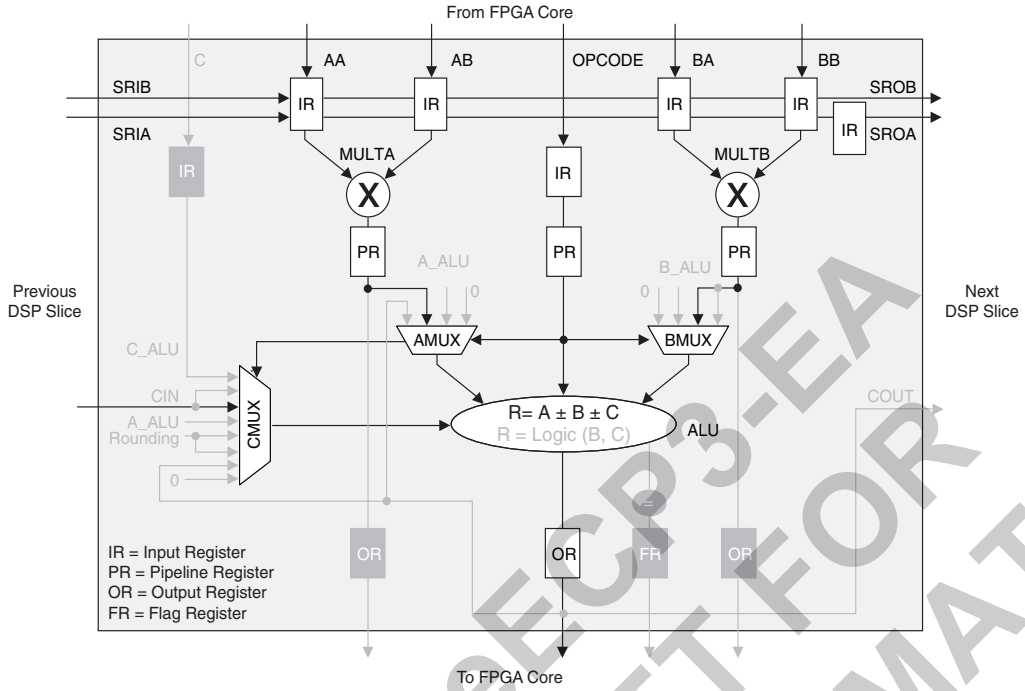


Figure 2-31. MULTADDSUBSUM Slice 1



Advanced sysDSP Slice Features

Cascading

The LatticeECP3 sysDSP slice has been enhanced to allow cascading. Adder trees are implemented fully in sysDSP slices, improving the performance. Cascading of slices uses the signals CIN, COUT and C Mux of the slice.

Addition

The LatticeECP3 sysDSP slice allows for the bypassing of multipliers and cascading of adder logic. High performance adder functions are implemented without the use of LUTs. The maximum width adders that can be implemented are 54-bit.

Rounding

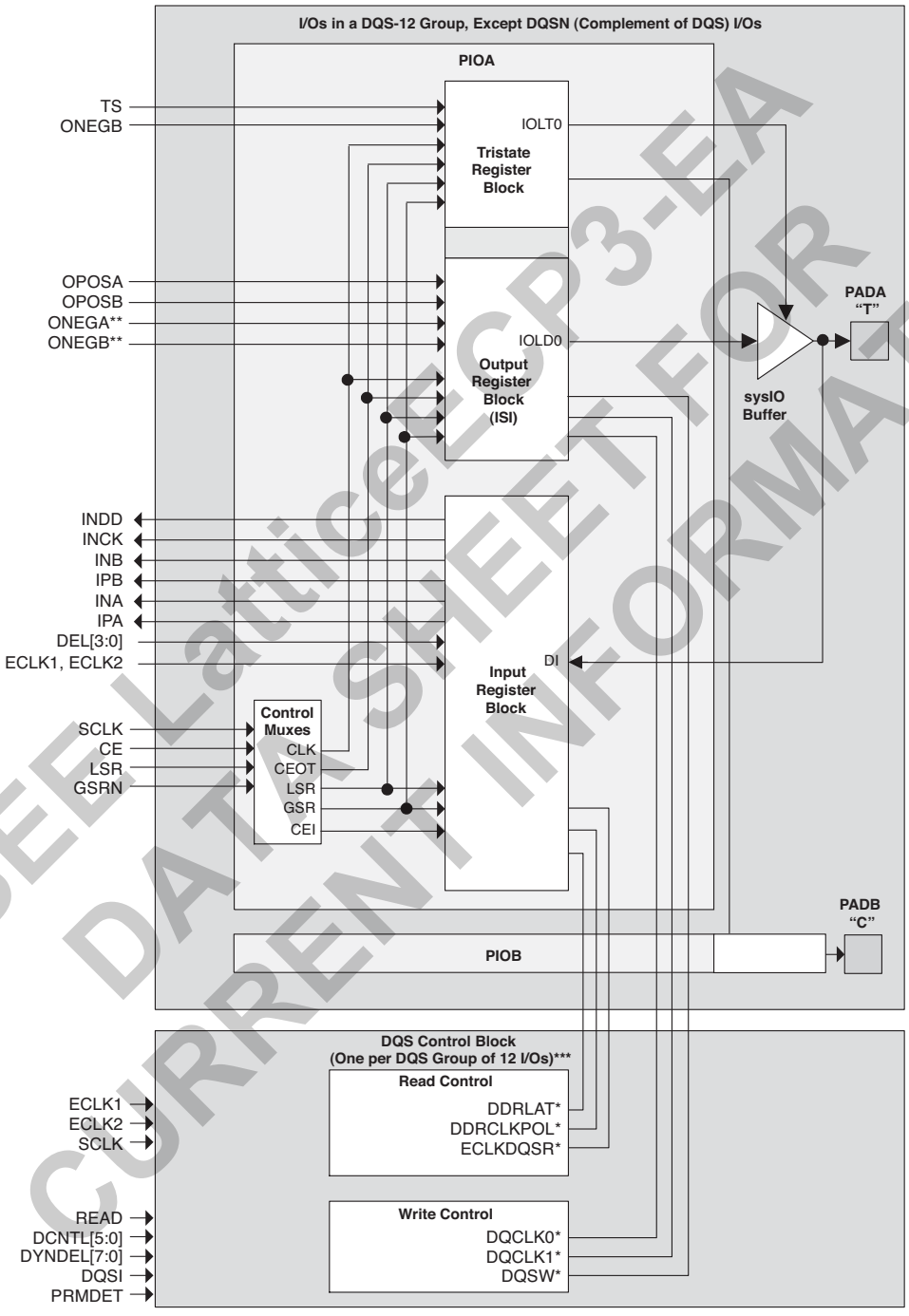
The rounding operation is implemented in the ALU and is done by adding a constant followed by a truncation operation. The rounding methods supported are:

- Rounding to zero (RTZ)
- Rounding to infinity (RTI)
- Dynamic rounding
- Random rounding
- Convergent rounding

Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O buffers as shown in Figure 2-32. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysI/O buffer and receives input from the buffer. Table 2-11 provides the PIO signal list.

Figure 2-32. PIC Diagram



* Signals are available on left/right/top edges only.
** Signals are available on the left and right sides only
*** Selected PIO.

Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block.

DDR Memory Support

Certain PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR1, DDR2 and DDR3 memory interfaces. The support varies by the edge of the device as detailed below.

Left and Right Edges

The left and right sides of the PIC have fully functional elements supporting DDR1, DDR2, and DDR3 memory interfaces. One of every 12 PIOs supports the dedicated DQS pins with the DQS control logic block. Figure 2-35 shows the DQS bus spanning 11 I/O pins. Two of every 12 PIOs support the dedicated DQS and DQS# pins with the DQS control logic block.

Bottom Edge

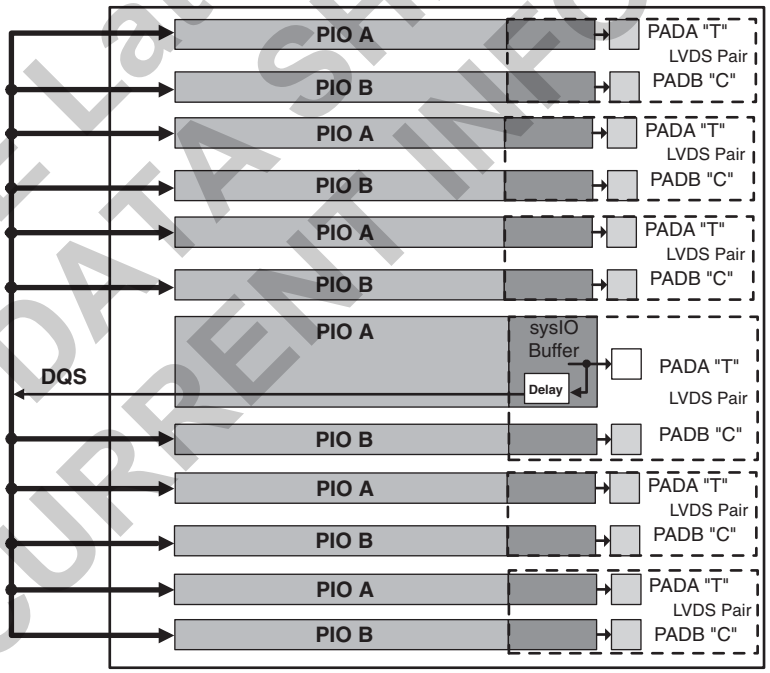
PICs on the bottom edge of the device do not support DDR memory and Generic DDR interfaces.

Top Edge

PICs on the top side are similar to the PIO elements on the left and right sides but do not support gearing on the output registers. Hence, the modes to support output/tristate DDR3 memory are removed on the top side.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left, right and top edges are designed for DDR memories that support 10 bits of data.

Figure 2-35. DQS Grouping on the Left, Right and Top Edges



DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces, a PLL is used for this adjustment. However, in DDR memories the clock

To accomplish write leveling in DDR3, each DQS group has a slightly different delay that is set by DYN DELAY[7:0] in the DQS Write Control logic block. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock.

LatticeECP3 input and output registers can also support DDR gearing that is used to receive and transmit the high speed DDR data from and to the DDR3 Memory.

LatticeECP3 supports the 1.5V SSTL I/O standard required for the DDR3 memory interface. In addition, it supports on-chip termination to VTT on the DDR3 memory input pins. For more information, refer to the sysIO section of this data sheet.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on DDR Memory interface implementation in LatticeECP3.

sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVDS, BLVDS, HSTL, SSTL Class I & II, LVCMOS, LVTTL, LVPECL, PCI.

sysI/O Buffer Banks

LatticeECP3 devices have six sysI/O buffer banks: six banks for user I/Os arranged two per side. The banks on the bottom side are wraparounds of the banks on the lower right and left sides. The seventh sysI/O buffer bank (Configuration Bank) is located adjacent to Bank 2 and has dedicated/shared I/Os for configuration. When a shared pin is not used for configuration it is available as a user I/O. Each bank is capable of supporting multiple I/O standards. Each sysI/O bank has its own I/O supply voltage (V_{CCIO}). In addition, each bank, except the Configuration Bank, has voltage references, V_{REF1} and V_{REF2}, which allow it to be completely independent from the others. The Configuration Bank top side shares V_{REF1} and V_{REF2} from sysI/O bank 1 and right side shares V_{REF1} and V_{REF2} from sysI/O bank 2. Figure 2-38 shows the seven banks and their associated supplies.

In LatticeECP3 devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using V_{CCIO}. LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO}.

Each bank can support up to two separate V_{REF} voltages, V_{REF1} and V_{REF2}, that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Figure 2-40. SERDES/PCS Quads (LatticeECP3-150)

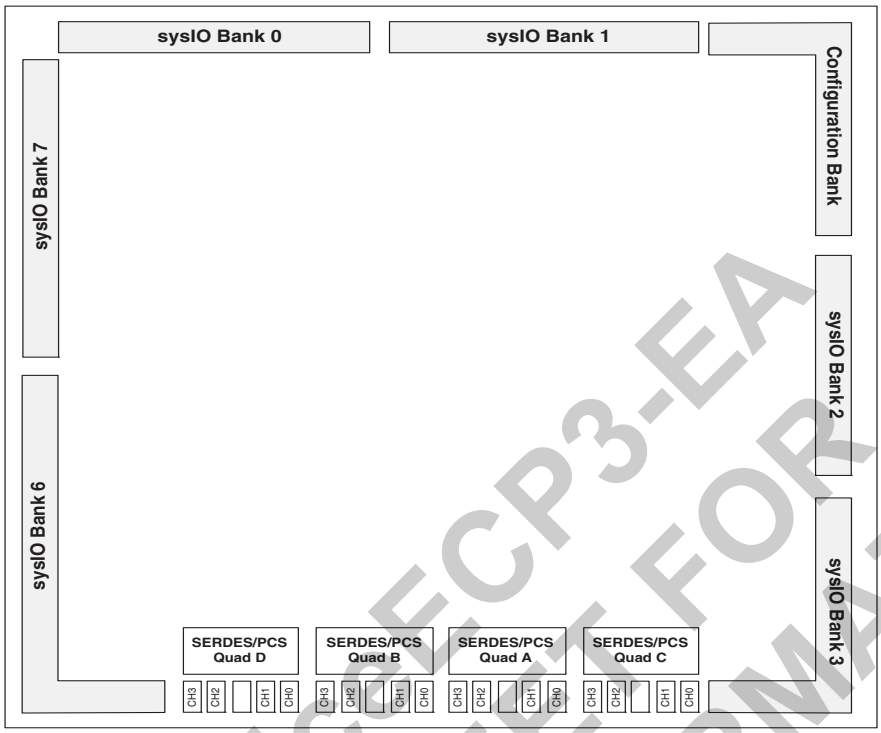


Table 2-13. LatticeECP3 SERDES Standard Support

Standard	Data Rate (Mbps)	Number of General/Link Width	Encoding Style
PCI Express 1.1	2500	x1, x2, x4	8b10b
Gigabit Ethernet	1250, 2500	x1	8b10b
SGMII	1250	x1	8b10b
XAUI	3125	x4	8b10b
Serial RapidIO Type I, Serial RapidIO Type II, Serial RapidIO Type III	1250, 2500, 3125	x1, x4	8b10b
CPRI-1, CPRI-2, CPRI-3, CPRI-4	614.4, 1228.8, 2457.6, 3072.0	x1	8b10b
SD-SDI (259M, 344M)	143[1], 177[1], 270, 360, 540	x1	NRZI/Scrambled
HD-SDI (292M)	1483.5, 1485	x1	NRZI/Scrambled
3G-SDI (424M)	2967, 2970	x1	NRZI/Scrambled
SONET-STS-3[2]	155.52	x1	N/A
SONET-STS-12[2]	622.08	x1	N/A
SONET-STS-48[2]	2488	x1	N/A

1. For slower rates, the SERDES are bypassed and CML signals are directly connected to the FPGA routing.
2. The SONET protocol is supported in 8-bit SERDES mode. See TN1176 Lattice ECP3 SERDES/PCS Usage Guide for more information.

The ispLEVER design tools from Lattice support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With ispLEVER, the user can define the mode for each quad in a design.

Popular standards such as 10Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), a single quad (Four SERDES channels and PCS) and some additional logic from the core.

The LatticeECP3 family also supports a wide range of primary and secondary protocols. Within the same quad, the LatticeECP3 family can support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. Table 2-15 lists the allowable combination of primary and secondary protocol combinations.

Flexible Quad SERDES Architecture

The LatticeECP3 family SERDES architecture is a quad-based architecture. For most SERDES settings and standards, the whole quad (consisting of four SERDES) is treated as a unit. This helps in silicon area savings, better utilization and overall lower cost.

However, for some specific standards, the LatticeECP3 quad architecture provides flexibility; more than one standard can be supported within the same quad.

Table 2-15 shows the standards can be mixed and matched within the same quad. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same quad. In Table 2-15, the Primary Protocol column refers to the standard that determines the reference clock and PLL settings. The Secondary Protocol column shows the other standard that can be supported within the same quad.

Furthermore, Table 2-15 also implies that more than two standards in the same quad can be supported, as long as they conform to the data rate and reference clock requirements. For example, a quad may contain PCI Express 1.1, SGMII, Serial RapidIO Type I and Serial RapidIO Type II, all in the same quad.

Table 2-15. LatticeECP3 Primary and Secondary Protocol Support

Primary Protocol	Secondary Protocol
PCI Express 1.1	SGMII
PCI Express 1.1	Gigabit Ethernet
PCI Express 1.1	Serial RapidIO Type I
PCI Express 1.1	Serial RapidIO Type II
Serial RapidIO Type I	SGMII
Serial RapidIO Type I	Gigabit Ethernet
Serial RapidIO Type II	SGMII
Serial RapidIO Type II	Gigabit Ethernet
Serial RapidIO Type II	Serial RapidIO Type I
CPRI-3	CPRI-2 and CPRI-1
3G-SDI	HD-SDI and SD-SDI

For further information on SERDES, please see TN1176, LatticeECP3 SERDES/PCS Usage Guide.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeECP3 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test

sysI/O Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS33[2]	3.135	3.3	3.465	—	—	—
LVCMOS25[2]	2.375	2.5	2.625	—	—	—
LVCMOS18	1.71	1.8	1.89	—	—	—
LVCMOS15	1.425	1.5	1.575	—	—	—
LVCMOS12[2]	1.14	1.2	1.26	—	—	—
LVTTL33[2]	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
SSTL15[3]	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, II[2]	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I, II[2]	2.375	2.5	2.625	1.15	1.25	1.35
SSTL33_I, II[2]	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15_I[2]	1.425	1.5	1.575	0.68	0.75	0.9
HSTL18_I, II[2]	1.71	1.8	1.89	0.816	0.9	1.08
LVDS25[2]	2.375	2.5	2.625	—	—	—
MLVDS25[1]	2.375	2.5	2.625	—	—	—
LVPECL33[1, 2]	3.135	3.3	3.465	—	—	—
Mini LVDS	—	—	—	—	—	—
BLVDS25[1, 2]	2.375	2.5	2.625	—	—	—
RSDS25[1, 2]	2.375	2.5	2.625	—	—	—
RSDS25E[1, 2]	2.375	2.5	2.625	—	—	—
TRLVDS	3.14	3.3	3.47	—	—	—
PPLVDS	3.14/2.25	3.3/2.5	3.47/2.75	—	—	—
SSTL15D	1.43	1.5	1.57	—	—	—
SSTL18D_I[2], II[2]	1.71	1.8	1.89	—	—	—
SSTL25D_ I[2], II[2]	2.375	2.5	2.625	—	—	—
SSTL33D_ I[2], II[2]	3.135	3.3	3.465	—	—	—
HSTL15D_ I[2]	1.425	1.5	1.575	—	—	—
HSTL18D_ I[2], II[2]	1.71	1.8	1.89	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.
2. For input voltage compatibility, refer to the "Mixed Voltage Support" section of TN1177, LatticeECP3 sysIO Usage Guide.

sysI/O Differential Electrical Characteristics

LVDS25

Over Recommended Operating Conditions

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage		0	—	2.4	V
V_{CM}	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	+/-100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	+/-10	µA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.9V	1.03	—	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low		—	—	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100 Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50	mV
I_{SAB}	Output Short Circuit Current	V_{OD} = 0V Driver Outputs Shorted to Each Other	—	—	12	mA

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

LatticeECP3 External Switching Characteristics (Continued)[1, 2]

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-70E/95E	—	250	—	250	—	250	MHz
Generic DDRX1 Inputs with Clock and Data (<10 Bits Wide) Centered at Pin (GDDRX1_RX.DQS.Centered) Using DQS Pin for Clock Input									
Left, Right and Top for Data and Clock									
t_{SUGDDR}	Data Valid After CLK	ECP3-150EA		—		—		—	ns
t_{HGDDR}	Data Hold After CLK	ECP3-150EA		—		—		—	ns
f_{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-150EA	—		—		—		ns
Generic DDRX1 Inputs with Clock and Data (<10 Bits Wide) Aligned at Pin (GDDRX1_RX.DQS.Aligned) Using DQS Pin for Clock Input									
Left and Right Sides									
$t_{DVACLKGDDR}$	Data Setup Before CLK (Left and Right Sides)	ECP3-150EA	—		—		—		UI
$t_{DVECLKGDDR}$	Data Hold After CLK (Left and Right Sides)	ECP3-150EA		—		—		—	UI
f_{MAX_GDDR}	DDRX1 Clock Frequency (Left and Right Sides)	ECP3-150EA	—		—		—		UI
Top Side									
$t_{DVACLKGDDR}$	Data Setup Before CLK (Top Side)	ECP3-150EA	—		—		—		UI
$t_{DVECLKGDDR}$	Data Hold After CLK (Top Side)	ECP3-150EA		—		—		—	UI
f_{MAX_GDDR}	DDRX1 Clock Frequency (Top Side)	ECP3-150EA	—		—		—		UI
Generic DDRX2 Inputs with Clock and Data (>10 Bits Wide) Centered at Pin (GDDRX2_RX.ECLK.Centered) Using PCLK Pin for Clock Input									
Left and Right Sides									
t_{SUGDDR}	Data Setup Before CLK	ECP3-150EA		—		—		—	ns
t_{HGDDR}	Data Hold After CLK	ECP3-150EA		—		—		—	ns
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	—		—		—		MHz
Generic DDRX2 Inputs with Clock in the Center of Data Window, Without DLL[3] (GDDRX2_RX.ECLK.Centered)									
t_{SUGDDR}	Data Setup Before CLK	ECP3-70E/95E	260	—	312	—	352	—	ps
t_{HOGDDR}	Data Hold After CLK	ECP3-70E/95E	260	—	312	—	352	—	ps
f_{MAX_GDDR}	DDR/DDRX2 Clock Frequency[8]	ECP3-70E/95E	—	500	—	420	—	375	MHz
Generic DDRX2 Inputs with Clock and Data (>10 Bits Wide) Aligned at Pin (GDDRX2_RX.ECLK.Aligned)									
Left and Right Side Using DLLCLKIN Pin for Clock Input									
$t_{DVACLKGDDR}$	Data Setup Before CLK (Left and Right Side)	ECP3-150EA	—		—		—		UI
$t_{DVECLKGDDR}$	Data Hold After CLK (Left and Right Side)	ECP3-150EA		—		—		—	UI
f_{MAX_GDDR}	DDRX1 Clock Frequency (Left and Right Side)	ECP3-150EA	—		—		—		MHz
Top Side Using PCLK Pin for Clock Input									
$t_{DVACLKGDDR}$	Data Setup Before CLK (Top Side)	ECP3-150EA	—		—		—		UI
$t_{DVECLKGDDR}$	Data Hold After CLK (Top Side)	ECP3-150EA		—		—		—	UI
f_{MAX_GDDR}	DDRX1 Clock Frequency (Top Side)	ECP3-150EA	—		—		—		MHz
Generic DDRX2 Inputs with Clock and Data Edges Aligned, with DLLDEL[3] (GDDRX2_RX.ECLK.Aligned)									
$t_{DVACLKGDDR}$	Data Valid After CLK	ECP3-70E/95E	—	0.235	—	0.235	—	0.235	UI

LatticeECP3 External Switching Characteristics (Continued)[1, 2]

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-70E/95E	0.765	—	0.765	—	0.765	—	UI
f_{MAX_GDDR}	DDR/DDRX2 Clock Frequency[8]	ECP3-70E/95E	—	500	—	420	—	375	MHz
Generic DDRX2 Inputs with Clock and Data (<10 Bits Wide) Centered at Pin (GDDRX2_RX.DQS.Centered) using DQS Pin for Clock Input									
Left and Right Sides									
t_{SUGDDR}	Data Setup Before CLK	ECP3-150EA		—		—		—	ns
t_{HGDDR}	Data Hold After CLK	ECP3-150EA		—		—		—	ns
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	—		—		—		ns
Generic DDRX2 Inputs with Clock and Data (<10 Bits Side) Aligned at Pin (GDDRX2_RX.DQS.Aligned) Using DQS Pin for Clock Input									
Left and Right Sides									
$t_{DVACLKGDDR}$	Data Setup Before CLK (Left and Right Side)	ECP3-150EA	—		—		—		
$t_{DVECLKGDDR}$	Data Hold After CLK (Left and Right Side)	ECP3-150EA		—		—		—	
f_{MAX_GDDR}	DDRX2 Clock Frequency (Left and Right Side)	ECP3-150EA	—		—		—		
Generic DDRX1 Output with Clock and Data (>10 Bits Wide) Centered at Pin (GDDRX1_TX.SCLK.Centered)									
Left, Right and Top Sides									
$t_{DVBGDDR}$	Data Valid Before CLK	ECP3-150EA		—		—		—	
$t_{DVAGDDR}$	Data Valid After CLK	ECP3-150EA		—		—		—	
f_{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-150EA	—		—		—		
Generic DDRX1 Outputs with clock in the center of data window, with PLL 90-degree shifted clock ouput (GDDRX1_TX.ECLK.Centered)									
$t_{DIBGDDR}$	Data Invalid Before CLK	ECP3-70E/95E	670	—	670	—	670	—	ps
$t_{DIAGDDR}$	Data Invalid After CLK	ECP3-70E/95E	670	—	670	—	670	—	ps
fMAX_GDDR	DDRX1 Clock Frequency	ECP3-70E/95E	—	250	—	250	—	250	MHz
Generic DDRX1 Output with Clock and Data (> 10 Bits Wide) Aligned at Pin (GDDRX1_TX.SCLK.Aligned)									
Left, Right and Top Sides									
$t_{DIBGDDR}$	Data Hold After CLK	ECP3-150EA	—		—		—		
$t_{DIAGDDR}$	Data Setup Before CLK	ECP3-150EA	—		—		—		
f_{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-150EA	—		—		—		
Generic DDRX1 Outputs with clock and data edge aligned, without PLL									
$t_{DIBGDDR}$	Data Invalid Before CLK	ECP3-70E/95E	—	330	—	330	—	330	ps
$t_{DIAGDDR}$	Data Invalid After CLK	ECP3-70E/95E	—	330	—	330	—	330	ps
f_{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-70E/95E	—	250	—	250	—	250	MHz
Generic DDRX1 Output with Clock and Data (<10 Bits Wide) Centered at Pin (GDDRX1_TX.DQS.Centered)									
Left, Right and Top Sides									
$t_{DVBGDDR}$	Data Valid Before CLK	ECP3-150EA	—		—		—		
$t_{DVAGDDR}$	Data Valid After CLK	ECP3-150EA	—		—		—		
f_{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-150EA	—		—		—		

LatticeECP3 Family Timing Adders[1, 2, 3, 4, 5] (Continued)

Over Recommended Commercial Operating Conditions

Buffer Type	Description	-8	-7	-6	Units
RSDS25	RSDS, VCCIO = 2.5V	0.05	0.10	0.16	ns
PPLVDS	Point-to-Point LVDS, Emulated, VCCIO = 2.5V	-0.10	-0.05	0.01	ns
LVPECL33	LVPECL, Emulated, VCCIO = 3.0V	-0.02	-0.04	-0.06	ns
HSTL18_I	HSTL_18 class I 8mA drive, VCCIO = 1.8V	-0.19	-0.16	-0.12	ns
HSTL18_II	HSTL_18 class II, VCCIO = 1.8V	-0.30	-0.28	-0.25	ns
HSTL18D_I	Differential HSTL 18 class I 8mA drive	-0.19	-0.16	-0.12	ns
HSTL18D_II	Differential HSTL 18 class II	-0.30	-0.28	-0.25	ns
HSTL15_I	HSTL_15 class I 4mA drive, VCCIO = 1.5V	-0.22	-0.19	-0.16	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	-0.22	-0.19	-0.16	ns
SSTL33_I	SSTL_3 class I, VCCIO = 3.0V	0.08	0.13	0.19	ns
SSTL33_II	SSTL_3 class II, VCCIO = 3.0V	-0.20	-0.17	-0.14	ns
SSTL33D_I	Differential SSTL_3 class I	0.08	0.13	0.18	ns
SSTL33D_II	Differential SSTL_3 class II	-0.20	-0.17	-0.14	ns
SSTL25_I	SSTL_2 class I 8mA drive, VCCIO = 2.5V	-0.06	-0.02	0.02	ns
SSTL25_II	SSTL_2 class II 16mA drive, VCCIO = 2.5V	-0.19	-0.15	-0.12	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.06	-0.02	0.02	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.19	-0.15	-0.12	ns
SSTL18_I	SSTL_1.8 class I, VCCIO = 1.8V	-0.14	-0.10	-0.07	ns
SSTL18_II	SSTL_1.8 class II 8mA drive, VCCIO = 1.8V	-0.20	-0.17	-0.14	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.14	-0.10	-0.07	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.20	-0.17	-0.14	ns
SSTL15	SSTL_1.5, VCCIO = 1.5V	0.07	0.08	0.08	ns
SSTL15D	Differential SSTL_15	0.07	0.08	0.08	ns
LVTTL33_4mA	LVTTL 4mA drive, VCCIO = 3.0V	0.21	0.23	0.25	ns
LVTTL33_8mA	LVTTL 8mA drive, VCCIO = 3.0V	0.09	0.09	0.10	ns
LVTTL33_12mA	LVTTL 12mA drive, VCCIO = 3.0V	0.02	0.03	0.03	ns
LVTTL33_16mA	LVTTL 16mA drive, VCCIO = 3.0V	0.12	0.13	0.13	ns
LVTTL33_20mA	LVTTL 20mA drive, VCCIO = 3.0V	0.08	0.08	0.09	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, fast slew rate	0.21	0.23	0.25	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, fast slew rate	0.09	0.09	0.10	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, fast slew rate	0.02	0.03	0.03	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, fast slew rate	0.12	0.13	0.13	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, fast slew rate	0.08	0.08	0.09	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, fast slew rate	0.12	0.12	0.12	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, fast slew rate	0.05	0.05	0.05	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, fast slew rate	0.08	0.08	0.08	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, fast slew rate	0.04	0.04	0.04	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, fast slew rate	0.08	0.09	0.09	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, fast slew rate	0.02	0.01	0.01	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, fast slew rate	-0.03	-0.03	-0.03	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, fast slew rate	0.03	0.03	0.03	ns

DLL Timing

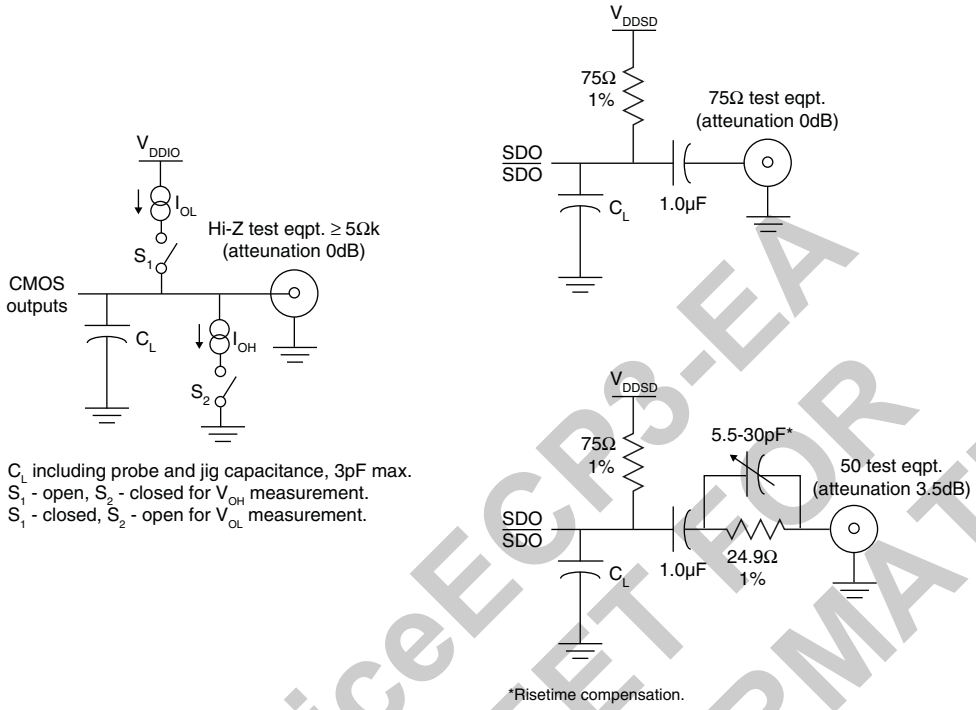
Over Recommended Operating Conditions

Parameter	Description	Condition	Min.	Typ.	Max.	Units
f_{REF}	Input reference clock frequency (on-chip or off-chip)		133	—	500	MHz
f_{FB}	Feedback clock frequency (on-chip or off-chip)		133	—	500	MHz
f_{CLKOP}[1]	Output clock frequency, CLKOP		133	—	500	MHz
f_{CLKOS}[2]	Output clock frequency, CLKOS		33.3	—	500	MHz
t_{PJIT}	Output clock period jitter (clean input)			—	200	ps p-p
t_{DUTY}	Output clock duty cycle (at 50% levels, 50% duty cycle input clock, 50% duty cycle circuit turned off, time reference delay mode)	Edge Clock	40		60	%
		Primary Clock	30		70	%
$t_{DUTYTRD}$	Output clock duty cycle (at 50% levels, arbitrary duty cycle input clock, 50% duty cycle circuit enabled, time reference delay mode)	Primary Clock < 250MHz	45		55	%
		Primary Clock ≥ 250MHz	30		70	%
		Edge Clock	45		55	%
$t_{DUTYCIR}$	Output clock duty cycle (at 50% levels, arbitrary duty cycle input clock, 50% duty cycle circuit enabled, clock injection removal mode) with DLL cascading	Primary Clock < 250MHz	40		60	%
		Primary Clock ≥ 250MHz	30		70	%
		Edge Clock	45		55	%
t_{SKEW}[3]	Output clock to clock skew between two outputs with the same phase setting		—	—	100	ps
t_{PHASE}	Phase error measured at device pads between off-chip reference clock and feedback clocks		—	—	+/-400	ps
t_{PWH}	Input clock minimum pulse width high (at 80% level)		550	—	—	ps
t_{PWL}	Input clock minimum pulse width low (at 20% level)		550	—	—	ps
t_{INSTB}	Input clock period jitter		—	—	500	p-p
t_{LOCK}	DLL lock time		8	—	8200	cycles
t_{RSWD}	Digital reset minimum pulse width (at 80% level)		3	—	—	ns
t_{DEL}	Delay step size		27	45	70	ps
t_{RANGE1}	Max. delay setting for single delay block (64 taps)		1.9	3.1	4.4	ns
t_{RANGE4}	Max. delay setting for four chained delay blocks		7.6	12.4	17.6	ns

1. CLKOP runs at the same frequency as the input clock.
2. CLKOS minimum frequency is obtained with divide by 4.
3. This is intended to be a “path-matching” design guideline and is not a measurable specification.

Figure 3-15. Test Loads

Test Loads



C_L including probe and jig capacitance, 3pF max.
S_1 - open, S_2 - closed for V_{OH} measurement.
S_1 - closed, S_2 - open for V_{OL} measurement.

*Risetime compensation.

Timing Jitter Bandpass

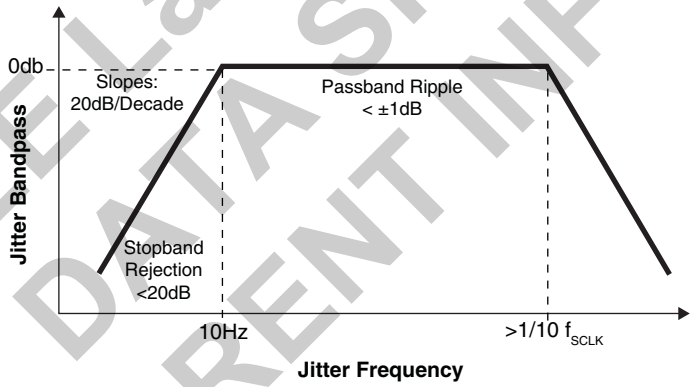
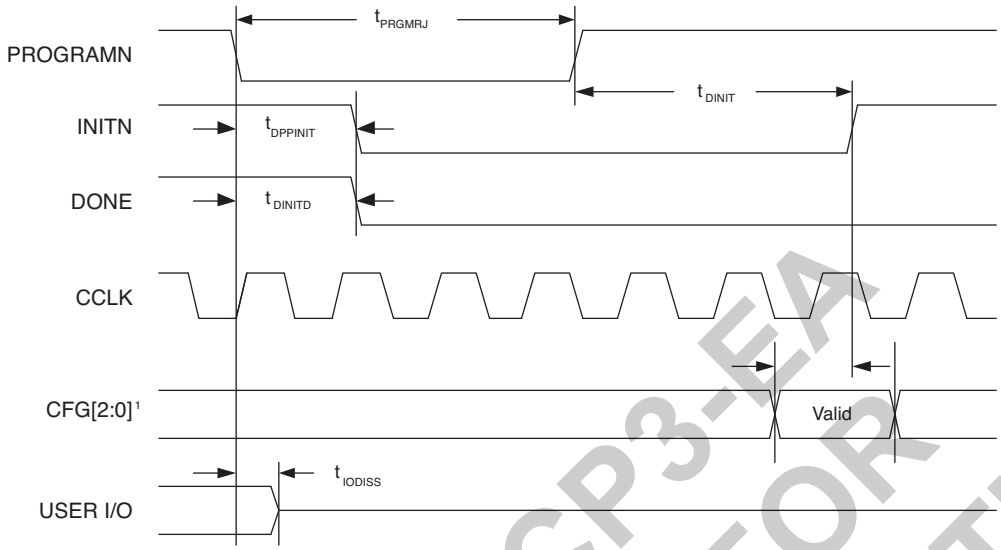
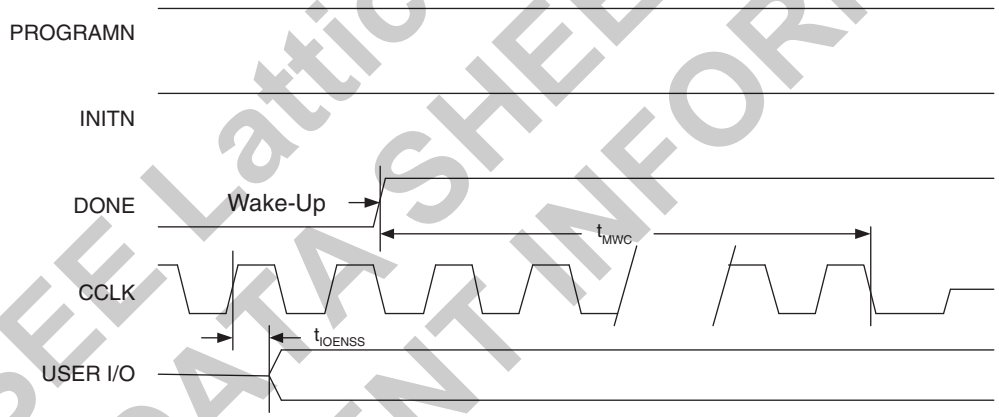


Figure 3-22. Configuration from PROGRAMN Timing



1. The CFG pins are normally static (hard wired)

Figure 3-23. Wake-Up Timing

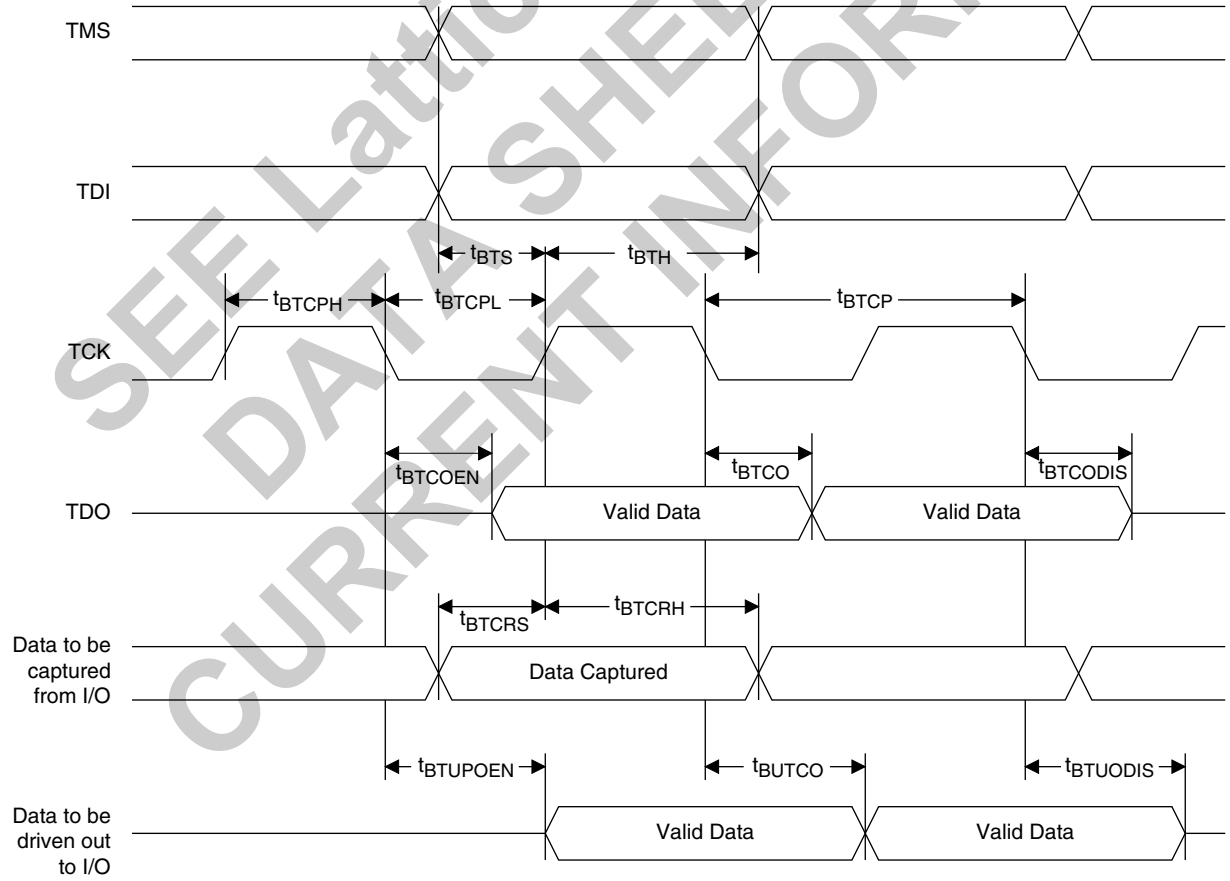


JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Figure 3-25. JTAG Port Timing Waveforms



Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-70E-6FN484C[1]	1.2V	-6	Lead-Free fpBGA	484	COM	67
LFE3-70E-7FN484C[1]	1.2V	-7	Lead-Free fpBGA	484	COM	67
LFE3-70E-8FN484C[1]	1.2V	-8	Lead-Free fpBGA	484	COM	67
LFE3-70E-6FN672C[1]	1.2V	-6	Lead-Free fpBGA	672	COM	67
LFE3-70E-7FN672C[1]	1.2V	-7	Lead-Free fpBGA	672	COM	67
LFE3-70E-8FN672C[1]	1.2V	-8	Lead-Free fpBGA	672	COM	67
LFE3-70E-6FN1156C[1]	1.2V	-6	Lead-Free fpBGA	1156	COM	67
LFE3-70E-7FN1156C[1]	1.2V	-7	Lead-Free fpBGA	1156	COM	67
LFE3-70E-8FN1156C[1]	1.2V	-8	Lead-Free fpBGA	1156	COM	67

1.This device has associated errata. View www.latticesemi.com/documents/ds1021.zip for a description of the errata.

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-95EA-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	92
LFE3-95EA-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	92
LFE3-95EA-8FN484C	1.2V	-8	Lead-Free fpBGA	484	COM	92
LFE3-95EA-6FN672C	1.2V	-6	Lead-Free fpBGA	672	COM	92
LFE3-95EA-7FN672C	1.2V	-7	Lead-Free fpBGA	672	COM	92
LFE3-95EA-8FN672C	1.2V	-8	Lead-Free fpBGA	672	COM	92
LFE3-95EA-6FN1156C	1.2V	-6	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-7FN1156C	1.2V	-7	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-8FN1156C	1.2V	-8	Lead-Free fpBGA	1156	COM	92

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-95E-6FN484C[1]	1.2V	-6	Lead-Free fpBGA	484	COM	92
LFE3-95E-7FN484C[1]	1.2V	-7	Lead-Free fpBGA	484	COM	92
LFE3-95E-8FN484C[1]	1.2V	-8	Lead-Free fpBGA	484	COM	92
LFE3-95E-6FN672C[1]	1.2V	-6	Lead-Free fpBGA	672	COM	92
LFE3-95E-7FN672C[1]	1.2V	-7	Lead-Free fpBGA	672	COM	92
LFE3-95E-8FN672C[1]	1.2V	-8	Lead-Free fpBGA	672	COM	92
LFE3-95E-6FN1156C[1]	1.2V	-6	Lead-Free fpBGA	1156	COM	92
LFE3-95E-7FN1156C[1]	1.2V	-7	Lead-Free fpBGA	1156	COM	92
LFE3-95E-8FN1156C[1]	1.2V	-8	Lead-Free fpBGA	1156	COM	92

1.This device has associated errata. View www.latticesemi.com/documents/ds1021.zip for a description of the errata.

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672C	1.2V	-6	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7FN672C	1.2V	-7	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8FN672C	1.2V	-8	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6FN1156C	1.2V	-6	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7FN1156C	1.2V	-7	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8FN1156C	1.2V	-8	Lead-Free fpBGA	1156	COM	149