# Lattice Semiconductor Corporation - LFE3-70E-8FN484I Datasheet


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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 8375 |
| Number of Logic Elements/Cells | 67000 |
| Total RAM Bits | 4526080 |
| Number of I/O | 295 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 484-BBGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-70e-8fn484i |

*Table 2-5. DLL Signals*

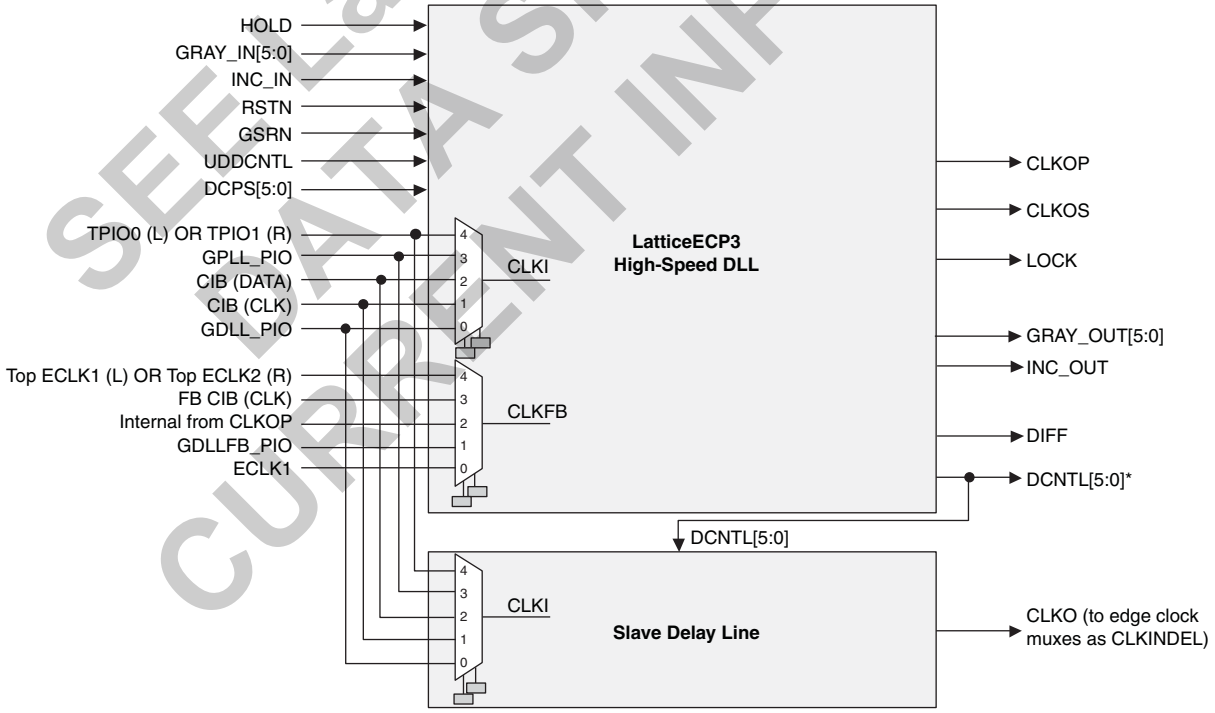
| Signal | I/O | Description |
|---|---|---|
| CLKI | I | Clock input from external pin or routing |
| CLKFB | I | DLL feed input from DLL output, clock net, routing or external pin |
| RSTN | I | Active low synchronous reset |
| ALUHOLD | I | Active high freezes the ALU |
| UDDCNTL | I | Synchronous enable signal (hold high for two cycles) from routing |
| CLKOP | O | The primary clock output |
| CLKOS | O | The secondary clock output with fine delay shift and/or division by 2 or by 4 |
| LOCK | O | Active high phase lock indicator |
| INCI | I | Incremental indicator from another DLL via CIB. |
| GRAYI[5:0] | I | Gray-coded digital control bus from another DLL in time reference mode. |
| DIFF | O | Difference indicator when DCNTL is difference than the internal setting and update is needed. |
| INCO | O | Incremental indicator to other DLLs via CIB. |
| GRAYO[5:0] | O | Gray-coded digital control bus to other DLLs via CIB |

LatticeECP3 devices have two general DLLs and four Slave Delay lines, two per DLL. The DLLs are in the lowest EBR row and located adjacent to the EBR. Each DLL replaces one EBR block. One Slave Delay line is placed adjacent to the DLL and the duplicate Slave Delay line (in Figure 2-6) for the DLL is placed in the I/O ring between Banks 6 and 7 and Banks 2 and 3.

The outputs from the DLL and Slave Delay lines are fed to the clock distribution network.

For more information, please see TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide.

*Figure 2-6. Top-Level Block Diagram, High-Speed DLL and Slave Delay Line*




* This signal is not user accessible. It can only be used to feed the slave delay line.

## PLL/DLL Cascading

LatticeECP3 devices have been designed to allow certain combinations of PLL and DLL cascading. The allowable combinations are:

- PLL to PLL supported
- PLL to DLL supported

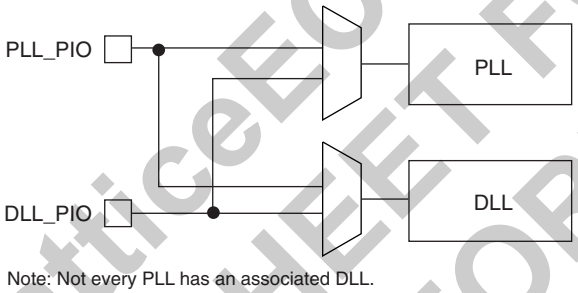
The DLLs in the LatticeECP3 are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLLs and PLLs.

For further information about the DLL, please see the list of technical documentation at the end of this data sheet.

## PLL/DLL PIO Input Pin Connections

All LatticeECP3 devices contains two DLLs and up to ten PLLs, arranged in quadrants. If a PLL and a DLL are next to each other, they share input pins as shown in the Figure 2-7.

***Figure 2-7. Sharing of PIO Pins by PLLs and DLLs in LatticeECP3 Devices***




Note: Not every PLL has an associated DLL.

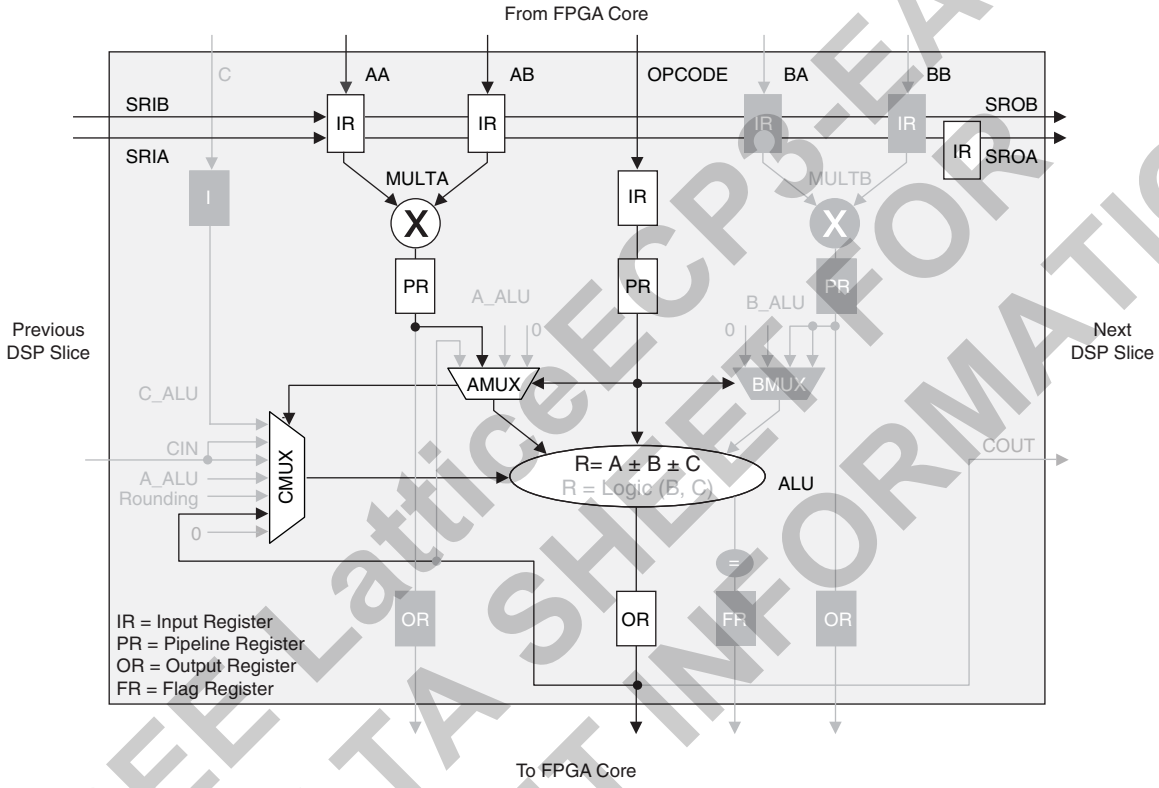
# Clock Dividers

LatticeECP3 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PLL/DLL outputs, the Slave Delay lines, routing or from an external clock input. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and asynchronously forces all outputs to low. The RELEASE signal releases outputs synchronously to the input clock. For further information on clock dividers, please see TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide. Figure 2-8 shows the clock divider connections.

## MAC DSP Element

In this case, the two operands, AA and AB, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The ALU is configured as the accumulator in the sysDSP slice in the LatticeECP3 family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-27 shows the MAC sysDSP element.

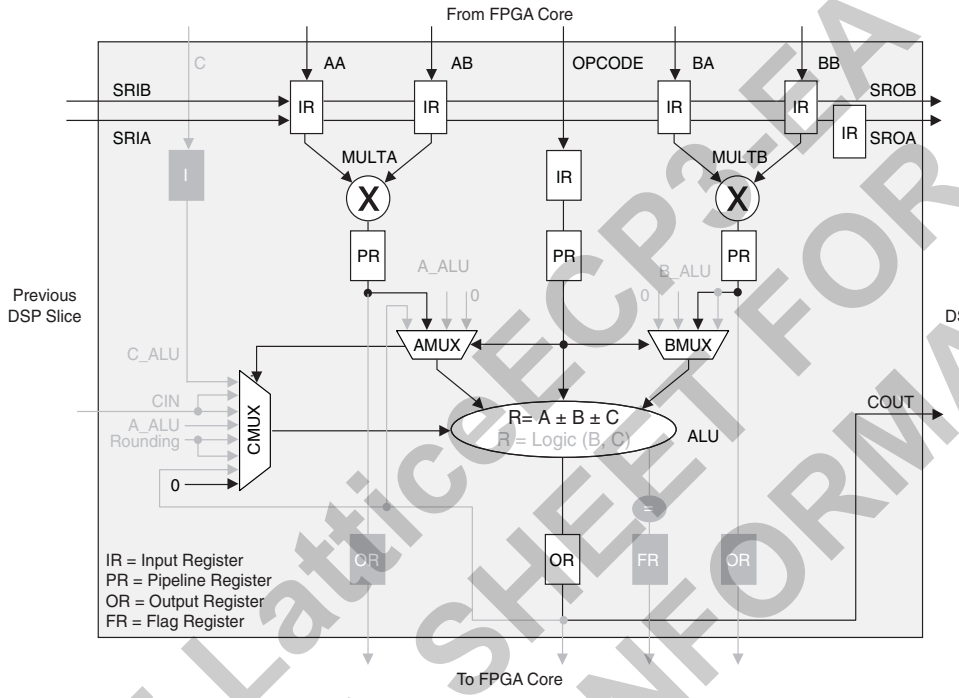
***Figure 2-27. MAC DSP Element***



## MULTADDSUBSUM DSP Element

In this case, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB of Slice 0. Additionally, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB of Slice 1. The results of both addition/subtractions are added by the second ALU following the slice cascade path. The user can enable the input, output and pipeline registers. Figure 2-30 and Figure 2-31 show the MULTADDSUBSUM sysDSP element.

***Figure 2-30. MULTADDSUBSUM Slice 0***



## ALU Flags

The sysDSP slice provides a number of flags from the ALU including:

- Equal to zero (EQZ)
- Equal to zero with mask (EQZM)
- Equal to one with mask (EQOM)
- Equal to pattern with mask (EQPAT)
- Equal to bit inverted pattern with mask (EQPATB)
- Accumulator Overflow (OVER)
- Accumulator Underflow (UNDER)
- Either over or under flow supporting LatticeECP2 legacy designs (OVERUNDER)

## Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every sysDSP slice. From four clock sources (CLK0, CLK1, CLK2, and CLK3) one clock is selected for each input register, pipeline register and output register. Similarly Clock Enable (CE) and Reset (RST) are selected at each input register, pipeline register and output register.

## Resources Available in the LatticeECP3 Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP3 family. Table 2-10 shows the maximum available EBR RAM Blocks in each LatticeECP3 device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

***Table 2-9. Maximum Number of DSP Slices in the LatticeECP3 Family***

| Device | DSP Slices | 9x9 Multiplier | 18x18 Multiplier | 36x36 Multiplier |
|---|---|---|---|---|
| ECP3-17 | 12 | 48 | 24 | 6 |
| ECP3-35 | 32 | 128 | 64 | 16 |
| ECP3-70 | 64 | 256 | 128 | 32 |
| ECP3-95 | 64 | 256 | 128 | 32 |
| ECP3-150 | 160 | 640 | 320 | 80 |

***Table 2-10. Embedded SRAM in the LatticeECP3 Family***

| Device | EBR SRAM Block | Total EBR SRAM (Kbits) |
|---|---|---|
| ECP3-17 | 38 | 700 |
| ECP3-35 | 72 | 1327 |
| ECP3-70 | 240 | 4420 |
| ECP3-95 | 240 | 4420 |
| ECP3-150 | 372 | 6850 |

The ispLEVER design tools from Lattice support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With ispLEVER, the user can define the mode for each quad in a design.

Popular standards such as 10Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), a single quad (Four SERDES channels and PCS) and some additional logic from the core.

The LatticeECP3 family also supports a wide range of primary and secondary protocols. Within the same quad, the LatticeECP3 family can support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. Table 2-15 lists the allowable combination of primary and secondary protocol combinations.

## Flexible Quad SERDES Architecture

The LatticeECP3 family SERDES architecture is a quad-based architecture. For most SERDES settings and standards, the whole quad (consisting of four SERDES) is treated as a unit. This helps in silicon area savings, better utilization and overall lower cost.

However, for some specific standards, the LatticeECP3 quad architecture provides flexibility; more than one standard can be supported within the same quad.

Table 2-15 shows the standards can be mixed and matched within the same quad. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same quad. In Table 2-15, the Primary Protocol column refers to the standard that determines the reference clock and PLL settings. The Secondary Protocol column shows the other standard that can be supported within the same quad.

Furthermore, Table 2-15 also implies that more than two standards in the same quad can be supported, as long as they conform to the data rate and reference clock requirements. For example, a quad may contain PCI Express 1.1, SGMII, Serial RapidIO Type I and Serial RapidIO Type II, all in the same quad.

***Table 2-15. LatticeECP3 Primary and Secondary Protocol Support***

| Primary Protocol | Secondary Protocol |
|---|---|
| PCI Express 1.1 | SGMII |
| PCI Express 1.1 | Gigabit Ethernet |
| PCI Express 1.1 | Serial RapidIO Type I |
| PCI Express 1.1 | Serial RapidIO Type II |
| Serial RapidIO Type I | SGMII |
| Serial RapidIO Type I | Gigabit Ethernet |
| Serial RapidIO Type II | SGMII |
| Serial RapidIO Type II | Gigabit Ethernet |
| Serial RapidIO Type II | Serial RapidIO Type I |
| CPRI-3 | CPRI-2 and CPRI-1 |
| 3G-SDI | HD-SDI and SD-SDI |

For further information on SERDES, please see TN1176, LatticeECP3 SERDES/PCS Usage Guide.

## IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeECP3 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test

can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode (normal operation) the device can be programmed to generate an error signal.

For further information on SED support, please see TN1184, LatticeECP3 Soft Error Detection (SED) Usage Guide.

### External Resistor

LatticeECP3 devices require a single external, 10K ohm ±1% value between the XRES pin and ground. Device configuration will not be completed if this resistor is missing. There is no boundary scan register on the external resistor pad.

### On-Chip Oscillator

Every LatticeECP3 device has an internal CMOS oscillator which is used to derive a Master Clock (MCLK) for configuration. The oscillator and the MCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCLK is nominally 2.5MHz. Table 2-16 lists all the available MCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 3.1MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.5MHz.

This internal CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

***Table 2-16. Selectable Master Clock (MCLK) Frequencies During Configuration (Nominal)***

| MCLK (MHz) | MCLK (MHz) | MCLK (MHz) |
|---|---|---|
| 2.5[1] | 10 | 41 |
| 3.1 | 13 | 45 |
| 4.3 | 15 | 51 |
| 5.4 | 20 | 55 |
| 6.9 | 26 | 60 |
| 8.1 | 30 | 130 |
| 9.2 | 34 | — |

1. Software default MCLK frequency. Hardware default is 3.1MHz.



## Density Shifting

The LatticeECP3 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same packge.

## LVDS25E

The top and bottom sides of LatticeECP3 devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.

***Figure 3-1. LVDS25E Output Termination Example***

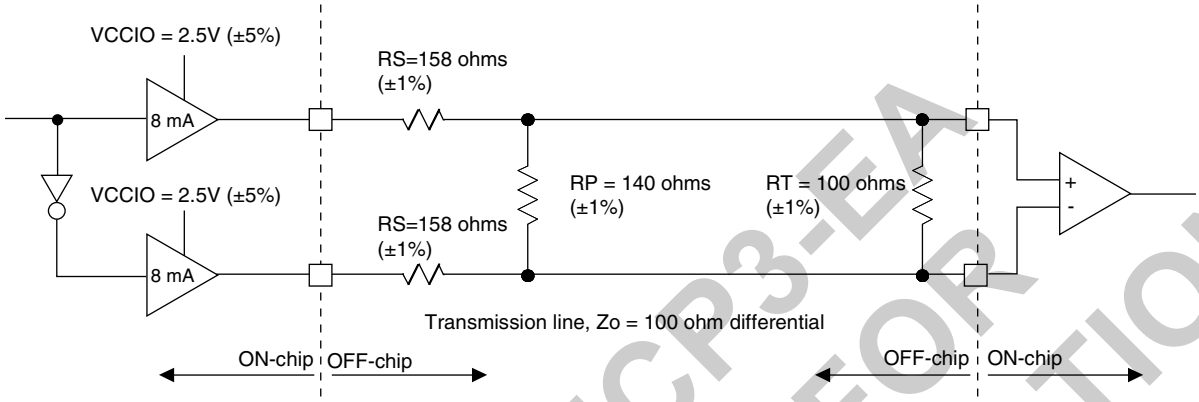



***Table 3-1. LVDS25E DC Conditions***

| Parameter | Description | Typical | Units |
|---|---|---|---|
| $V_{CCIO}$ | Output Driver Supply (+/-5%) | 2.50 | V |
| $Z_{OUT}$ | Driver Impedance | 20 | Ω |
| $R_S$ | Driver Series Resistor (+/-1%) | 158 | Ω |
| $R_P$ | Driver Parallel Resistor (+/-1%) | 140 | Ω |
| $R_T$ | Receiver Termination (+/-1%) | 100 | Ω |
| $V_{OH}$ | Output High Voltage | 1.43 | V |
| $V_{OL}$ | Output Low Voltage | 1.07 | V |
| $V_{OD}$ | Output Differential Voltage | 0.35 | V |
| $V_{CM}$ | Output Common Mode Voltage | 1.25 | V |
| $Z_{BACK}$ | Back Impedance | 100.5 | Ω |
| $I_{DC}$ | DC Output Current | 6.03 | mA |

## LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3V $V_{CCIO}$. The default drive current for LVCMOS33D output is 12mA with the option to change the device strength to 4mA, 8mA, 16mA or 20mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.

### Register-to-Register Performance[1, 2]

| Function | -8 Timing | Units |
|---|---|---|
| 18x18 Multiply/Accumulate (Input & Output Registers) | 200 | MHz |
| 18x18 Multiply-Add/Sub (All Registers) | 400 | MHz |
| **DSP IP Functions** | | |
| 16-Tap Fully-Parallel FIR Filter | | MHz |
| 1024-pt, Radix 4, Decimation in Frequency FFT | | MHz |
| 8X8 Matrix Multiplication | | MHz |

1. These timing numbers were generated using ispLEVER tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the ispLEVER software.

## Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the ispLEVER design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The ispLEVER design tool can provide logic timing numbers at a particular temperature and voltage.

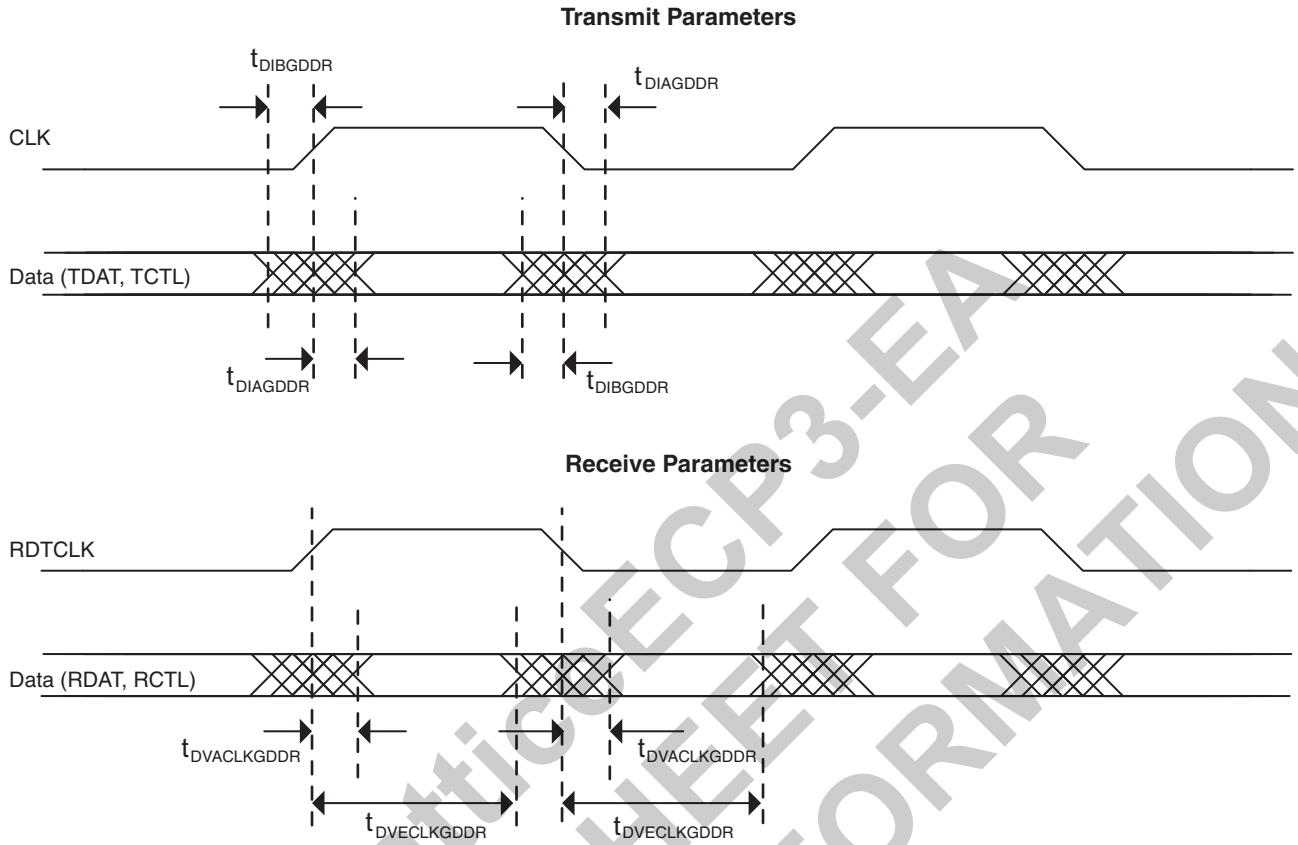
# LatticeECP3 External Switching Characteristics (Continued)[1, 2]

**Over Recommended Commercial Operating Conditions**

| Parameter | Description | Device | -8 | | -7 | | -6 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Generic DDRX2 Output with Clock and Data (> 10 Bits Wide) Aligned at Pin (GDDRX2_TX.ECLK.Aligned)** | | | | | | | | | |
| **Left and Right Sides** | | | | | | | | | |
| $t_{DIBGDDR}$ | Data Setup Before CLK | ECP3-150EA | — | | — | | — | | ps |
| $t_{DIAGDDR}$ | Data Hold After CLK | ECP3-150EA | — | | — | | — | | ps |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-150EA | — | | — | | — | | MHz |
| **Generic DDRX2 Outputs with Clock and Data Edges Aligned, Without PLL 90-degree shifted clock output[5] (GDDRX2_TX.Aligned)** | | | | | | | | | |
| $t_{DIBGDDR}$ | Data Invalid Before Clock | ECP3-70E/95E | — | 200 | — | 225 | — | 250 | ps |
| $t_{DIAGDDR}$ | Data Invalid After Clock | ECP3-70E/95E | — | 200 | — | 225 | — | 250 | ps |
| $f_{MAX\_GDDR}$ | DDR/DDRX2 Clock Frequency[8] | ECP3-70E/95E | — | 500 | — | 420 | — | 375 | MHz |
| **Generic DDRX2 Output with Clock and Data (> 10 Bits Wide) Centered at Pin Using DQSDLL (GDDRX2_TX.DQS-DLL.Centered)** | | | | | | | | | |
| **Left and Right Sides** | | | | | | | | | |
| $t_{DVBGDDR}$ | Data Valid Before CLK | ECP3-150EA | | — | | — | | — | ns |
| $t_{DVAGDDR}$ | Data Valid After CLK | ECP3-150EA | | — | | — | | — | ns |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-150EA | — | | — | | — | | ns |
| **Generic DDRX2 Output with Clock and Data (> 10 Bits Wide) Centered at Pin Using PLL (GDDRX2_TX.PLL.Centered)** | | | | | | | | | |
| **Left and Right Sides** | | | | | | | | | |
| $t_{DVBGDDR}$ | Data Valid Before CLK | ECP3-150EA | | — | | — | | — | ns |
| $t_{DVAGDDR}$ | Data Valid After CLK | ECP3-150EA | | — | | — | | — | ns |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-150EA | — | | — | | — | | ns |
| **Generic DDRX2 Outputs with Clock Edge in the Center of Data Window, with PLL 90-degree Shifted Clock Output[6] (GDDRX2_TX.PLL.Centered)** | | | | | | | | | |
| $t_{DVBGDDR}$ | Data Valid Before CLK | ECP3-70E/95E | 300 | — | 370 | — | 417 | — | ps |
| $t_{DVAGDDR}$ | Data Valid After CLK | ECP3-70E/95E | 300 | — | 370 | — | 417 | — | ps |
| $f_{MAX\_GDDR}$ | DDR/DDRX2 Clock Frequency[8] | ECP3-70E/95E | — | 500 | — | 420 | — | 375 | MHz |

| Parameter | Description | Device | -8 | | -7 | | -6 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Memory Interface** | | | | | | | | | |
| **DDR/DDR2 SDRAM I/O Pin Parameters (Input Data are Strobe Edge Aligned, Output Strobe Edge is Data Centered)[4]** | | | | | | | | | |
| $t_{DVADQ}$ | Data Valid After DQS (DDR Read) | ECP3-150EA | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVEDQ}$ | Data Hold After DQS (DDR Read) | ECP3-150EA | 0.64 | — | 0.64 | — | 0.64 | — | UI |
| $t_{DQVBS}$ | Data Valid Before DQS | ECP3-150EA | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Data Valid After DQS | ECP3-150EA | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{MAX\_DDR}$ | DDR Clock Frequency | ECP3-150EA | 95 | 200 | 95 | 200 | 95 | 166 | MHz |
| $f_{MAX\_DDR2}$ | DDR2 clock frequency | ECP3-150EA | 133 | 266 | 133 | 200 | 133 | 166 | MHz |
| $t_{DVADQ}$ | Data Valid After DQS (DDR Read) | ECP3-70E/95E | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVEDQ}$ | Data Hold After DQS (DDR Read) | ECP3-70E/95E | 0.64 | — | 0.64 | — | 0.64 | — | UI |
| $t_{DQVBS}$ | Data Valid Before DQS | ECP3-70E/95E | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Data Valid After DQS | ECP3-70E/95E | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{MAX\_DDR}$ | DDR Clock Frequency | ECP3-70E/95E | 95 | 200 | 95 | 200 | 95 | 133 | MHz |

*Figure 3-6. Generic DDR/DDR2 (With Clock and Data Edges Aligned)*

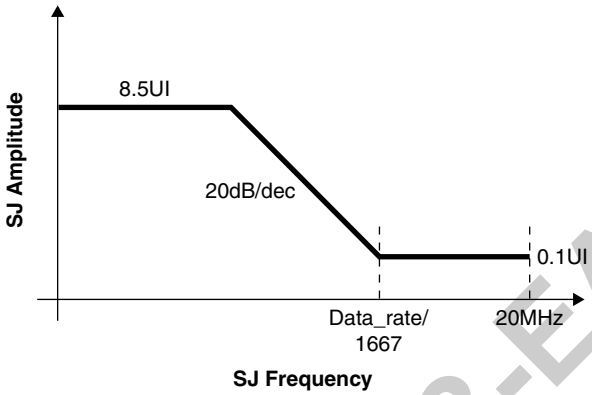


## LatticeECP3 Family Timing Adders[1, 2, 3, 4, 5]

**Over Recommended Commercial Operating Conditions**

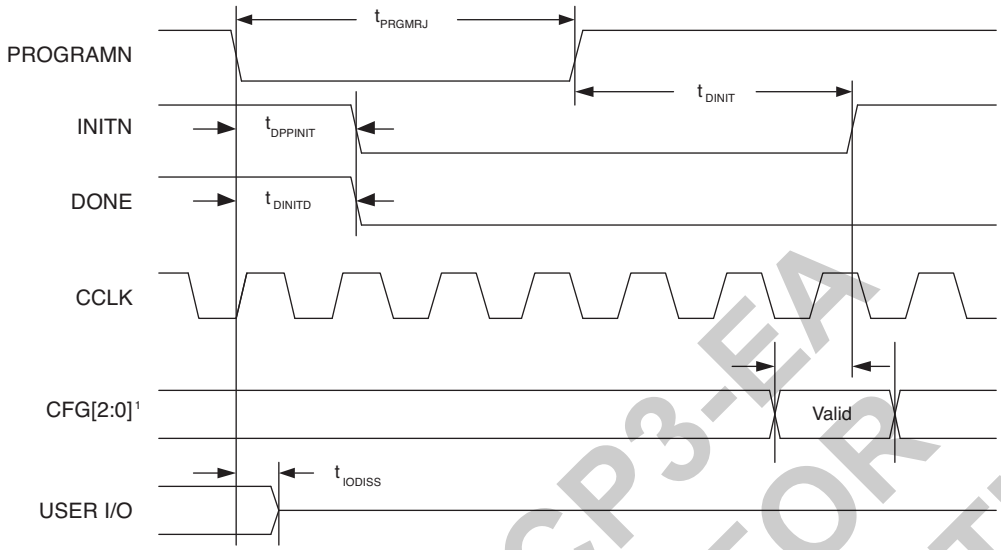
| Buffer Type | Description | -8 | -7 | -6 | Units |
|---|---|---|---|---|---|
| **Input Adjusters** | | | | | |
| LVDS25E | LVDS, Emulated, VCCIO = 2.5V | 0.03 | -0.01 | -0.03 | ns |
| LVDS25 | LVDS, VCCIO = 2.5V | 0.03 | 0.00 | -0.04 | ns |
| BLVDS25 | BLVDS, Emulated, VCCIO = 2.5V | 0.03 | 0.00 | -0.04 | ns |
| MLVDS25 | MLVDS, Emulated, VCCIO = 2.5V | 0.03 | 0.00 | -0.04 | ns |
| RSDS25 | RSDS, VCCIO = 2.5V | 0.03 | 0.00 | -0.03 | ns |
| PPLVDS | Point-to-Point LVDS | 0.03 | -0.01 | -0.03 | ns |
| TRLVDS | Transition-Reduced LVDS | 0.03 | 0.00 | -0.04 | ns |
| Mini MLVDS | Mini LVDS | 0.03 | -0.01 | -0.03 | ns |
| LVPECL33 | LVPECL, Emulated, VCCIO = 3.0V | 0.17 | 0.07 | -0.04 | ns |
| HSTL18_I | HSTL_18 class I, VCCIO = 1.8V | 0.20 | 0.17 | 0.13 | ns |
| HSTL18_II | HSTL_18 class II, VCCIO = 1.8V | 0.20 | 0.17 | 0.13 | ns |
| HSTL18D_I | Differential HSTL 18 class I | 0.20 | 0.17 | 0.13 | ns |
| HSTL18D_II | Differential HSTL 18 class II | 0.20 | 0.17 | 0.13 | ns |
| HSTL15_I | HSTL_15 class I, VCCIO = 1.5V | 0.10 | 0.12 | 0.13 | ns |
| HSTL15D_I | Differential HSTL 15 class I | 0.10 | 0.12 | 0.13 | ns |
| SSTL33_I | SSTL_3 class I, VCCIO = 3.0V | 0.17 | 0.23 | 0.28 | ns |
| SSTL33_II | SSTL_3 class II, VCCIO = 3.0V | 0.17 | 0.23 | 0.28 | ns |
| SSTL33D_I | Differential SSTL_3 class I | 0.17 | 0.23 | 0.28 | ns |
| SSTL33D_II | Differential SSTL_3 class II | 0.17 | 0.23 | 0.28 | ns |
| SSTL25_I | SSTL_2 class I, VCCIO = 2.5V | 0.12 | 0.14 | 0.16 | ns |
| SSTL25_II | SSTL_2 class II, VCCIO = 2.5V | 0.12 | 0.14 | 0.16 | ns |
| SSTL25D_I | Differential SSTL_2 class I | 0.12 | 0.14 | 0.16 | ns |
| SSTL25D_II | Differential SSTL_2 class II | 0.12 | 0.14 | 0.16 | ns |
| SSTL18_I | SSTL_18 class I, VCCIO = 1.8V | 0.08 | 0.06 | 0.04 | ns |
| SSTL18_II | SSTL_18 class II, VCCIO = 1.8V | 0.08 | 0.06 | 0.04 | ns |
| SSTL18D_I | Differential SSTL_18 class I | 0.08 | 0.06 | 0.04 | ns |
| SSTL18D_II | Differential SSTL_18 class II | 0.08 | 0.06 | 0.04 | ns |
| SSTL15 | SSTL_15, VCCIO = 1.5V | 0.087 | 0.059 | 0.032 | ns |
| SSTL15D | Differential SSTL_15 | 0.087 | 0.025 | -0.036 | ns |
| LVTTL33 | LVTTL, VCCIO = 3.0V | 0.05 | 0.05 | 0.05 | ns |
| LVCMOS33 | LVCMOS, VCCIO = 3.0V | 0.05 | 0.05 | 0.05 | ns |
| LVCMOS25 | LVCMOS, VCCIO = 2.5V | 0.00 | 0.00 | 0.00 | ns |
| LVCMOS18 | LVCMOS, VCCIO = 1.8V | 0.06 | 0.08 | 0.11 | ns |
| LVCMOS15 | LVCMOS, VCCIO = 1.5V | 0.17 | 0.21 | 0.25 | ns |
| LVCMOS12 | LVCMOS, VCCIO = 1.2V | 0.01 | 0.05 | 0.08 | ns |
| PCI33 | PCI, VCCIO = 3.0V | 0.05 | 0.05 | 0.05 | ns |
| **Output Adjusters** | | | | | |
| LVDS25E | LVDS, Emulated, VCCIO = 2.5V | 0.15 | 0.15 | 0.16 | ns |
| LVDS25 | LVDS, VCCIO = 2.5V | 0.02 | 0.08 | 0.13 | ns |
| BLVDS25 | BLVDS, Emulated, VCCIO = 2.5V | 0.00 | -0.02 | -0.04 | ns |
| MLVDS25 | MLVDS, Emulated, VCCIO = 2.5V | 0.00 | -0.01 | -0.03 | ns |

*Figure 3-14. XAUI Sinusoidal Jitter Tolerance Mask*




Note: The sinusoidal jitter tolerance is measured with at least 0.37UIpp of Deterministic jitter (Dj) and the sum of Dj and Rj (random jitter) is at least 0.55UIpp. Therefore, the sum of Dj, Rj and Sj (sinusoidal jitter) is at least 0.65UIpp (Dj = 0.37, Rj = 0.18, Sj = 0.1).

***Figure 3-22. Configuration from PROGRAMN Timing***




1. The CFG pins are normally static (hard wired)

***Figure 3-23. Wake-Up Timing***

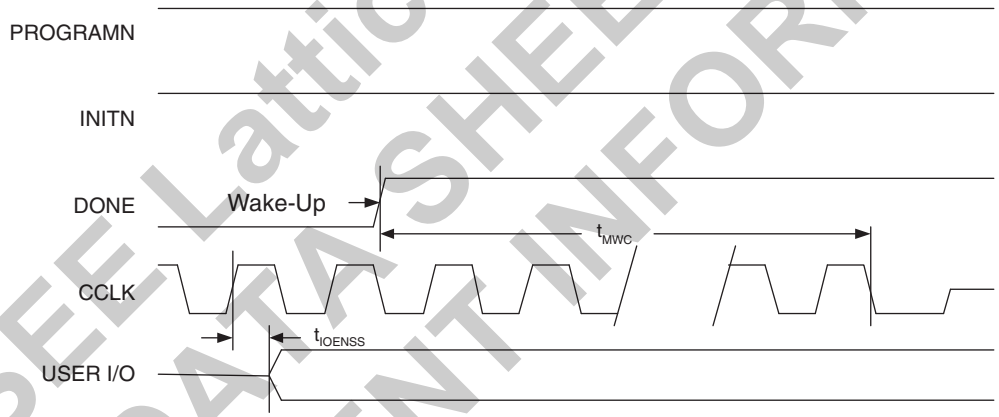
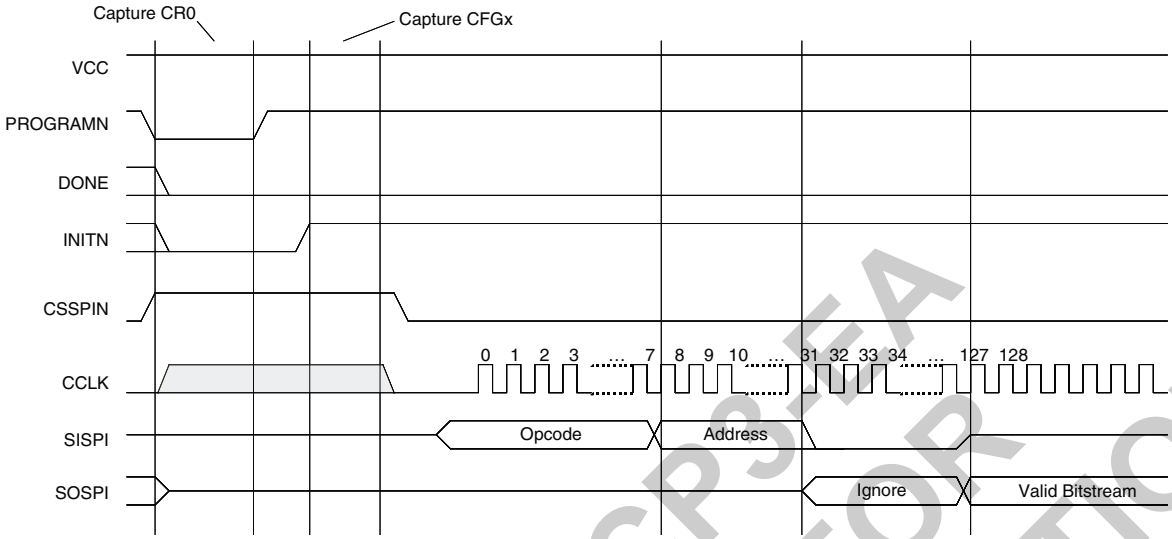


***Figure 3-24. Master SPI Configuration Waveforms***



## Pin Information Summary (Cont.)

| Pin Information Summary | | ECP3-95E/EA | | | ECP3-150EA | |
|---|---|---|---|---|---|---|
| Pin Type | | 484 fpBGA | 672 fpBGA | 1156 fpBGA | 672 fpBGA | 1156 fpBGA |
| General Purpose Inputs/Outputs per bank | Bank 0 | 42 | 60 | 86 | 60 | 94 |
| | Bank 1 | 36 | 48 | 78 | 48 | 86 |
| | Bank 2 | 24 | 34 | 36 | 34 | 58 |
| | Bank 3 | 54 | 59 | 86 | 59 | 104 |
| | Bank 6 | 63 | 67 | 86 | 67 | 104 |
| | Bank 7 | 36 | 48 | 54 | 48 | 76 |
| | Bank 8 | 24 | 24 | 24 | 24 | 24 |
| General Purpose Inputs per Bank | Bank 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 1 | 0 | 0 | 0 | 0 | 0 |
| | Bank 2 | 4 | 8 | 8 | 8 | 8 |
| | Bank 3 | 4 | 12 | 12 | 12 | 12 |
| | Bank 6 | 4 | 12 | 12 | 12 | 12 |
| | Bank 7 | 4 | 8 | 8 | 8 | 8 |
| | Bank 8 | 0 | 0 | 0 | 0 | 0 |
| General Purpose Outputs per Bank | Bank 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 1 | 0 | 0 | 0 | 0 | 0 |
| | Bank 2 | 0 | 0 | 0 | 0 | 0 |
| | Bank 3 | 0 | 0 | 0 | 0 | 0 |
| | Bank 6 | 0 | 0 | 0 | 0 | 0 |
| | Bank 7 | 0 | 0 | 0 | 0 | 0 |
| | Bank 8 | 0 | 0 | 0 | 0 | 0 |
| Total Single-Ended User I/O | | 295 | 380 | 490 | 380 | 586 |
| VCC | | 16 | 32 | 32 | 32 | 32 |
| VCCAUX | | 8 | 12 | 16 | 12 | 16 |
| VTT | | 4 | 4 | 8 | 4 | 8 |
| VCCA | | 4 | 8 | 16 | 8 | 16 |
| VCCPLL | | 4 | 4 | 4 | 4 | 4 |
| VCCIO | Bank 0 | 2 | 4 | 4 | 4 | 4 |
| | Bank 1 | 2 | 4 | 4 | 4 | 4 |
| | Bank 2 | 2 | 4 | 4 | 4 | 4 |
| | Bank 3 | 2 | 4 | 4 | 4 | 4 |
| | Bank 6 | 2 | 4 | 4 | 4 | 4 |
| | Bank 7 | 2 | 4 | 4 | 4 | 4 |
| | Bank 8 | 2 | 2 | 2 | 2 | 2 |
| VCCJ | | 1 | 1 | 1 | 1 | 1 |
| TAP | | 4 | 4 | 4 | 4 | 4 |
| GND, GNDIO | | 98 | 139 | 233 | 139 | 233 |
| NC | | 0 | 0 | 238 | 0 | 116 |
| Reserved[1] | | 2 | 2 | 2 | 2 | 2 |
| SERDES | | 26 | 52 | 78 | 52 | 104 |
| Miscellaneous Pins | | 8 | 8 | 8 | 8 | 8 |
| Total Bonded Pins | | 484 | 672 | 1156 | 672 | 1156 |

# LatticeECP3 Family Data Sheet Ordering Information

March 2010 Preliminary Data Sheet DS1021

## LatticeECP3 Part Number Description

LFE3 – XXX XX – X XXXXXX X

**Device Family**
ECP3 (LatticeECP3 FPGA + SERDES)

**Logic Capacity**
17 = 17K LUTs
35 = 33K LUTs
70 = 67K LUTs
95 = 92K LUTs
150 = 149K LUTs

**Supply Voltage**
E or EA = 1.2V

**Speed**
6 = Slowest
7
8 = Fastest

**Grade**
C = Commercial
I = Industrial

**Package**
FTN256 = 256-ball Lead-Free ftBGA
FN484 = 484-ball Lead-Free fpBGA
FN672 = 672-ball Lead-Free fpBGA
FN1156 = 1156-ball Lead-Free fpBGA

## Ordering Information

LatticeECP3 devices have top-side markings, for commercial and industrial grades, as shown below:

**Commercial**

Lattice ECP3
LFE3-95E
7FN672C
Datecode

**Industrial**

Lattice ECP3
LFE3-95E
7FN672I
Datecode

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|
| LFE3-70E-6FN484I[1] | 1.2V | -6 | Lead-Free fpBGA | 484 | IND | 67 |
| LFE3-70E-7FN484I[1] | 1.2V | -7 | Lead-Free fpBGA | 484 | IND | 67 |
| LFE3-70E-8FN484I[1] | 1.2V | -8 | Lead-Free fpBGA | 484 | IND | 67 |
| LFE3-70E-6FN672I[1] | 1.2V | -6 | Lead-Free fpBGA | 672 | IND | 67 |
| LFE3-70E-7FN672I[1] | 1.2V | -7 | Lead-Free fpBGA | 672 | IND | 67 |
| LFE3-70E-8FN672I[1] | 1.2V | -8 | Lead-Free fpBGA | 672 | IND | 67 |
| LFE3-70E-6FN1156I[1] | 1.2V | -6 | Lead-Free fpBGA | 1156 | IND | 67 |
| LFE3-70E-7FN1156I[1] | 1.2V | -7 | Lead-Free fpBGA | 1156 | IND | 67 |
| LFE3-70E-8FN1156I[1] | 1.2V | -8 | Lead-Free fpBGA | 1156 | IND | 67 |

1.This device has associated errata. View www.latticesemi.com/documents/ds1021.zip for a description of the errata.

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|
| LFE3-95EA-6FN484I | 1.2V | -6 | Lead-Free fpBGA | 484 | IND | 92 |
| LFE3-95EA-7FN484I | 1.2V | -7 | Lead-Free fpBGA | 484 | IND | 92 |
| LFE3-95EA-8FN484I | 1.2V | -8 | Lead-Free fpBGA | 484 | IND | 92 |
| LFE3-95EA-6FN672I | 1.2V | -6 | Lead-Free fpBGA | 672 | IND | 92 |
| LFE3-95EA-7FN672I | 1.2V | -7 | Lead-Free fpBGA | 672 | IND | 92 |
| LFE3-95EA-8FN672I | 1.2V | -8 | Lead-Free fpBGA | 672 | IND | 92 |
| LFE3-95EA-6FN1156I | 1.2V | -6 | Lead-Free fpBGA | 1156 | IND | 92 |
| LFE3-95EA-7FN1156I | 1.2V | -7 | Lead-Free fpBGA | 1156 | IND | 92 |
| LFE3-95EA-8FN1156I | 1.2V | -8 | Lead-Free fpBGA | 1156 | IND | 92 |

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|
| LFE3-95E-6FN484I[1] | 1.2V | -6 | Lead-Free fpBGA | 484 | IND | 92 |
| LFE3-95E-7FN484I[1] | 1.2V | -7 | Lead-Free fpBGA | 484 | IND | 92 |
| LFE3-95E-8FN484I[1] | 1.2V | -8 | Lead-Free fpBGA | 484 | IND | 92 |
| LFE3-95E-6FN672I[1] | 1.2V | -6 | Lead-Free fpBGA | 672 | IND | 92 |
| LFE3-95E-7FN672I[1] | 1.2V | -7 | Lead-Free fpBGA | 672 | IND | 92 |
| LFE3-95E-8FN672I[1] | 1.2V | -8 | Lead-Free fpBGA | 672 | IND | 92 |
| LFE3-95E-6FN1156I[1] | 1.2V | -6 | Lead-Free fpBGA | 1156 | IND | 92 |
| LFE3-95E-7FN1156I[1] | 1.2V | -7 | Lead-Free fpBGA | 1156 | IND | 92 |
| LFE3-95E-8FN1156I[1] | 1.2V | -8 | Lead-Free fpBGA | 1156 | IND | 92 |

1.This device has associated errata. View www.latticesemi.com/documents/ds1021.zip for a description of the errata.

# LatticeECP3 Family Data Sheet Supplemental Information



## For Further Information

A variety of technical notes for the LatticeECP3 family are available on the Lattice website at www.latticesemi.com.

- TN1169, LatticeECP3 sysCONFIG Usage Guide
- TN1176, LatticeECP3 SERDES/PCS Usage Guide
- TN1177, LatticeECP3 sysIO Usage Guide
- TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide
- TN1179, LatticeECP3 Memory Usage Guide
- TN1180, LatticeECP3 High-Speed I/O Interface
- TN1181, Power Consumption and Management for LatticeECP3 Devices
- TN1182, LatticeECP3 sysDSP Usage Guide
- TN1184, LatticeECP3 Soft Error Detection (SED) Usage Guide
- TN1189, LatticeECP3 Hardware Checklist

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com

# LatticeECP3 Family Data Sheet Revision History



| Date | Version | Section | Change Summary |
|---|---|---|---|
| February 2009 | 01.0 | — | Initial release. |
| May 2009 | 01.1 | All | Removed references to Parallel burst mode Flash. |
| | | Introduction | Features - Changed 250 Mbps to 230 Mbps in Embedded SERDES bulleted section and added a footnote to indicate 230 Mbps applies to 8b10b and 10b12b applications. |
| | | | Updated data for ECP3-17 in LatticeECP3 Family Selection Guide table. |
| | | | Changed embedded memory from 552 to 700 Kbits in LatticeECP3 Family Selection Guide table. |
| | | Architecture | Updated description for CLKFB in General Purpose PLL Diagram. |
| | | | Corrected Primary Clock Sources text section. |
| | | | Corrected Secondary Clock/Control Sources text section. |
| | | | Corrected Secondary Clock Regions table. |
| | | | Corrected note below Detailed sysDSP Slice Diagram. |
| | | | Corrected Clock, Clock Enable, and Reset Resources text section. |
| | | | Corrected ECP3-17 EBR number in Embedded SRAM in the LatticeECP3 Family table. |
| | | | Added On-Chip Termination Options for Input Modes table. |
| | | | Updated Available SERDES Quads per LatticeECP3 Devices table. |
| | | | Updated Simplified Channel Block Diagram for SERDES/PCS Block diagram. |
| | | | Updated Device Configuration text section. |
| | | | Corrected software default value of MCLK to be 2.5 MHz. |
| | | DC and Switching Characteristics | Updated VCCOB Min/Max data in Recommended Operating Conditions table. |
| | | | Corrected footnote 2 in sysIO Recommended Operating Conditions table. |
| | | | Added added footnote 7 for $t_{SKEW\_PRIB}$ to External Switching Characteristics table. |
| | | | Added 2-to-1 Gearing text section and table. |
| | | | Updated External Reference Clock Specification (refclkp/refclkn) table. |
| | | | LatticeECP3 sysCONFIG Port Timing Specifications - updated $t_{DINIT}$ information. |
| | | | Added sysCONFIG Port Timing waveform. |
| | | | Serial Input Data Specifications table, delete Typ data for $V_{RX\text{-}DIFF\text{-}S}$. |
| | | | Added footnote 4 to sysCLOCK PLL Timing table for $t_{PFD}$. |
| | | | Added SERDES/PCS Block Latency Breakdown table. |
| | | | External Reference Clock Specifications table, added footnote 4, add symbol name vREF-IN-DIFF. |
| | | | Added SERDES External Reference Clock Waveforms. |
| | | | Updated Serial Output Timing and Levels table. |
| | | | Pin-to-pin performance table, changed "typically 3% slower" to "typically slower". |