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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	8375
Number of Logic Elements/Cells	67000
Total RAM Bits	4526080
Number of I/O	380
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-70e-8fn672c

Architecture Overview

Each LatticeECP3 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sys-DSP™ Digital Signal Processing slices, as shown in Figure 2-1. In addition, the LatticeECP3 family contains SERDES Quads on the bottom of the device.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LatticeECP3 devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18Kbit fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, LatticeECP3 devices contain up to two rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The LatticeECP3 devices feature up to 16 embedded 3.2Gbps SERDES (Serializer / Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of four SERDES channels, along with its Physical Coding Sub-layer (PCS) block, creates a quad. The functionality of the SERDES/PCS quads can be controlled by memory cells set during device configuration or by registers that are addressable during device operation. The registers in every quad can be programmed via the SERDES Client Interface (SCI). These quads (up to four) are located at the bottom of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the LatticeECP3 devices are arranged in seven banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. 50% of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3.

Other blocks provided include PLLs, DLLs and configuration functions. The LatticeECP3 architecture provides two Delay Locked Loops (DLLs) and up to ten Phase Locked Loops (PLLs). In addition, each LatticeECP3 family member provides two DLLs per device. The PLL and DLL blocks are located at the end of the EBR/DSP rows.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located toward the center of this EBR row. Every device in the LatticeECP3 family supports a sysCONFIG™ port located in the corner between banks one and two, which allows for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The LatticeECP3 devices use 1.2V as their core voltage.

Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with asynchronous clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals. A 16x2-bit pseudo dual port RAM (PDPR) memory is created by using one Slice as the read-write port and the other companion slice as the read-only port.

LatticeECP3 devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in LatticeECP3 devices, please see TN1179, [LatticeECP3 Memory Usage Guide](#).

Table 2-3. Number of Slices Required to Implement Distributed RAM

	SPR 16X4	PDPR 16X4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

chain in order to better match the reference and feedback signals. This digital code from the ALU is also transmitted via the Digital Control bus (DCNTL) bus to its associated Slave Delay lines (two per DLL). The ALUHOLD input allows the user to suspend the ALU output at its current value. The UDDCNTL signal allows the user to latch the current value on the DCNTL bus.

The DLL has two clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine delay shift and divider blocks to allow this output to be further modified, if required. The fine delay shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. Both the CLKOS and CLKOP outputs are available with optional duty cycle correction. Divide by two and divide by four frequencies are available at CLKOS. The LOCK output signal is asserted when the DLL is locked. Figure 2-5 shows the DLL block diagram and Table 2-5 provides a description of the DLL inputs and outputs.

The user can configure the DLL for many common functions such as time reference delay mode and clock injection removal mode. Lattice provides primitives in its design tools for these functions.

Figure 2-5. Delay Locked Loop Diagram (DLL)

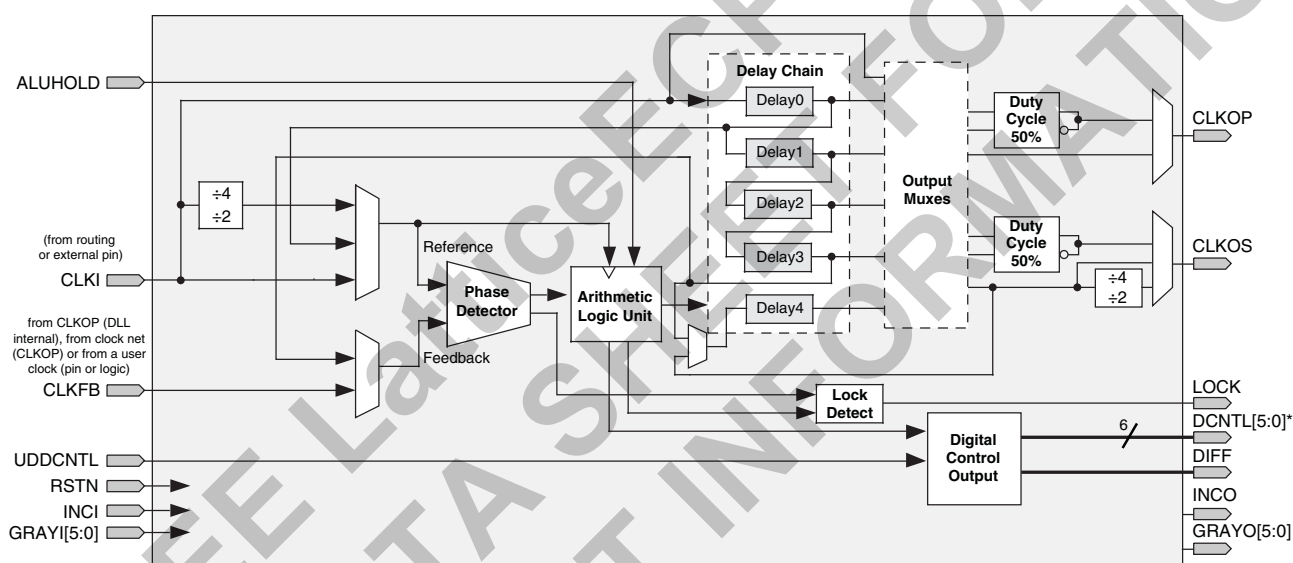


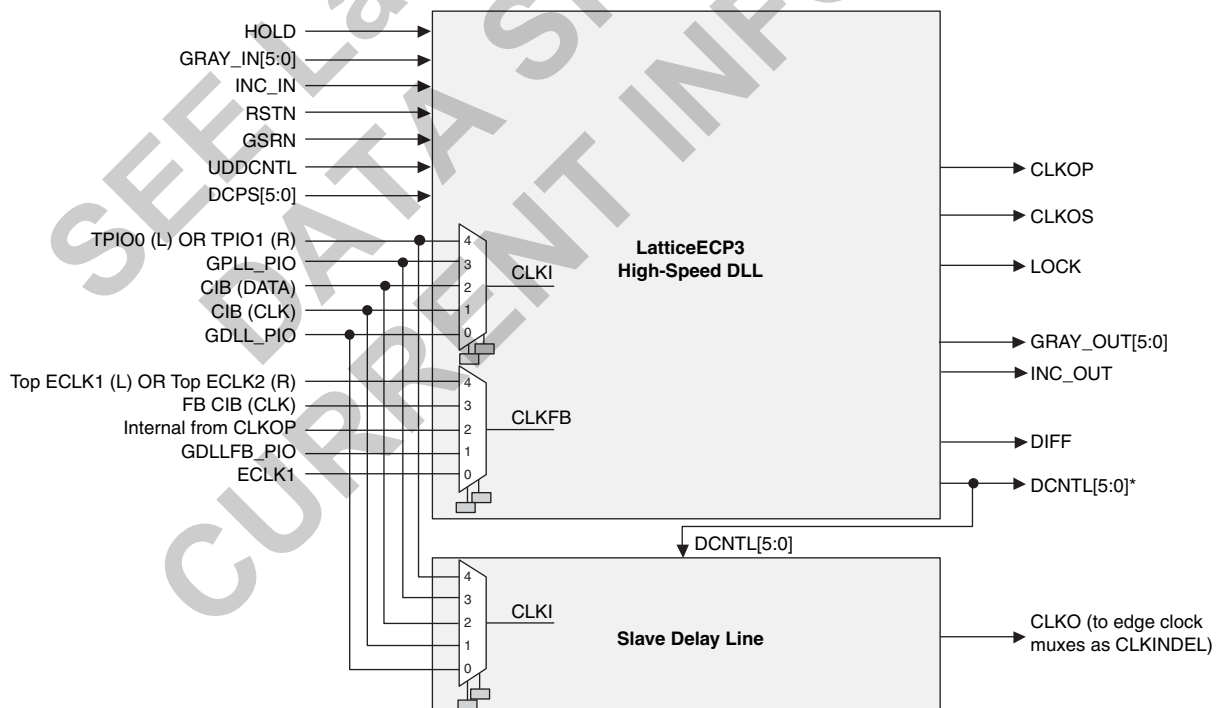
Table 2-5. DLL Signals

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	DLL feed input from DLL output, clock net, routing or external pin
RSTN	I	Active low synchronous reset
ALUHOLD	I	Active high freezes the ALU
UDDCNTL	I	Synchronous enable signal (hold high for two cycles) from routing
CLKOP	O	The primary clock output
CLKOS	O	The secondary clock output with fine delay shift and/or division by 2 or by 4
LOCK	O	Active high phase lock indicator
INCI	I	Incremental indicator from another DLL via CIB.
GRAYI[5:0]	I	Gray-coded digital control bus from another DLL in time reference mode.
DIFF	O	Difference indicator when DCNTL is difference than the internal setting and update is needed.
INCO	O	Incremental indicator to other DLLs via CIB.
GRAYO[5:0]	O	Gray-coded digital control bus to other DLLs via CIB

LatticeECP3 devices have two general DLLs and four Slave Delay lines, two per DLL. The DLLs are in the lowest EBR row and located adjacent to the EBR. Each DLL replaces one EBR block. One Slave Delay line is placed adjacent to the DLL and the duplicate Slave Delay line (in Figure 2-6) for the DLL is placed in the I/O ring between Banks 6 and 7 and Banks 2 and 3.

The outputs from the DLL and Slave Delay lines are fed to the clock distribution network.

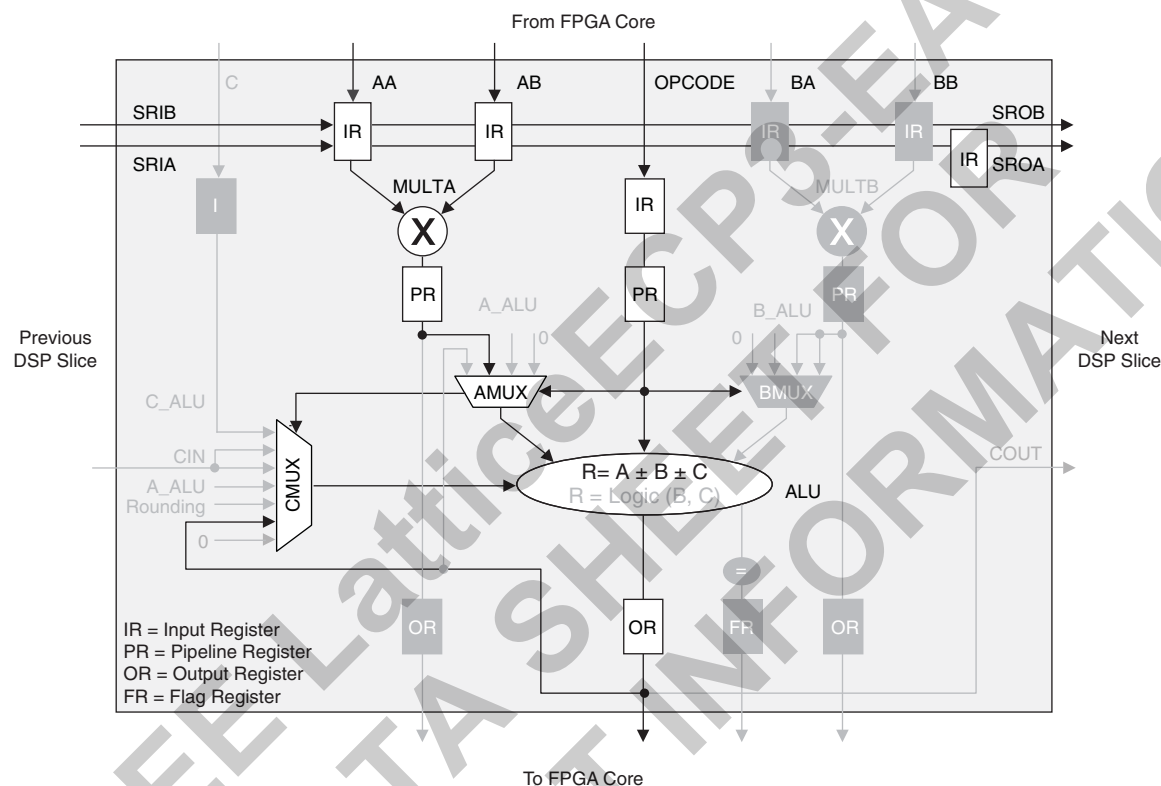
For more information, please see TN1178, [LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide](#).

Figure 2-6. Top-Level Block Diagram, High-Speed DLL and Slave Delay Line

* This signal is not user accessible. It can only be used to feed the slave delay line.

In this case, the two operands, AA and AB, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The ALU is configured as the accumulator in the sysDSP slice in the LatticeECP3 family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-27 shows the MAC sysDSP element.

Figure 2-27. MAC DSP Element



MULTADDSUBSUM DSP Element

In this case, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB of Slice 0. Additionally, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB of Slice 1. The results of both addition/subtractions are added by the second ALU following the slice cascade path. The user can enable the input, output and pipeline registers. Figure 2-30 and Figure 2-31 show the MULTADDSUBSUM sysDSP element.

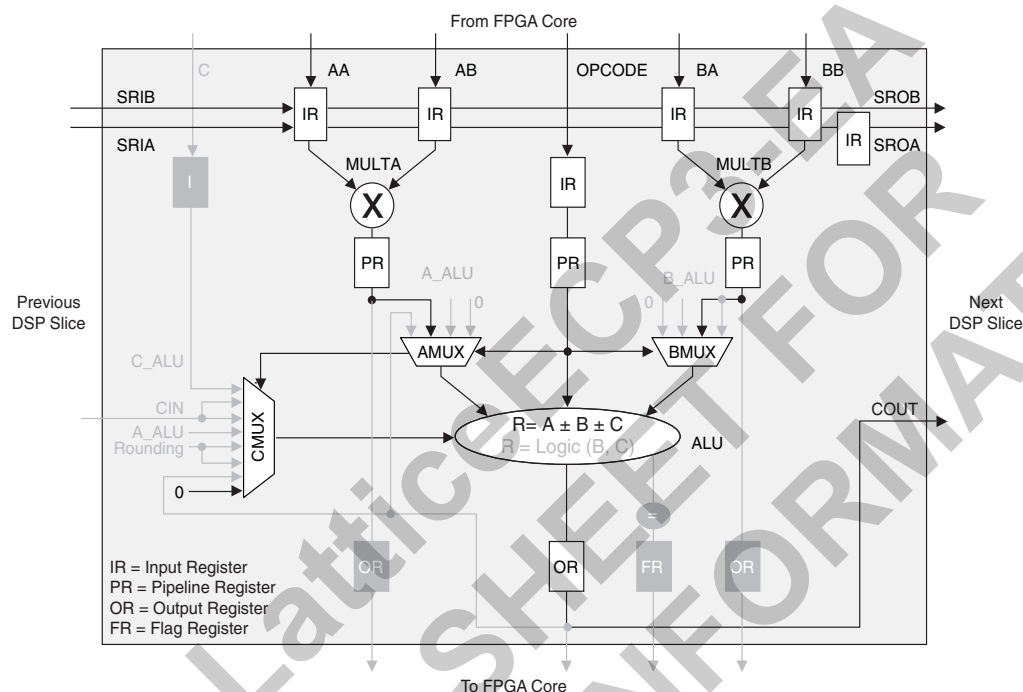
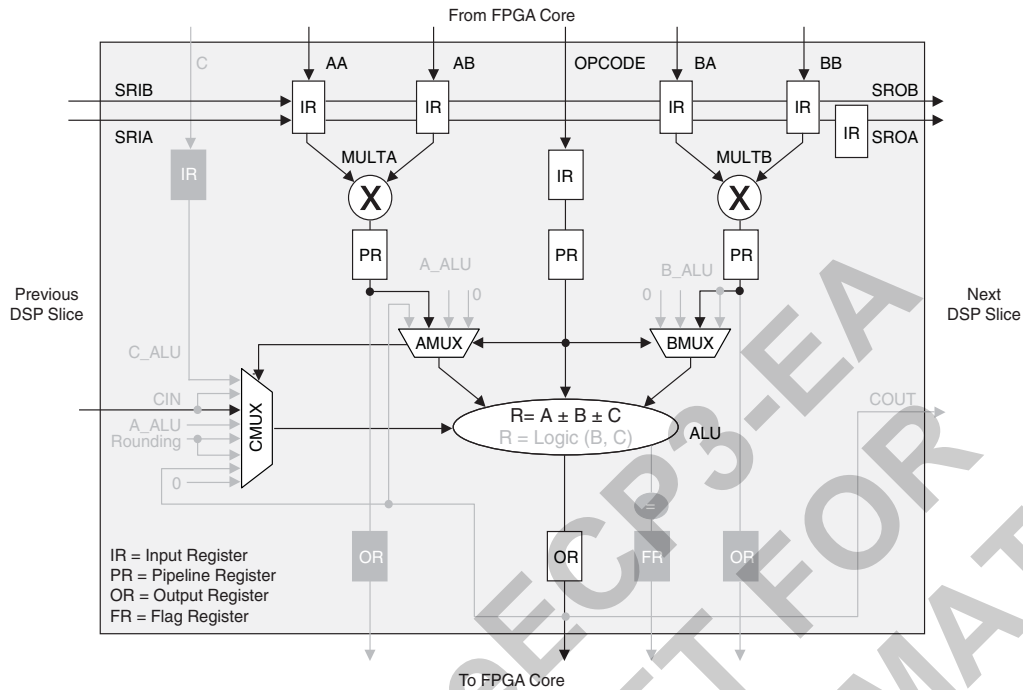
Figure 2-30. MULTADDSUBSUM Slice 0

Figure 2-31. MULTADDSUBSUM Slice 1



Advanced sysDSP Slice Features

Cascading

The LatticeECP3 sysDSP slice has been enhanced to allow cascading. Adder trees are implemented fully in sysDSP slices, improving the performance. Cascading of slices uses the signals CIN, COUT and C Mux of the slice.

Addition

The LatticeECP3 sysDSP slice allows for the bypassing of multipliers and cascading of adder logic. High performance adder functions are implemented without the use of LUTs. The maximum width adders that can be implemented are 54-bit.

Rounding

The rounding operation is implemented in the ALU and is done by adding a constant followed by a truncation operation. The rounding methods supported are:

- Rounding to zero (RTZ)
- Rounding to infinity (RTI)
- Dynamic rounding
- Random rounding
- Convergent rounding

The diagram illustrates the Lattice ECP3Q10000 architecture, showing four memory banks (Bank 0, Bank 1, Bank 2, Bank 3) and a Configuration Bank. Each bank contains DDR DLL (Left and Right) blocks and is connected to a central SERDES block. The diagram also shows DQS Strobe and Transition Detect Logic and I/O Ring components.

Legend:

- DQS Strobe and Transition Detect Logic
- I/O Ring

Bank 0

- DQS
- DQS
- DQS
- DQS
- DQS

Bank 1

- DQS
- DQS
- DQS
- DQS

Configuration Bank

- DQS Delay Control Bus
- ECLK1
- ECLK2
- DQCLK0
- DQCLK1
- DDRLAT
- DDRCLKPOL
- ECLKDQSR
- DATAVALID

Bank 2

- DQS
- DQS
- DQS
- DQS
- DQS
- DQS
- DQS
- DQS

Bank 3

- DQS
- DQS
- DQS
- DQS
- DQS
- DQS
- DQS

Bank 6

- DQS
- DQS
- DQS
- DQS
- DQS
- DQS
- DQS

Bank 7

- DQS
- DQS
- DQS
- DQS
- DQS
- DQS
- DQS

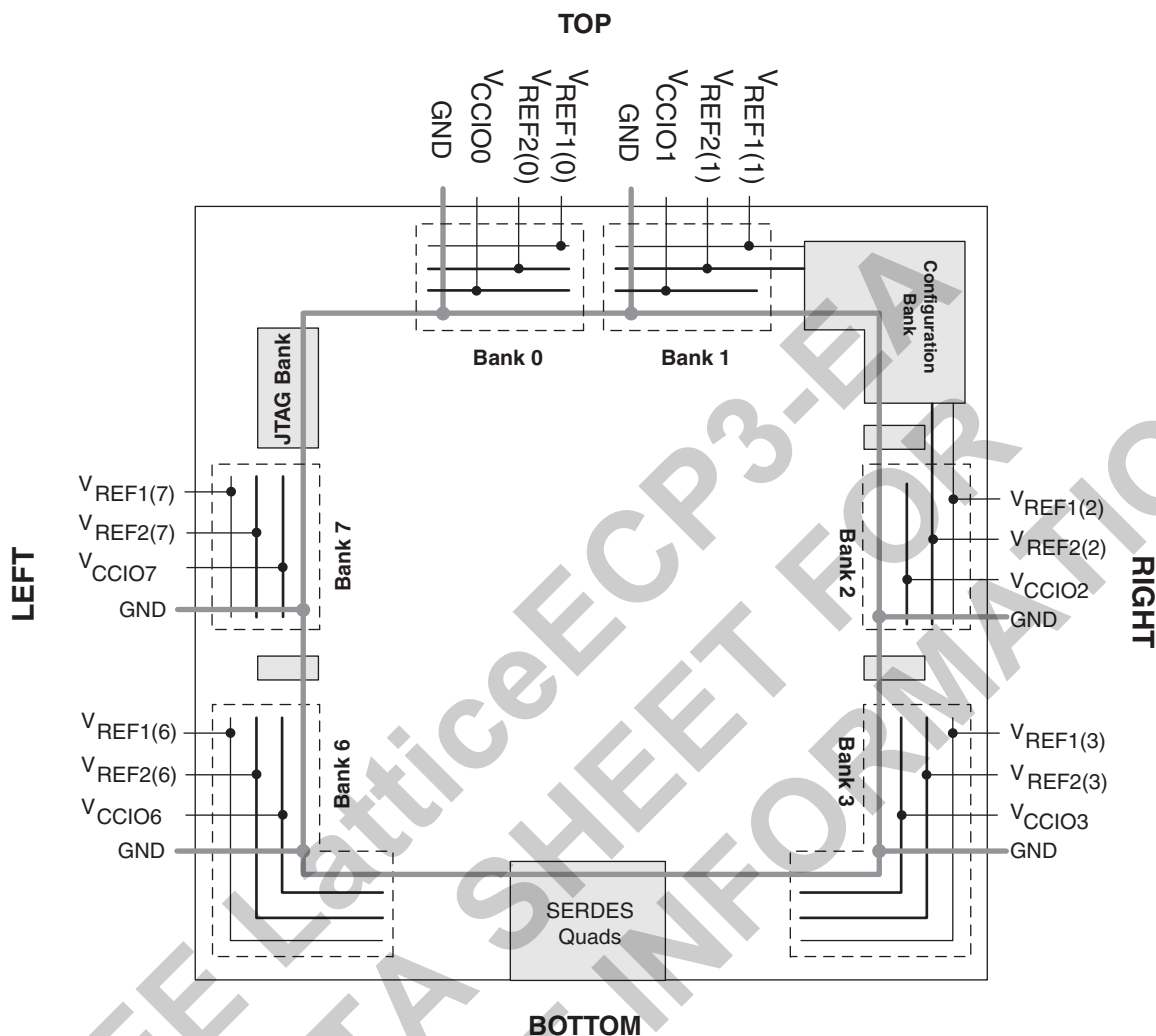
Internal Components:

- DDR DLL (Left)
- DDR DLL (Right)
- SERDES

Notes:

- *Includes shared configuration I/Os and dedicated configuration I/Os.

Figure 2-38. LatticeECP3 Banks



LatticeECP3 devices contain two types of sysI/O buffer pairs.

1. Top (Bank 0 and Bank 1) and Bottom sysI/O Buffer Pairs (Single-Ended Outputs Only)

The sysI/O buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input. Only the top edge buffers have a programmable PCI clamp.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

On the top and bottom sides, there is no support for programmable on-chip input termination, which is required for DQ and DQS pins for DDR3 interface. This side is ideal for ADDR/CMD signals of DDR3, general purpose I/O, PCI, TR-LVDS (transition reduced LVDS) or LVDS inputs. Only the top I/O banks support hot socketing with I_{DK} specified under the Hot Socketing Specifications. The configuration bank is not hot-socketable.

2. Left and Right (Banks 2, 3, 6 and 7) sysI/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)

The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing on these sides as the clamp is always present.

LVDS, RSDS, PPLVDS and Mini-LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

3. Configuration Bank sysI/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)

The sysI/O buffers in the Configuration Bank consist of single-ended output drivers and single-ended input buffers (both ratioed and referenced). The referenced input buffer can also be configured as a differential input.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Programmable PCI clamps are only available on top banks (PCI clamps are used primarily on inputs and bidirectional pads to reduce ringing on the receiving end) can also be used on inputs.

Typical sysI/O I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} , V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LatticeECP3 devices, see the list of technical documentation at the end of this data sheet.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported sysI/O Standards

The LatticeECP3 sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2V, 1.5V, 1.8V, 2.5V and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, MLVDS, RSDS, Mini-LVDS, PPLVDS (point-to-point LVDS), TRLVDS (Transition Reduced LVDS), differential SSTL and differential HSTL. Tables 2-13 and 2-14 show the I/O standards (together with their supply and reference voltages) supported by LatticeECP3 devices. For further information on utilizing the sysI/O buffer to support a variety of standards please see TN1177, [LatticeECP3 sysI/O Usage Guide](#).

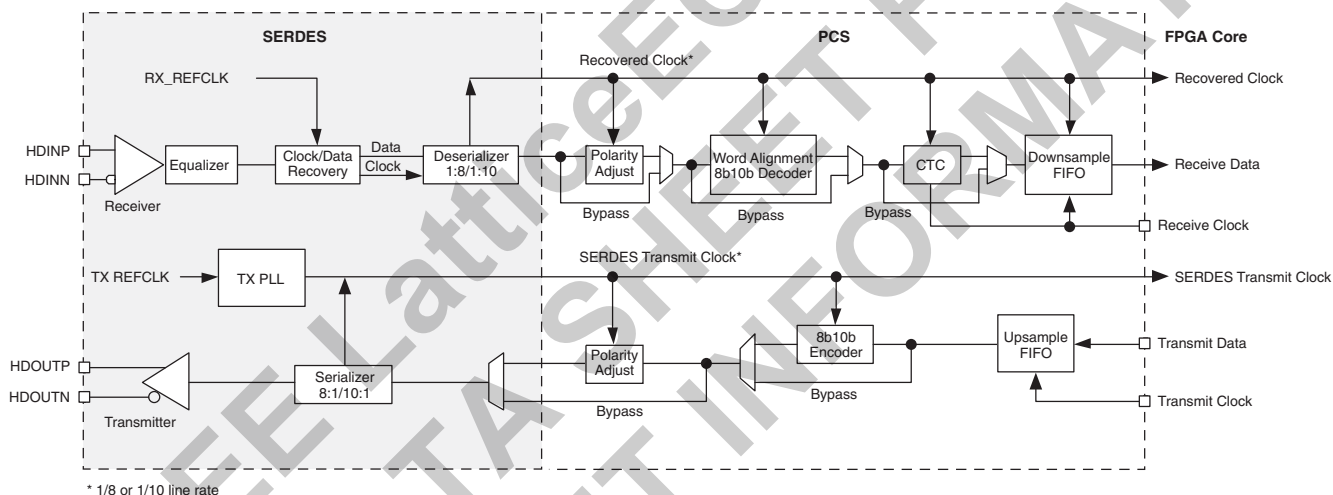
Table 2-14. Available SERDES Quads per LatticeECP3 Devices

Package	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
256 ftBGA	1	1	—	—	—
484 ftBGA	1	1	1	1	—
672 ftBGA	—	1	2	2	2
1156 ftBGA	—	—	3	3	4

SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2-41 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCOB and VCCIB).

Figure 2-41. Simplified Channel Block Diagram for SERDES/PCS Block

PCS

As shown in Figure 2-41, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

SCI (SERDES Client Interface) Bus

The SERDES Client Interface (SCI) is an IP interface that allows the SERDES/PCS Quad block to be controlled by registers rather than the configuration memory cells. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

The ispLEVER design tools from Lattice support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With ispLEVER, the user can define the mode for each quad in a design.

Popular standards such as 10Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), a single quad (Four SERDES channels and PCS) and some additional logic from the core.

The LatticeECP3 family also supports a wide range of primary and secondary protocols. Within the same quad, the LatticeECP3 family can support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. Table 2-15 lists the allowable combination of primary and secondary protocol combinations.

Flexible Quad SERDES Architecture

The LatticeECP3 family SERDES architecture is a quad-based architecture. For most SERDES settings and standards, the whole quad (consisting of four SERDES) is treated as a unit. This helps in silicon area savings, better utilization and overall lower cost.

However, for some specific standards, the LatticeECP3 quad architecture provides flexibility; more than one standard can be supported within the same quad.

Table 2-15 shows the standards can be mixed and matched within the same quad. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same quad. In Table 2-15, the Primary Protocol column refers to the standard that determines the reference clock and PLL settings. The Secondary Protocol column shows the other standard that can be supported within the same quad.

Furthermore, Table 2-15 also implies that more than two standards in the same quad can be supported, as long as they conform to the data rate and reference clock requirements. For example, a quad may contain PCI Express 1.1, SGMII, Serial RapidIO Type I and Serial RapidIO Type II, all in the same quad.

Table 2-15. LatticeECP3 Primary and Secondary Protocol Support

Primary Protocol	Secondary Protocol
PCI Express 1.1	SGMII
PCI Express 1.1	Gigabit Ethernet
PCI Express 1.1	Serial RapidIO Type I
PCI Express 1.1	Serial RapidIO Type II
Serial RapidIO Type I	SGMII
Serial RapidIO Type I	Gigabit Ethernet
Serial RapidIO Type II	SGMII
Serial RapidIO Type II	Gigabit Ethernet
Serial RapidIO Type II	Serial RapidIO Type I
CPRI-3	CPRI-2 and CPRI-1
3G-SDI	HD-SDI and SD-SDI

For further information on SERDES, please see TN1176, [LatticeECP3 SERDES/PCS Usage Guide](#).

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeECP3 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test

LatticeECP3 External Switching Characteristics ^{1, 2}

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Clocks									
Primary Clock ⁶									
f _{MAX_PRI}	Frequency for Primary Clock Tree	ECP3-150EA	—	500	—	420	—	375	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	ECP3-150EA	0.8	—	0.9	—	1.0	—	ns
t _{SKEW_PRI}	Primary Clock Skew Within a Device	ECP3-150EA	—	300	—	330	—	360	ps
t _{SKEW_PRI} B	Primary Clock Skew Within a Bank	ECP3-150EA	—	250	—	280	—	300	ps
f _{MAX_PRI}	Frequency for Primary Clock Tree	ECP3-70E/95E	—	500	—	420	—	375	MHz
f _{MAX_PRI}	Frequency for Primary Clock Tree	ECP3-70E/95E	0.8	—	0.9	—	1.0	—	ns
t _{SKEW_PRI}	Primary Clock Skew Within a Device	ECP3-70E/95E	—	300	—	330	—	360	ps
t _{SKEW_PRI} B	Primary Clock Skew Within a Bank	ECP3-70E/95E	—	250	—	280	—	300	ps
Edge Clock ⁶									
f _{MAX_EDGE}	Frequency for Edge Clock	ECP3-150EA	—	500	—	420	—	375	MHz
t _{W_EDGE}	Clock Pulse Width for Edge Clock	ECP3-150EA	0.9	—	1.0	—	1.2	—	ns
t _{SKEW_EDGE_DQS}	Edge Clock Skew Within an Edge of the Device	ECP3-150EA	—	200	—	210	—	220	ps
f _{MAX_EDGE}	Frequency for Edge Clock	ECP3-70E/95E	—	500	—	420	—	375	MHz
t _{W_EDGE}	Clock Pulse Width for Edge Clock	ECP3-70E/95E	0.9	—	1.0	—	1.2	—	ns
t _{SKEW_EDGE_DQS}	Edge Clock Skew Within an Edge of the Device	ECP3-70E/95E	—	200	—	225	—	250	ps

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic SDR									
General I/O Pin Parameters Using Dedicated Clock Input Primary Clock Without PLL ²									
t _{CO}	Clock to Output - PIO Output Register	ECP3-150EA	—	4.0	—	4.4	—	4.8	ns
t _{SU}	Clock to Data Setup - PIO Input Register	ECP3-150EA	0.0	—	0.0	—	0.0	—	ns
t _H	Clock to Data Hold - PIO Input Register	ECP3-150EA	1.6	—	1.8	—	2.1	—	ns
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-150EA	1.2	—	1.3	—	1.5	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-150EA	0.1	—	0.1	—	0.1	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-150EA	—	500	—	420	—	375	MHz
t _{CO}	Clock to Output - PIO Output Register	ECP3-70E/95E	—	3.9	—	4.3	—	4.7	ns
t _{SU}	Clock to Data Setup - PIO Input Register	ECP3-70E/95E	0.0	—	0.0	—	0.0	—	ns
t _H	Clock to Data Hold - PIO Input Register	ECP3-70E/95E	1.5	—	1.8	—	2.0	—	ns
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-70E/95E	1.3	—	1.5	—	1.8	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-70E/95E	0.0	—	0.0	—	0.0	—	ns

LatticeECP3 External Switching Characteristics (Continued)^{1, 2}

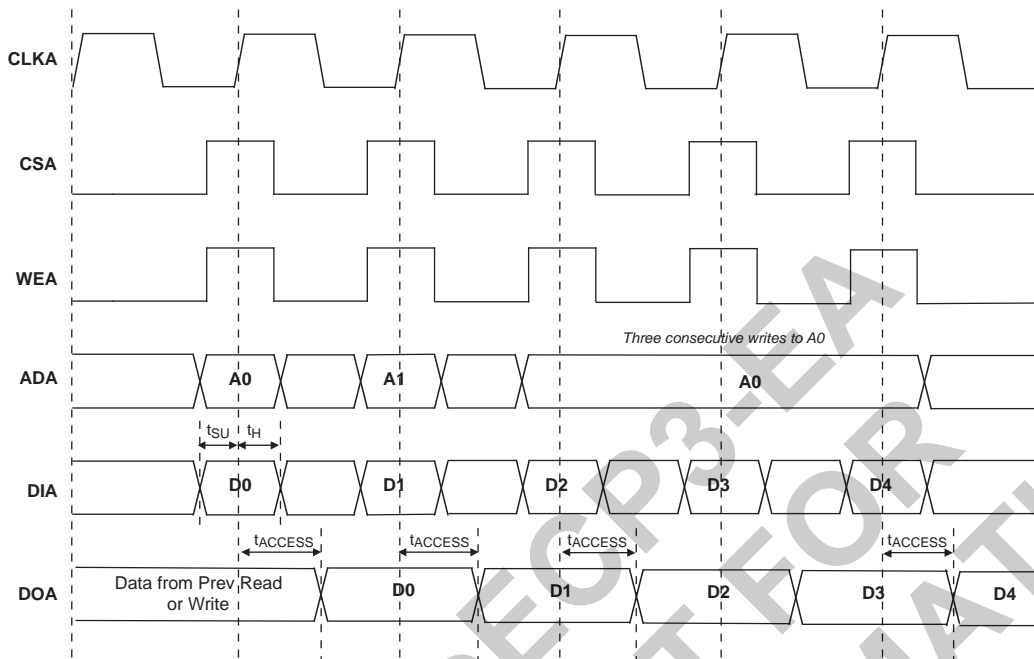
Over Recommended Commercial Operating Conditions

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-70E/95E	0.765	—	0.765	—	0.765	—	UI
f_{MAX_GDDR}	DDR/DDR2 Clock Frequency ⁸	ECP3-70E/95E	—	500	—	420	—	375	MHz
Generic DDR2 Inputs with Clock and Data (<10 Bits Wide) Centered at Pin (GDDR2_RX.DQS.Centered) using DQS Pin for Clock Input									
Left and Right Sides									
t_{SUGDDR}	Data Setup Before CLK	ECP3-150EA	—	—	—	—	—	—	ns
t_{HGDDR}	Data Hold After CLK	ECP3-150EA	—	—	—	—	—	—	ns
f_{MAX_GDDR}	DDR2 Clock Frequency	ECP3-150EA	—	—	—	—	—	—	ns
Generic DDR2 Inputs with Clock and Data (<10 Bits Side) Aligned at Pin (GDDR2_RX.DQS.Aligned) Using DQS Pin for Clock Input									
Left and Right Sides									
$t_{DVACLKGDDR}$	Data Setup Before CLK (Left and Right Side)	ECP3-150EA	—	—	—	—	—	—	
$t_{DVECLKGDDR}$	Data Hold After CLK (Left and Right Side)	ECP3-150EA	—	—	—	—	—	—	
f_{MAX_GDDR}	DDR2 Clock Frequency (Left and Right Side)	ECP3-150EA	—	—	—	—	—	—	
Generic DDR1 Output with Clock and Data (>10 Bits Wide) Centered at Pin (GDDR1_TX.SCLK.Centered)									
Left, Right and Top Sides									
$t_{DVBGDDR}$	Data Valid Before CLK	ECP3-150EA	—	—	—	—	—	—	
$t_{DVAGDDR}$	Data Valid After CLK	ECP3-150EA	—	—	—	—	—	—	
f_{MAX_GDDR}	DDR1 Clock Frequency	ECP3-150EA	—	—	—	—	—	—	
Generic DDR1 Outputs with clock in the center of data window, with PLL 90-degree shifted clock output (GDDR1_TX.ECLK.Centered)									
$t_{DIBGDDR}$	Data Invalid Before CLK	ECP3-70E/95E	670	—	670	—	670	—	ps
$t_{DIAGDDR}$	Data Invalid After CLK	ECP3-70E/95E	670	—	670	—	670	—	ps
f_{MAX_GDDR}	DDR1 Clock Frequency	ECP3-70E/95E	—	250	—	250	—	250	MHz
Generic DDR1 Output with Clock and Data (> 10 Bits Wide) Aligned at Pin (GDDR1_TX.SCLK.Aligned)									
Left, Right and Top Sides									
$t_{DIBGDDR}$	Data Hold After CLK	ECP3-150EA	—	—	—	—	—	—	
$t_{DIAGDDR}$	Data Setup Before CLK	ECP3-150EA	—	—	—	—	—	—	
f_{MAX_GDDR}	DDR1 Clock Frequency	ECP3-150EA	—	—	—	—	—	—	
Generic DDR1 Outputs with clock and data edge aligned, without PLL									
$t_{DIBGDDR}$	Data Invalid Before CLK	ECP3-70E/95E	—	330	—	330	—	330	ps
$t_{DIAGDDR}$	Data Invalid After CLK	ECP3-70E/95E	—	330	—	330	—	330	ps
f_{MAX_GDDR}	DDR1 Clock Frequency	ECP3-70E/95E	—	250	—	250	—	250	MHz
Generic DDR1 Output with Clock and Data (<10 Bits Wide) Centered at Pin (GDDR1_TX.DQS.Centered)									
Left, Right and Top Sides									
$t_{DVBGDDR}$	Data Valid Before CLK	ECP3-150EA	—	—	—	—	—	—	
$t_{DVAGDDR}$	Data Valid After CLK	ECP3-150EA	—	—	—	—	—	—	
f_{MAX_GDDR}	DDR1 Clock Frequency	ECP3-150EA	—	—	—	—	—	—	

LatticeECP3 Internal Switching Characteristics^{1, 2}

Over Recommended Commercial Operating Conditions

Parameter	Description	-8		-7		-6		Units.
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t _{LUT4_PFU}	LUT4 delay (A to D inputs to F output)	—	0.147	—	0.163	—	0.179	ns
t _{LUT6_PFU}	LUT6 delay (A to D inputs to OFX output)	—	0.273	—	0.307	—	0.342	ns
t _{LSR_PFU}	Set/Reset to output of PFU (Asynchronous)	—	0.593	—	0.674	—	0.756	ns
t _{LSRREC_PFU}	Asynchronous Set/Reset recovery time for PFU Logic	—	0.298	—	0.345	—	0.391	ns
t _{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.134	—	0.144	—	0.153	—	ns
t _{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	-0.097	—	-0.103	—	-0.109	—	ns
t _{SUD_PFU}	Clock to D input setup time	0.061	—	0.068	—	0.075	—	ns
t _{HD_PFU}	Clock to D input hold time	0.019	—	0.013	—	0.015	—	ns
t _{CK2Q_PFU}	Clock to Q delay, (D-type Register Configuration)	—	0.243	—	0.273	—	0.303	ns
PFU Dual Port Memory Mode Timing								
t _{CORAM_PFU}	Clock to Output (F Port)	—	0.710	—	0.803	—	0.897	ns
t _{SUDATA_PFU}	Data Setup Time	-0.137	—	-0.155	—	-0.174	—	ns
t _{HDATA_PFU}	Data Hold Time	0.188	—	0.217	—	0.246	—	ns
t _{SUADDR_PFU}	Address Setup Time	-0.227	—	-0.257	—	-0.286	—	ns
t _{HADDR_PFU}	Address Hold Time	0.240	—	0.275	—	0.310	—	ns
t _{SUWREN_PFU}	Write/Read Enable Setup Time	-0.055	—	-0.055	—	-0.063	—	ns
t _{HWREN_PFU}	Write/Read Enable Hold Time	0.059	—	0.059	—	0.071	—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t _{IN_PIO}	Input Buffer Delay (LVCMOS25)	—	0.423	—	0.466	—	0.508	ns
t _{OUT_PIO}	Output Buffer Delay (LVCMOS25)	—	1.115	—	1.155	—	1.196	ns
IOLOGIC Input/Output Timing								
t _{SUI_PIO}	Input Register Setup Time (Data Before Clock)	0.956	—	1.124	—	1.293	—	ns
t _{HI_PIO}	Input Register Hold Time (Data after Clock)	0.313	—	0.395	—	0.378	—	ns
t _{COO_PIO}	Output Register Clock to Output Delay [†]	—	1.455	—	1.564	—	1.674	ns
t _{SUCE_PIO}	Input Register Clock Enable Setup Time	0.220	—	0.185	—	0.150	—	ns
t _{HCE_PIO}	Input Register Clock Enable Hold Time	-0.085	—	-0.072	—	-0.058	—	ns
t _{SULSR_PIO}	Set/Reset Setup Time	0.117	—	0.103	—	0.088	—	ns
t _{HLSR_PIO}	Set/Reset Hold Time	-0.107	—	-0.094	—	-0.081	—	ns
EBR Timing								
t _{CO_EBR}	Clock (Read) to output from Address or Data	—	2.78	—	2.89	—	2.99	ns
t _{COO_EBR}	Clock (Write) to output from EBR output Register	—	0.31	—	0.32	—	0.33	ns
t _{SUDATA_EBR}	Setup Data to EBR Memory	-0.218	—	-0.227	—	-0.237	—	ns
t _{HDATA_EBR}	Hold Data to EBR Memory	0.249	—	0.257	—	0.265	—	ns
t _{SUADDR_EBR}	Setup Address to EBR Memroy	-0.071	—	-0.070	—	-0.068	—	ns
t _{HADDR_EBR}	Hold Address to EBR Memory	0.118	—	0.098	—	0.077	—	ns
t _{SUWREN_EBR}	Setup Write/Read Enable to PFU Memory	-0.107	—	-0.106	—	-0.106	—	ns

Figure 3-11. Write Through (SP Read/Write on Port A, Input Registers Only)

Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

DLL Timing

Over Recommended Operating Conditions

Parameter	Description	Condition	Min.	Typ.	Max.	Units
f_{REF}	Input reference clock frequency (on-chip or off-chip)		133	—	500	MHz
f_{FB}	Feedback clock frequency (on-chip or off-chip)		133	—	500	MHz
f_{CLKOP}^1	Output clock frequency, CLKOP		133	—	500	MHz
f_{CLKOS}^2	Output clock frequency, CLKOS		33.3	—	500	MHz
t_{PJIT}	Output clock period jitter (clean input)			—	200	ps p-p
t_{DUTY}	Output clock duty cycle (at 50% levels, 50% duty cycle input clock, 50% duty cycle circuit turned off, time reference delay mode)	Edge Clock	40		60	%
		Primary Clock	30		70	%
$t_{DUTYTRD}$	Output clock duty cycle (at 50% levels, arbitrary duty cycle input clock, 50% duty cycle circuit enabled, time reference delay mode)	Primary Clock < 250MHz	45		55	%
		Primary Clock ≥ 250MHz	30		70	%
		Edge Clock	45		55	%
$t_{DUTYCIR}$	Output clock duty cycle (at 50% levels, arbitrary duty cycle input clock, 50% duty cycle circuit enabled, clock injection removal mode) with DLL cascading	Primary Clock < 250MHz	40		60	%
		Primary Clock ≥ 250MHz	30		70	%
		Edge Clock	45		55	%
t_{SKEW}^3	Output clock to clock skew between two outputs with the same phase setting		—	—	100	ps
t_{PHASE}	Phase error measured at device pads between off-chip reference clock and feedback clocks		—	—	+/-400	ps
t_{PWH}	Input clock minimum pulse width high (at 80% level)		550	—	—	ps
t_{PWL}	Input clock minimum pulse width low (at 20% level)		550	—	—	ps
t_{INSTB}	Input clock period jitter		—	—	500	p-p
t_{LOCK}	DLL lock time		8	—	8200	cycles
t_{RSWD}	Digital reset minimum pulse width (at 80% level)		3	—	—	ns
t_{DEL}	Delay step size		27	45	70	ps
t_{RANGE1}	Max. delay setting for single delay block (64 taps)		1.9	3.1	4.4	ns
t_{RANGE4}	Max. delay setting for four chained delay blocks		7.6	12.4	17.6	ns

1. CLKOP runs at the same frequency as the input clock.

2. CLKOS minimum frequency is obtained with divide by 4.

3. This is intended to be a “path-matching” design guideline and is not a measurable specification.

SERDES/PCS Block Latency

Table 3-8 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3-12 shows the location of each block.

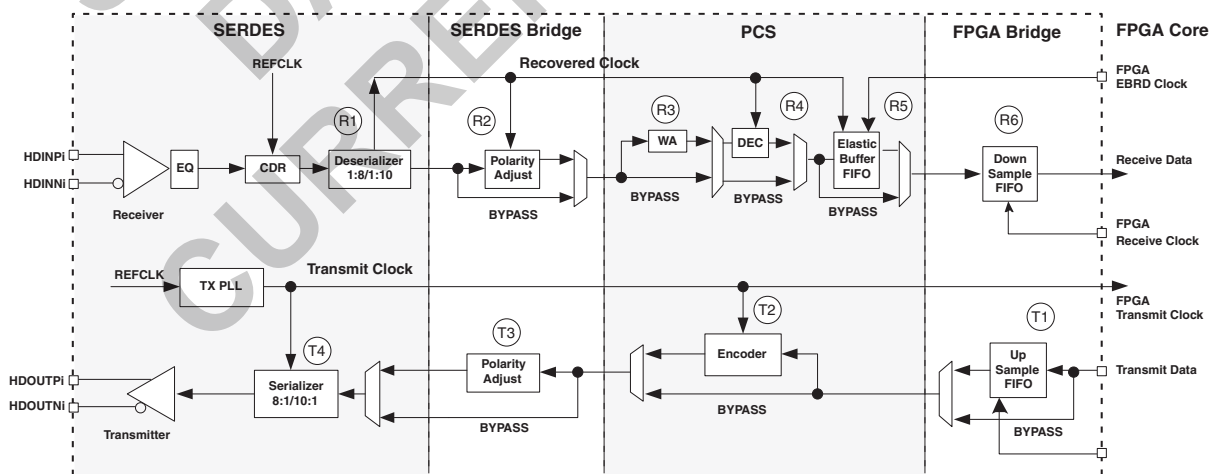
Table 3-8. SERDES/PCS Latency Breakdown

Item	Description	Min.	Avg.	Max.	Fixed	Bypass	Units
Transmit Data Latency¹							
T1	FPGA Bridge - Gearing disabled with different clocks	1	3	5	—	1	word clk
	FPGA Bridge - Gearing disabled with same clocks	—	—	—	3	1	word clk
	FPGA Bridge - Gearing enabled	1	3	5	—	—	word clk
T2	8b10b Encoder	—	—	—	2	1	word clk
T3	SERDES Bridge transmit	—	—	—	2	1	word clk
T4	Serializer: 8-bit mode	—	—	—	15 + $\Delta 1$	—	UI + ps
	Serializer: 10-bit mode	—	—	—	18 + $\Delta 1$	—	UI + ps
T5	Pre-emphasis ON	—	—	—	1 + $\Delta 2$	—	UI + ps
	Pre-emphasis OFF	—	—	—	0 + $\Delta 3$	—	UI + ps
Receive Data Latency²							
R1	Equalization ON	—	—	—	$\Delta 1$	—	UI + ps
	Equalization OFF	—	—	—	$\Delta 2$	—	UI + ps
R2	Deserializer: 8-bit mode	—	—	—	10 + $\Delta 3$	—	UI + ps
	Deserializer: 10-bit mode	—	—	—	12 + $\Delta 3$	—	UI + ps
R3	SERDES Bridge receive	—	—	—	2	—	word clk
R4	Word alignment	3.1	—	4	—	—	word clk
R5	8b10b decoder	—	—	—	1	—	word clk
R6	Clock Tolerance Compensation	7	15	23	1	1	word clk
R7	FPGA Bridge - Gearing disabled with different clocks	1	3	5	—	1	word clk
	FPGA Bridge - Gearing disabled with same clocks	—	—	—	3	1	word clk
	FPGA Bridge - Gearing enabled	1	3	5	—	—	word clk

1. $\Delta 1 = -245\text{ps}$, $\Delta 2 = +88\text{ps}$, $\Delta 3 = +112\text{ps}$.

2. $\Delta 1 = +118\text{ps}$, $\Delta 2 = +132\text{ps}$, $\Delta 3 = +700\text{ps}$.

Figure 3-12. Transmitter and Receiver Latency Block Diagram



Pin Information Summary (Cont.)

Pin Information Summary		ECP3-95E/EA			ECP3-150EA	
Pin Type		484 fpBGA	672 fpBGA	1156 fpBGA	672 fpBGA	1156 fpBGA
General Purpose Inputs/Outputs per bank	Bank 0	42	60	86	60	94
	Bank 1	36	48	78	48	86
	Bank 2	24	34	36	34	58
	Bank 3	54	59	86	59	104
	Bank 6	63	67	86	67	104
	Bank 7	36	48	54	48	76
	Bank 8	24	24	24	24	24
General Purpose Inputs per Bank	Bank 0	0	0	0	0	0
	Bank 1	0	0	0	0	0
	Bank 2	4	8	8	8	8
	Bank 3	4	12	12	12	12
	Bank 6	4	12	12	12	12
	Bank 7	4	8	8	8	8
	Bank 8	0	0	0	0	0
General Purpose Outputs per Bank	Bank 0	0	0	0	0	0
	Bank 1	0	0	0	0	0
	Bank 2	0	0	0	0	0
	Bank 3	0	0	0	0	0
	Bank 6	0	0	0	0	0
	Bank 7	0	0	0	0	0
	Bank 8	0	0	0	0	0
Total Single-Ended User I/O		295	380	490	380	586
VCC		16	32	32	32	32
VCCAUX		8	12	16	12	16
VTT		4	4	8	4	8
VCCA		4	8	16	8	16
VCCPLL		4	4	4	4	4
VCCIO	Bank 0	2	4	4	4	4
	Bank 1	2	4	4	4	4
	Bank 2	2	4	4	4	4
	Bank 3	2	4	4	4	4
	Bank 6	2	4	4	4	4
	Bank 7	2	4	4	4	4
	Bank 8	2	2	2	2	2
VCCJ		1	1	1	1	1
TAP		4	4	4	4	4
GND, GNDIO		98	139	233	139	233
NC		0	0	238	0	116
Reserved ¹		2	2	2	2	2
SERDES		26	52	78	52	104
Miscellaneous Pins		8	8	8	8	8
Total Bonded Pins		484	672	1156	672	1156

For Further Information

A variety of technical notes for the LatticeECP3 family are available on the Lattice website at www.latticesemi.com.

- TN1169, [LatticeECP3 sysCONFIG Usage Guide](#)
- TN1176, [LatticeECP3 SERDES/PCS Usage Guide](#)
- TN1177, [LatticeECP3 sysIO Usage Guide](#)
- TN1178, [LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide](#)
- TN1179, [LatticeECP3 Memory Usage Guide](#)
- TN1180, [LatticeECP3 High-Speed I/O Interface](#)
- TN1181, [Power Consumption and Management for LatticeECP3 Devices](#)
- TN1182, [LatticeECP3 sysDSP Usage Guide](#)
- TN1184, [LatticeECP3 Soft Error Detection \(SED\) Usage Guide](#)
- TN1189, [LatticeECP3 Hardware Checklist](#)

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com