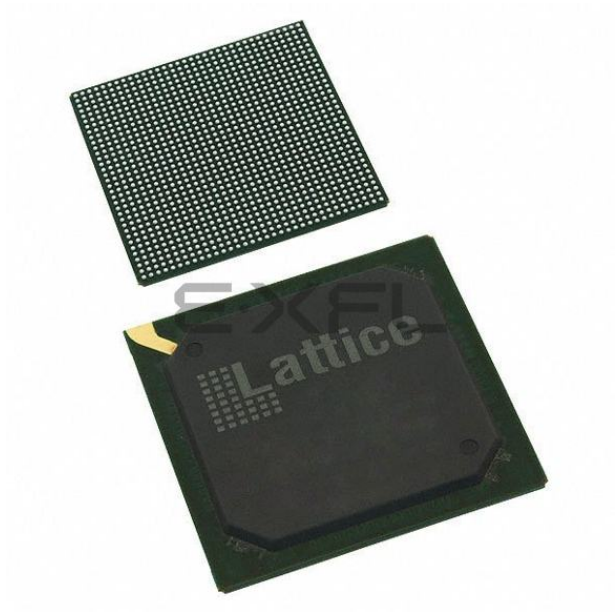
Lattice Semiconductor Corporation - LFE3-95E-6FN1156C Datasheet



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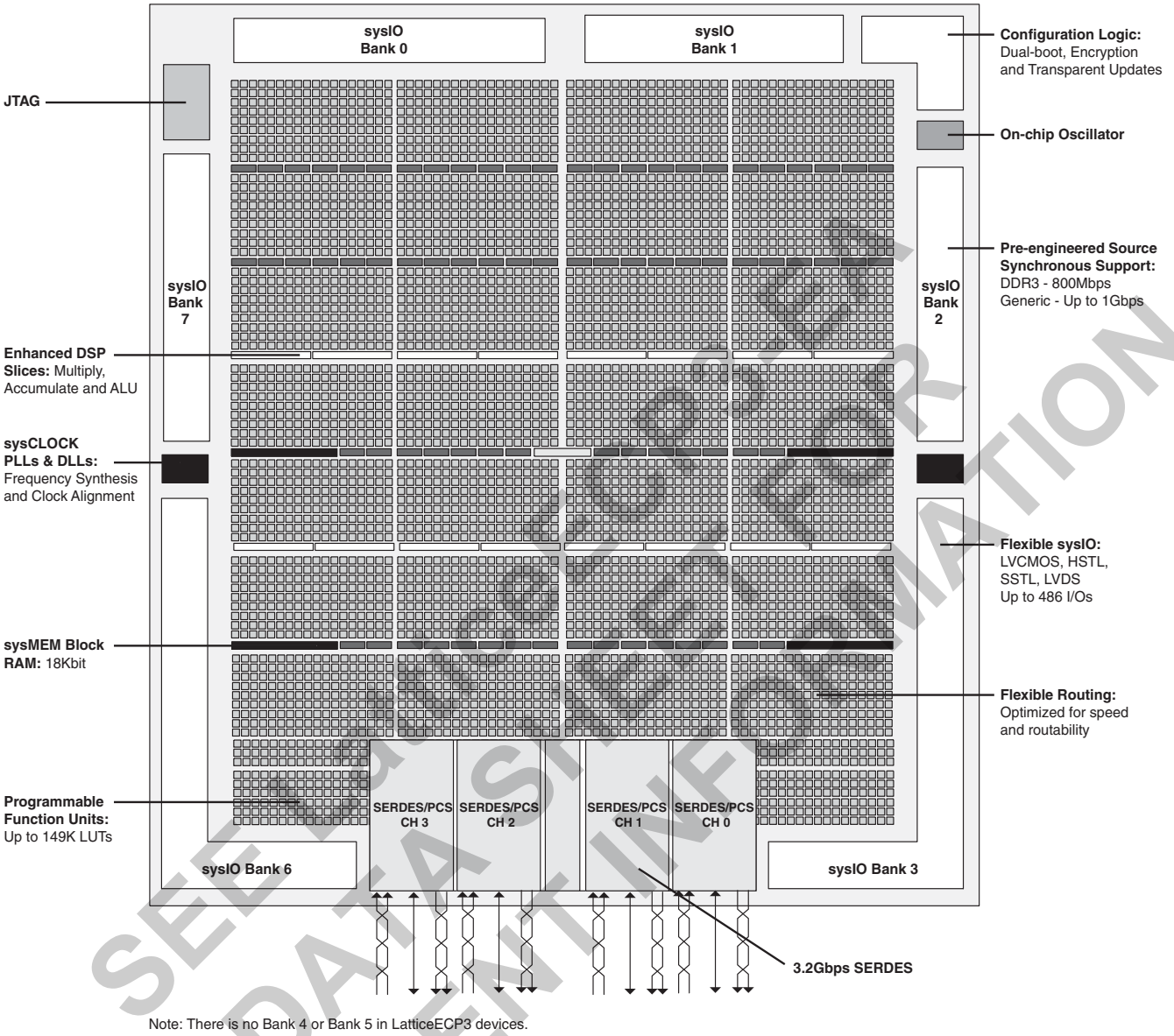
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	11500
Number of Logic Elements/Cells	92000
Total RAM Bits	4526080
Number of I/O	490
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95e-6fn1156c

Figure 2-1. Simplified Block Diagram, LatticeECP3-35 Device (Top Level)



Note: There is no Bank 4 or Bank 5 in LatticeECP3 devices.

PFU Blocks

The core of the LatticeECP3 device consists of PFU blocks, which are provided in two forms, the PFU and PFF. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices numbered 0-3 as shown in Figure 2-2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

ROM Mode
ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, please refer to TN1179, LatticeECP3 Memory Usage Guide.

Routing

There are many resources provided in the LatticeECP3 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The LatticeECP3 family has an enhanced routing architecture that produces a compact design. The ispLEVER design tool suite takes the output of the synthesis tool and places and routes the design.

sysCLOCK PLLs and DLLs

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. All the devices in the LatticeECP3 family support four to ten full-featured General Purpose PLLs.

General Purpose PLL

The architecture of the PLL is shown in Figure 2-4. A description of the PLL functionality follows.

CLKI is the reference frequency (generated either from the pin or from routing) for the PLL. CLKI feeds into the Input Clock Divider block. The CLKFB is the feedback signal (generated from CLKOP, CLKOS or from a user clock pin/logic). This signal feeds into the Feedback Divider. The Feedback Divider is used to multiply the reference frequency.

Both the input path and feedback signals enter the Voltage Controlled Oscillator (VCO) block. In this block the difference between the input path and feedback signals is used to control the frequency and phase of the oscillator. A LOCK signal is generated by the VCO to indicate that the VCO has locked onto the input clock signal. In dynamic mode, the PLL may lose lock after a dynamic delay adjustment and not relock until the t_{LOCK} parameter has been satisfied.

The output of the VCO then enters the CLKOP divider. The CLKOP divider allows the VCO to operate at higher frequencies than the clock output (CLKOP), thereby increasing the frequency range. The Phase/Duty Select block adjusts the phase and duty cycle of the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted. A secondary divider takes the CLKOP or CLKOS signal and uses it to derive lower frequency outputs (CLKOK).

The primary output from the CLKOP divider (CLKOP) along with the outputs from the secondary dividers (CLKOK and CLKOK2) and Phase/Duty select (CLKOS) are fed to the clock distribution network.

The PLL allows two methods for adjusting the phase of signal. The first is referred to as Fine Delay Adjustment. This inserts up to 16 nominal 125ps delays to be applied to the secondary PLL output. The number of steps may be set statically or from the FPGA logic. The second method is referred to as Coarse Phase Adjustment. This allows the phase of the rising and falling edge of the secondary PLL output to be adjusted in 22.5 degree steps. The number of steps may be set statically or from the FPGA logic.

Figure 2-4. General Purpose PLL Diagram

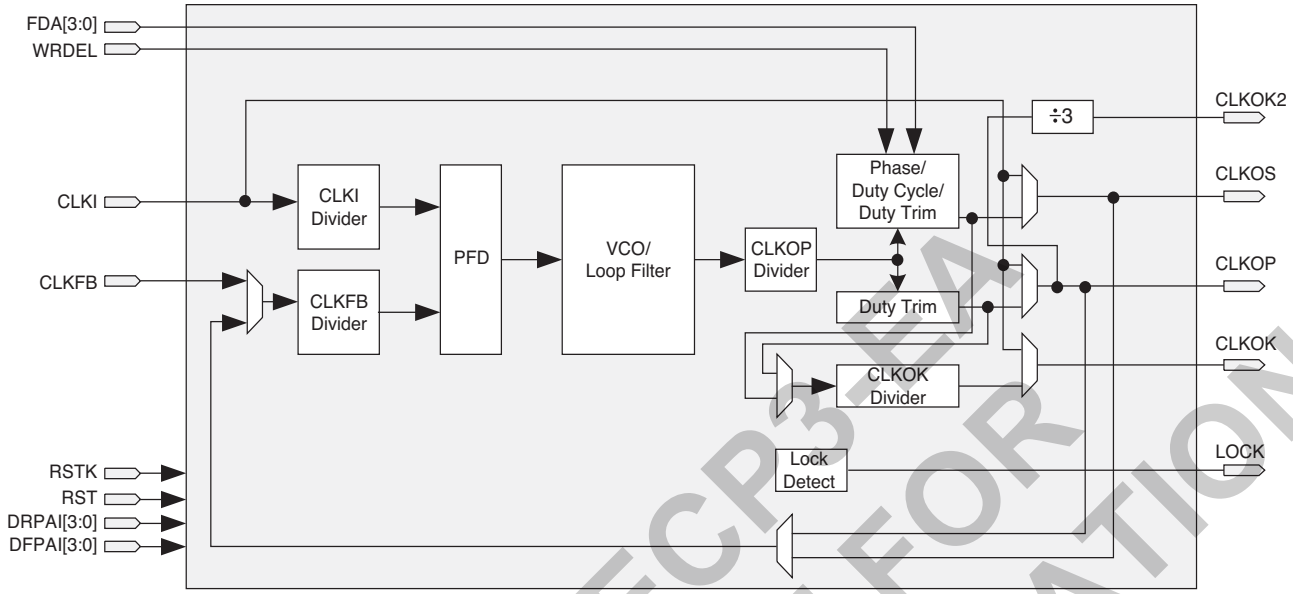


Table 2-4 provides a description of the signals in the PLL blocks.

Table 2-4. PLL Blocks Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP, CLKOS, or from a user clock (pin or logic)
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	"1" to reset K-divider
WRDEL	I	DPA Fine Delay Adjust input
CLKOS	O	PLL output to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output to clock tree (no phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
CLKOK2	O	PLL output to clock tree (CLKOP divided by 3)
LOCK	O	"1" indicates PLL LOCK to CLKI
FDA [3:0]	I	Dynamic fine delay adjustment on CLKOS output
DRPAI[3:0]	I	Dynamic coarse phase shift, rising edge setting
DFPAI[3:0]	I	Dynamic coarse phase shift, falling edge setting

Delay Locked Loops (DLL)

In addition to PLLs, the LatticeECP3 family of devices has two DLLs per device.

CLKI is the input frequency (generated either from the pin or routing) for the DLL. CLKI feeds into the output muxes block to bypass the DLL, directly to the DELAY CHAIN block and (directly or through divider circuit) to the reference input of the Phase Detector (PD) input mux. The reference signal for the PD can also be generated from the Delay Chain signals. The feedback input to the PD is generated from the CLKFB pin or from a tapped signal from the Delay chain.

The PD produces a binary number proportional to the phase and frequency difference between the reference and feedback signals. Based on these inputs, the ALU determines the correct digital control codes to send to the delay

PLL/DLL Cascading

LatticeECP3 devices have been designed to allow certain combinations of PLL and DLL cascading. The allowable combinations are:

- PLL to PLL supported
- PLL to DLL supported

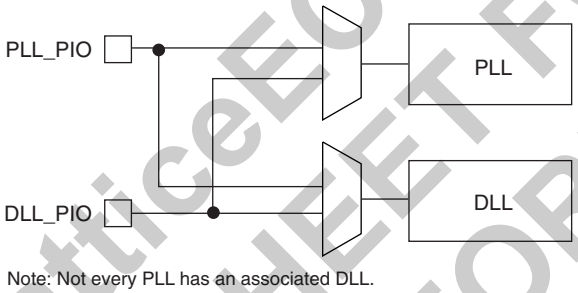
The DLLs in the LatticeECP3 are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLLs and PLLs.

For further information about the DLL, please see the list of technical documentation at the end of this data sheet.

PLL/DLL PIO Input Pin Connections

All LatticeECP3 devices contains two DLLs and up to ten PLLs, arranged in quadrants. If a PLL and a DLL are next to each other, they share input pins as shown in the Figure 2-7.

Figure 2-7. Sharing of PIO Pins by PLLs and DLLs in LatticeECP3 Devices



Note: Not every PLL has an associated DLL.

Clock Dividers

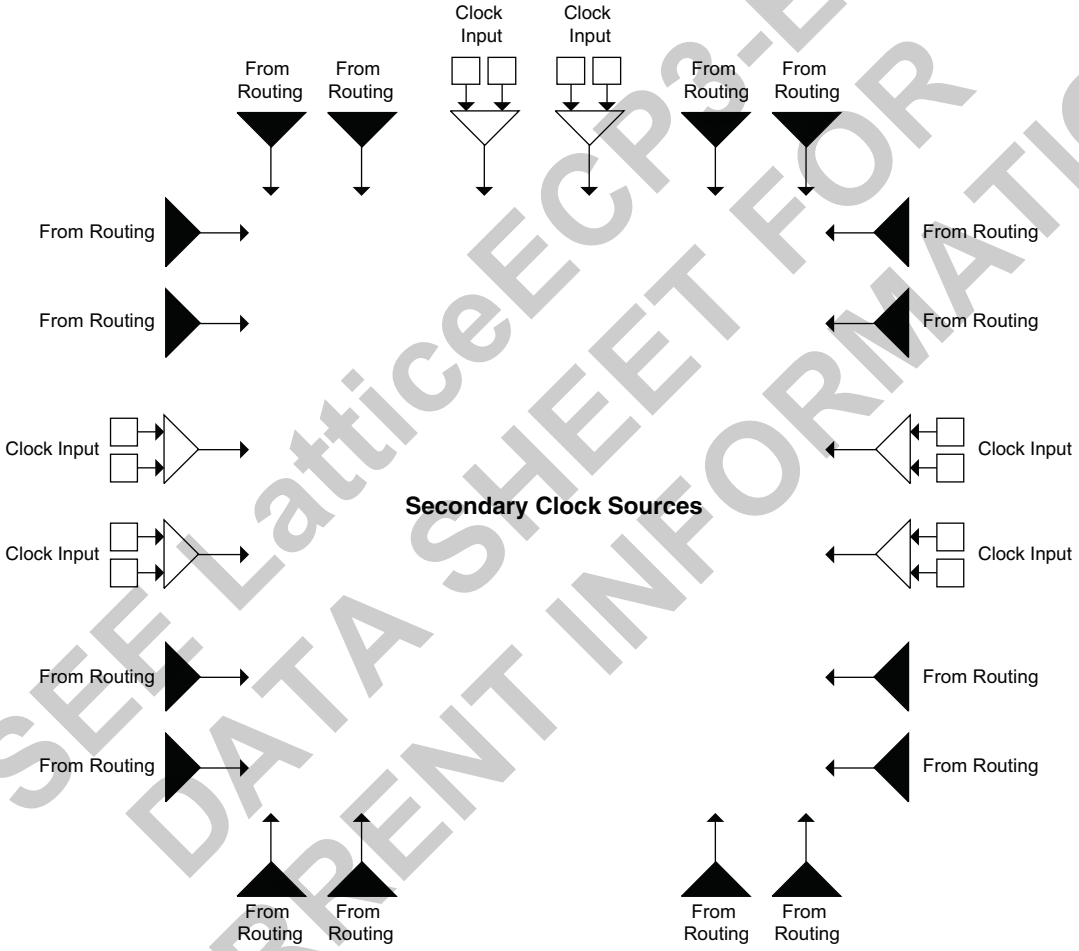
LatticeECP3 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PLL/DLL outputs, the Slave Delay lines, routing or from an external clock input. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and asynchronously forces all outputs to low. The RELEASE signal releases outputs synchronously to the input clock. For further information on clock dividers, please see TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide. Figure 2-8 shows the clock divider connections.

Secondary Clock/Control Sources

LatticeECP3 devices derive eight secondary clock sources (SC0 through SC7) from six dedicated clock input pads and the rest from routing. Figure 2-14 shows the secondary clock sources. All eight secondary clock sources are defined as inputs to a per-region mux SC0-SC7. SC0-SC3 are primary for control signals (CE and/or LSR), and SC4-SC7 are for clock and high fanout data.

In an actual implementation, there is some overlap to maximize routability. In addition to SC0-SC3, SC7 is also an input to the control signals (LSR or CE). SC0-SC2 are also inputs to clocks along with SC4-SC7. High fanout logic signals (LUT inputs) will utilize the X2 and X0 switches where SC0-SC7 are inputs to X2 switches, and SC4-SC7 are inputs to X0 switches. Note that through X0 switches, SC4-SC7 can also access control signals CE/LSR.

Figure 2-14. Secondary Clock Sources

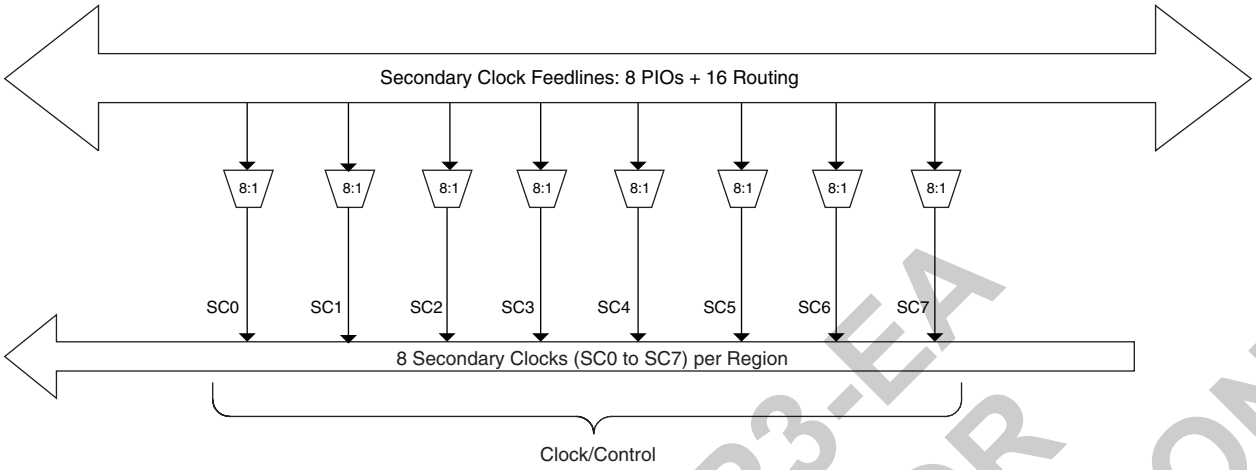


Note: Clock inputs can be configured in differential or single-ended mode.

Secondary Clock/Control Routing

Global secondary clock is a secondary clock that is distributed to all regions. The purpose of the secondary clock routing is to distribute the secondary clock sources to the secondary clock regions. Secondary clocks in the LatticeECP3 devices are region-based resources. Certain EBR rows and special vertical routing channels bind the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP slice in the DSP row or the center of the DSP row. Figure 2-15 shows this special vertical routing channel and the 20 secondary clock regions for the LatticeECP3 family of devices. All devices in the LatticeECP3 family have eight

Figure 2-16. Per Region Secondary Clock Selection



Slice Clock Selection

Figure 2-17 shows the clock selections and Figure 2-18 shows the control selections for Slice0 through Slice2. All the primary clocks and seven secondary clocks are routed to this clock selection mux. Other signals can be used as a clock input to the slices via routing. Slice controls are generated from the secondary clocks/controls or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-17. Slice0 through Slice2 Clock Selection

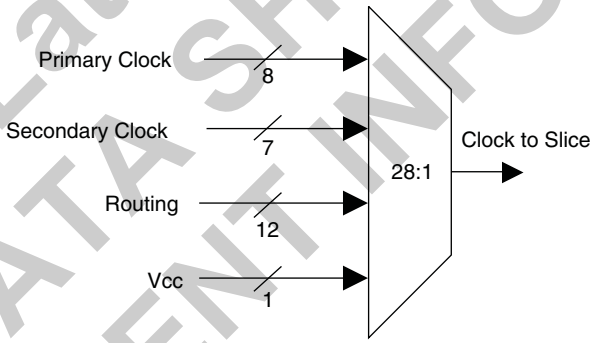


Figure 2-18. Slice0 through Slice2 Control Selection

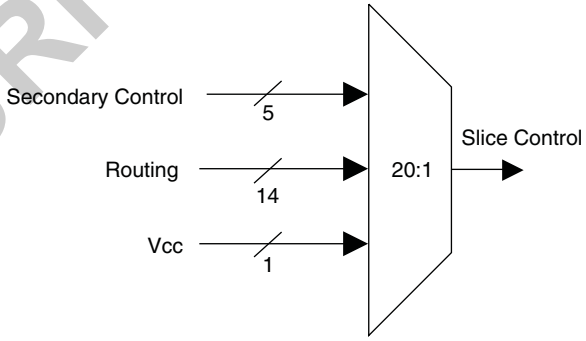


Figure 2-20. Sources of Edge Clock (Left and Right Edges)

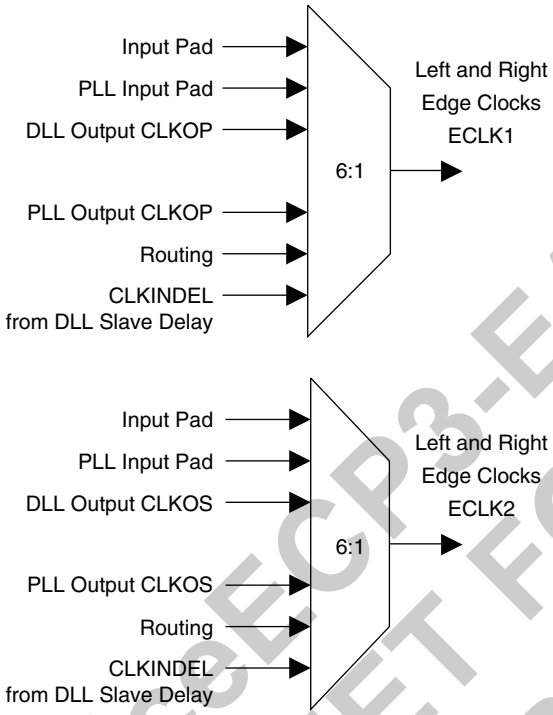
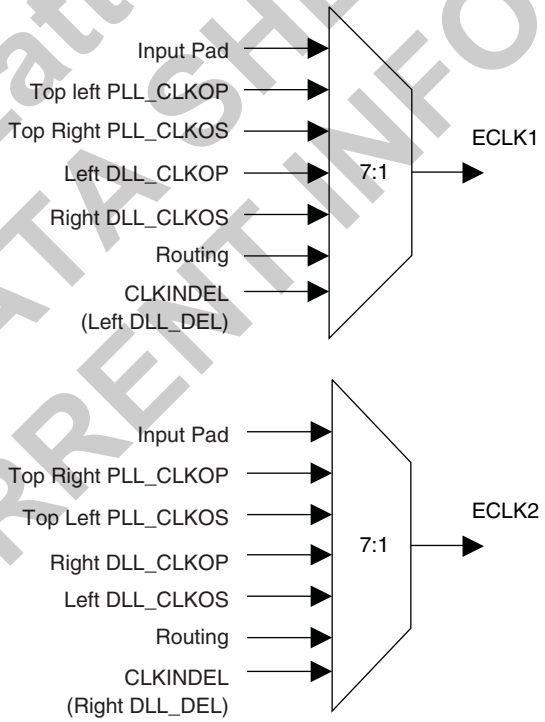


Figure 2-21. Sources of Edge Clock (Top Edge)



The edge clocks have low injection delay and low skew. They are used to clock the I/O registers and thus are ideal for creating I/O interfaces with a single clock signal and a wide data bus. They are also used for DDR Memory or Generic DDR interfaces.

MULTADDSUBSUM DSP Element

In this case, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB of Slice 0. Additionally, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB of Slice 1. The results of both addition/subtractions are added by the second ALU following the slice cascade path. The user can enable the input, output and pipeline registers. Figure 2-30 and Figure 2-31 show the MULTADDSUBSUM sysDSP element.

Figure 2-30. MULTADDSUBSUM Slice 0

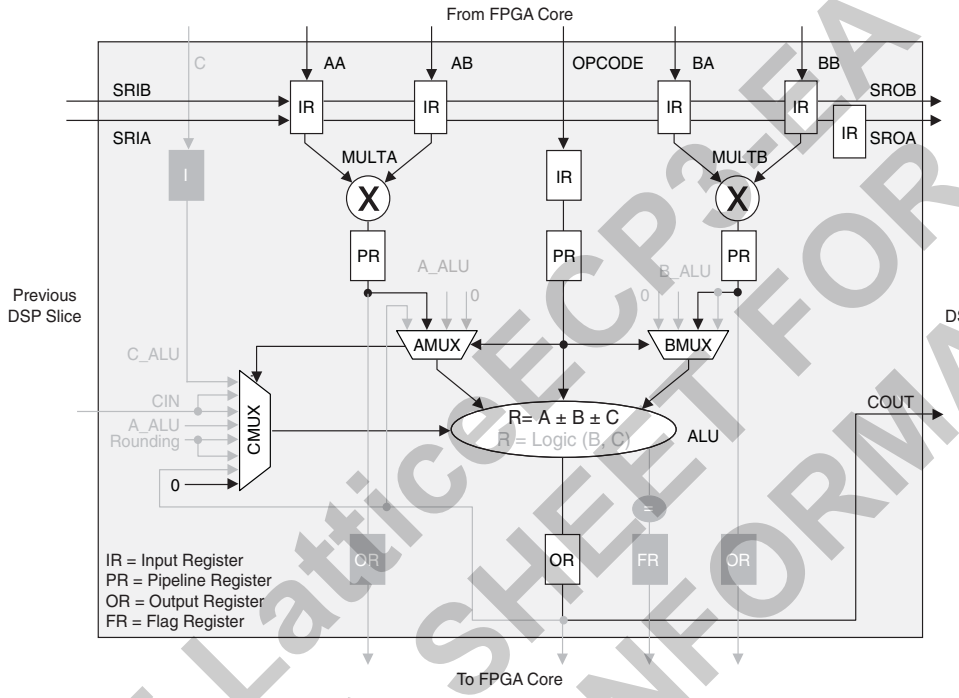
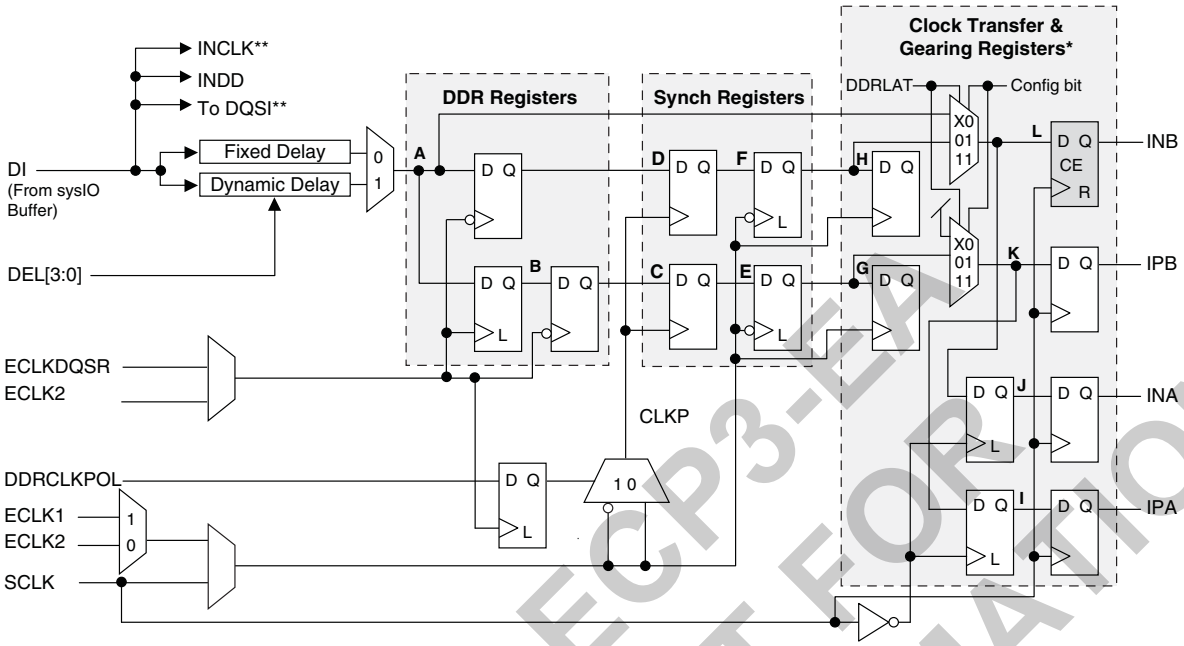


Figure 2-33. ECP3-70/95 (E or EA) Input Register Block for Left, Right and Top Edges



* Only on the left and right sides.
** Selected PIO.
Note: Simplified diagram does not show CE/SET/REST details.

Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysI/O buffers. The blocks on the left and right PIOs contain registers for SDR and full DDR operation. The topside PIO block is the same as the left and right sides except it does not support ODDRX2 gearing of output logic. ODDRX2 gearing is used in DDR3 memory interfaces.The PIO blocks on the bottom contain the SDR registers and generic DDR interface without gearing.

Figure 2-34 shows the Output Register Block for PIOs on the left and right edges.

In SDR mode, OPOSA feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a Dtype or latch. In DDR mode, two of the inputs are fed into registers on the positive edge of the clock. At the next clock cycle, one of the registered outputs is also latched.

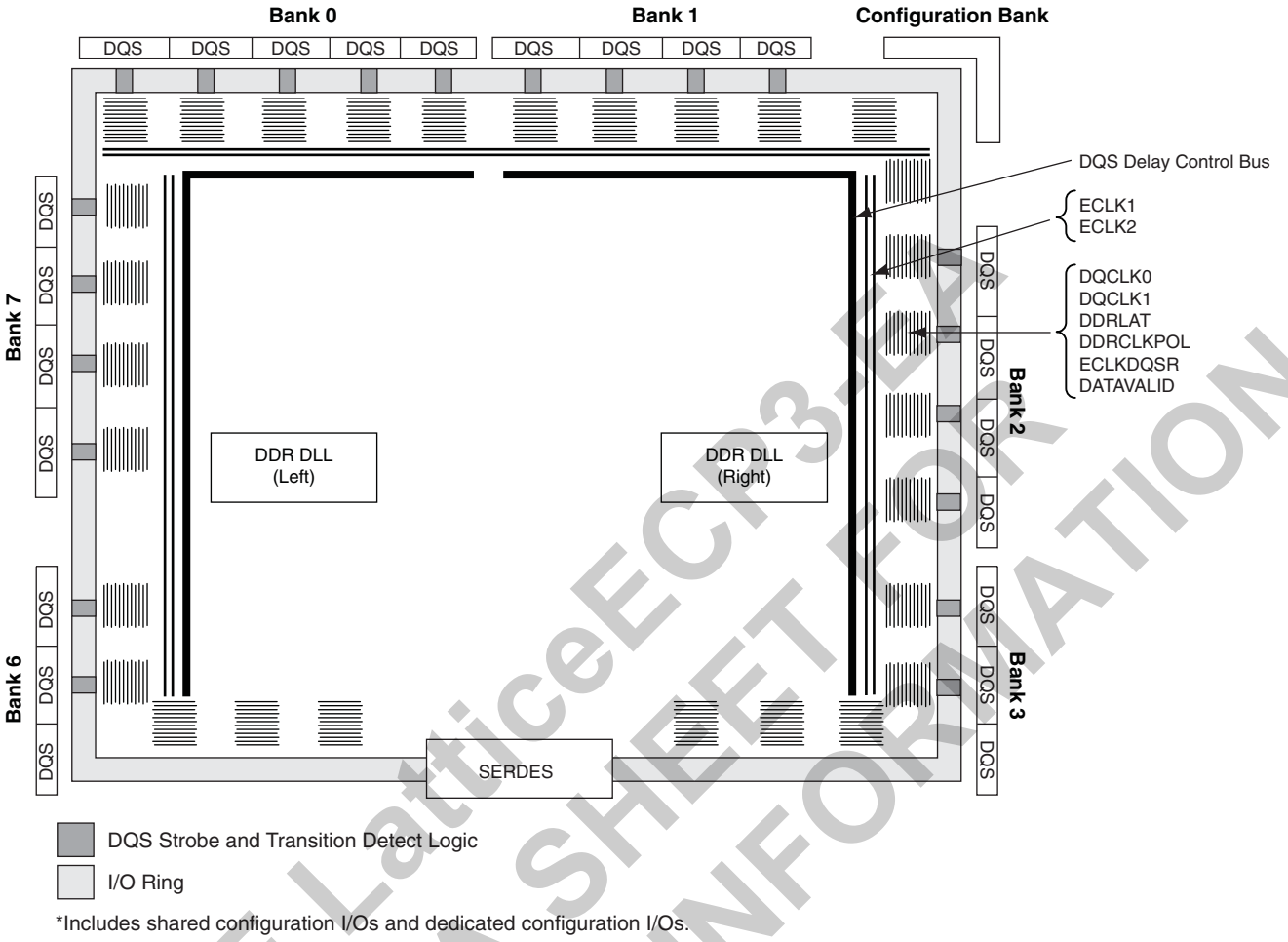
A multiplexer running off the same clock is used to switch the mux between the 11 and 01 inputs that will then feed the output.

A gearbox function can be implemented in the output register block that takes four data streams: OPOSA, ONEGA, OPOSB and ONEGB. All four data inputs are registered on the positive edge of the system clock and two of them are also latched. The data is then output at a high rate using a multiplexer that runs off the DQCLK0 and DQCLK1 clocks. DQCLK0 and DQCLK1 are used in this case to transfer data from the system clock to the edge clock domain. These signals are generated in the DQS Write Control Logic block. See Figure 2-37 for an overview of the DQS write control logic.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.

Further discussion on using the DQS strobe in this module is discussed in the DDR Memory section of this data sheet.

Figure 2-36. Edge Clock, DLL Calibration and DQS Local Bus Distribution



2. **Left and Right (Banks 2, 3, 6 and 7) sysI/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)**
   The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

   In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing on these sides as the clamp is always present.

   LVDS, RSDS, PPLVDS and Mini-LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

3. **Configuration Bank sysI/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)**
   The sysI/O buffers in the Configuration Bank consist of single-ended output drivers and single-ended input buffers (both ratioed and referenced). The referenced input buffer can also be configured as a differential input.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Programmable PCI clamps are only available on top banks (PCI clamps are used primarily on inputs and bidirectional pads to reduce ringing on the receiving end) can also be used on inputs.

Typical sysI/O I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC}, V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LatticeECP3 devices, see the list of technical documentation at the end of this data sheet.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported sysI/O Standards

The LatticeECP3 sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2V, 1.5V, 1.8V, 2.5V and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, MLVDS, RSDS, Mini-LVDS, PPLVDS (point-to-point LVDS), TRLVDS (Transition Reduced LVDS), differential SSTL and differential HSTL. Tables 2-13 and 2-14 show the I/O standards (together with their supply and reference voltages) supported by LatticeECP3 devices. For further information on utilizing the sysI/O buffer to support a variety of standards please see TN1177, LatticeECP3 sysIO Usage Guide.

Table 2-14. Available SERDES Quads per LatticeECP3 Devices

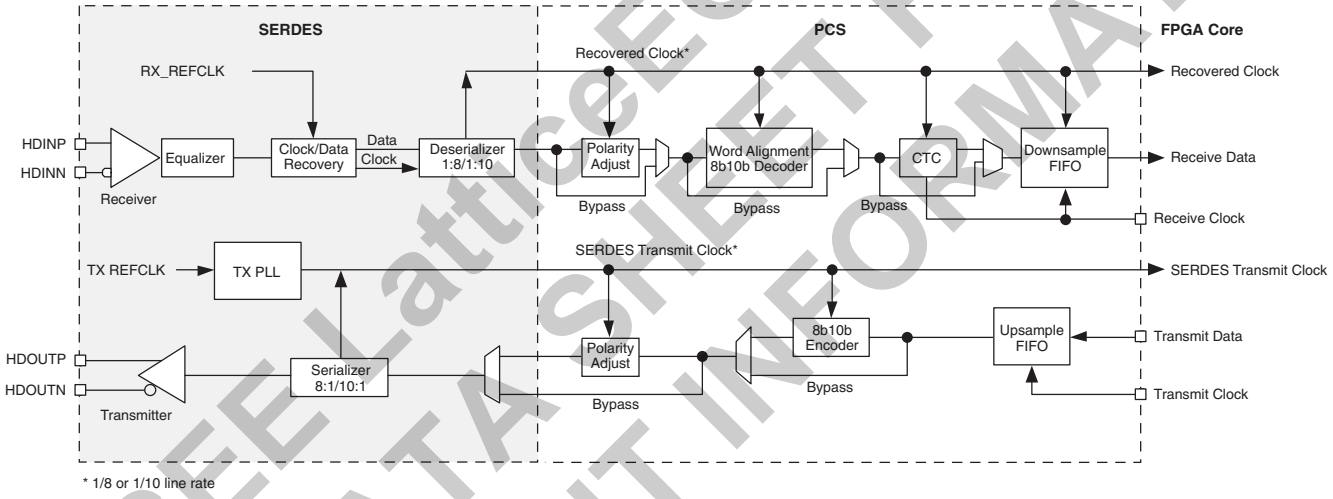
Package	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
256 ftBGA	1	1	—	—	—
484 ftBGA	1	1	1	1	
672 ftBGA	—	1	2	2	2
1156 ftBGA	—	—	3	3	4

SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2-41 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCOB and VCCIB).

Figure 2-41. Simplified Channel Block Diagram for SERDES/PCS Block



PCS

As shown in Figure 2-41, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

SCI (SERDES Client Interface) Bus

The SERDES Client Interface (SCI) is an IP interface that allows the SERDES/PCS Quad block to be controlled by registers rather than the configuration memory cells. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

SERDES Power Supply Requirements[1, 2, 3]

Over Recommended Operating Conditions

Symbol	Description	Typ.	Max.	Units
Standby (Power Down)				
I_{CCA-SB}	V_{CCA} current (per channel)	3	5	mA
$I_{CCIB-SB}$	Input buffer current (per channel)	—	—	mA
$I_{CCOB-SB}$	Output buffer current (per channel)	—	—	mA
Operating (Data Rate = 3.2 Gbps)				
I_{CCA-OP}	V_{CCA} current (per channel)	68	77	mA
$I_{CCIB-OP}$	Input buffer current (per channel)	5	7	mA
$I_{CCOB-OP}$	Output buffer current (per channel)	19	25	mA
Operating (Data Rate = 2.5 Gbps)				
I_{CCA-OP}	V_{CCA} current (per channel)	66	76	mA
$I_{CCIB-OP}$	Input buffer current (per channel)	4	5	mA
$I_{CCOB-OP}$	Output buffer current (per channel)	15	18	mA
Operating (Data Rate = 1.25 Gbps)				
I_{CCA-OP}	V_{CCA} current (per channel)	62	72	mA
$I_{CCIB-OP}$	Input buffer current (per channel)	4	5	mA
$I_{CCOB-OP}$	Output buffer current (per channel)	15	18	mA
Operating (Data Rate = 250 Mbps)				
I_{CCA-OP}	V_{CCA} current (per channel)	55	65	mA
$I_{CCIB-OP}$	Input buffer current (per channel)	4	5	mA
$I_{CCOB-OP}$	Output buffer current (per channel)	14	17	mA

1. Equalization enabled, pre-emphasis disabled.
2. One quarter of the total quad power (includes contribution from common circuits, all channels in the quad operating, pre-emphasis disabled, equalization enabled).
3. Pre-emphasis adds 20mA to ICCA-OP data.

Register-to-Register Performance[1, 2]

Function	-8 Timing	Units
18x18 Multiply/Accumulate (Input & Output Registers)	200	MHz
18x18 Multiply-Add/Sub (All Registers)	400	MHz
DSP IP Functions		
16-Tap Fully-Parallel FIR Filter		MHz
1024-pt, Radix 4, Decimation in Frequency FFT		MHz
8X8 Matrix Multiplication		MHz

1. These timing numbers were generated using ispLEVER tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the ispLEVER software.

Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the ispLEVER design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The ispLEVER design tool can provide logic timing numbers at a particular temperature and voltage.

PCI Express Electrical and Timing Characteristics

AC and DC Characteristics

Over Recommended Operating Conditions

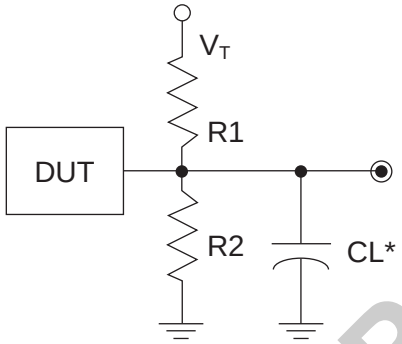
Symbol	Description	Test Conditions	Min	Typ	Max	Units
Transmit[1]						
UI	Unit interval		399.88	400	400.12	ps
$V_{TX-DIFF\_P-P}$	Differential peak-to-peak output voltage		0.8	1.0	1.2	V
$V_{TX-DE-RATIO}$	De-emphasis differential output voltage ratio		-3	-3.5	-4	dB
$V_{TX-CM-AC\_P}$	RMS AC peak common-mode output voltage		—	—	20	mV
$V_{TX-RCV-DETECT}$	Amount of voltage change allowed during receiver detection		—	—	600	mV
$V_{TX-DC-CM}$	Tx DC common mode voltage		0	—	V_{CCOB} + 5%	V
$I_{TX-SHORT}$	Output short circuit current	V_{TX-D+}=0.0V V_{TX-D-}=0.0V	—	—	90	mA
$Z_{TX-DIFF-DC}$	Differential output impedance		80	100	120	Ohms
$RL_{TX-DIFF}$	Differential return loss		10	—	—	dB
RL_{TX-CM}	Common mode return loss		6.0	—	—	dB
$T_{TX-RISE}$	Tx output rise time	20 to 80%	0.125	—	—	UI
$T_{TX-FALL}$	Tx output fall time	20 to 80%	0.125	—	—	UI
$L_{TX-SKEW}$	Lane-to-lane static output skew for all lanes in port/link		—	—	1.3	ns
T_{TX-EYE}	Transmitter eye width		0.75	—	—	UI
$T_{TX-EYE-MEDIAN-TO-MAX-JITTER}$	Maximum time between jitter median and maximum deviation from median		—	—	0.125	UI
Receive[1, 2]						
UI	Unit Interval		399.88	400	400.12	ps
$V_{RX-DIFF\_P-P}$	Differential peak-to-peak input voltage		0.34[3]	—	1.2	V
$V_{RX-IDLE-DET-DIFF\_P-P}$	Idle detect threshold voltage		65	—	340[3]	mV
$V_{RX-CM-AC\_P}$	Receiver common mode voltage for AC coupling		—	—	150	mV
$Z_{RX-DIFF-DC}$	DC differential input impedance		80	100	120	Ohms
Z_{RX-DC}	DC input impedance		40	50	60	Ohms
$Z_{RX-HIGH-IMP-DC}$	Power-down DC input impedance		200K	—	—	Ohms
$RL_{RX-DIFF}$	Differential return loss		10	—	—	dB
RL_{RX-CM}	Common mode return loss		6.0	—	—	dB
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Maximum time required for receiver to recognize and signal an unexpected idle on link		—	—	—	ms

1. Values are measured at 2.5 Gbps.
2. Measured with external AC-coupling on the receiver.
3.Not in compliance with PCI Express 1.1 standard.

Switching Test Conditions

Figure 3-26 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-23.

Figure 3-26. Output Test Load, LVTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-23. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	R_2	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L -> H, H -> L)	∞	∞	0pF	LVCMOS 3.3 = 1.5V	—
				LVCMOS 2.5 = V_{CCIO}/2	—
				LVCMOS 1.8 = V_{CCIO}/2	—
				LVCMOS 1.5 = V_{CCIO}/2	—
				LVCMOS 1.2 = V_{CCIO}/2	—
LVCMOS 2.5 I/O (Z -> H)	∞	1MΩ	0pF	V_{CCIO}/2	—
LVCMOS 2.5 I/O (Z -> L)	1MΩ	∞	0pF	V_{CCIO}/2	V_{CCIO}
LVCMOS 2.5 I/O (H -> Z)	∞	100	0pF	V_{OH} - 0.10	—
LVCMOS 2.5 I/O (L -> Z)	100	∞	0pF	V_{OL} + 0.10	V_{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Point-to-Point LVDS (PPLVDS)

Over Recommended Operating Conditions

Description	Min.	Typ.	Max.	Units
Output driver supply (+/- 5%)	3.14	3.3	3.47	V
	2.25	2.5	2.75	V
Input differential voltage	100		400	mV
Input common mode voltage	0.2		2.3	V
Output differential voltage	130		400	mV
Output common mode voltage	0.5	0.8	1.4	V

RSDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Typ.	Max.	Units
V_{OD}	Output voltage, differential, R_T = 100 ohms	100	200	600	mV
V_{OS}	Output voltage, common mode	0.5	1.2	1.5	V
I_{RSDS}	Differential driver output current	1	2	6	mA
V_{THD}	Input voltage differential	100	—	—	mV
V_{CM}	Input common mode voltage	0.3	—	1.5	V
T_R, T_F	Output rise and fall times, 20% to 80%	—	500	—	ps
T_{ODUTY}	Output clock duty cycle	35	50	65	%

Note: Data is for 2mA drive. Other differential driver current options are available.

Pin Information Summary (Cont.)

Pin Information Summary		ECP3-17EA		ECP3-35EA		
Pin Type		256 ftBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA
Emulated Differential I/O per Bank	Bank 0	13	18	13	21	24
	Bank 1	7	12	7	18	18
	Bank 2	2	4	1	8	8
	Bank 3	4	13	5	20	19
	Bank 6	5	13	6	22	20
	Bank 7	6	10	6	11	13
	Bank 8	12	12	12	12	12
Highspeed Differential I/O per Bank	Bank 0	0	0	0	0	0
	Bank 1	0	0	0	0	0
	Bank 2	2	3	3	6	6
	Bank 3	5	9	4	9	12
	Bank 6	5	9	4	11	12
	Bank 7	5	8	5	9	10
	Bank 8	0	0	0	0	0
Total Single Ended/ Total Differential I/O per Bank	Bank 0	26/13	36/18	26/13	42/21	48/24
	Bank 1	14/7	24/12	14/7	36/18	36/18
	Bank 2	8/4	14/7	8/4	28/14	28/14
	Bank 3	18/9	44/22	18/9	58/29	63/31
	Bank 6	20/10	44/22	20/10	67/33	65/32
	Bank 7	23/11	36/18	23/11	40/20	46/23
	Bank 8	24/12	24/12	24/12	24/12	24/12
DDR Groups Bonded per Bank	Bank 0	2	3	2	3	4
	Bank 1	1	2	1	3	3
	Bank 2	0	1	0	2	2
	Bank 3	1	3	1	3	4
	Bank 6	1	3	1	4	4
	Bank 7	1	2	1	3	3
	Configuration Bank 8	0	0	0	0	0
SERDES Quads		1	1	1	1	1

1. These pins must remain floating on the board.

Pin Information Summary (Cont.)

Pin Information Summary		ECP3-70E			ECP3-70EA		
Pin Type		484 fpBGA	672 fpBGA	1156 fpBGA	484 fpBGA	672 fpBGA	1156 fpBGA
Emulated Differential I/O per Bank	Bank 0	21	30	43	21	30	43
	Bank 1	18	24	39	18	24	39
	Bank 2	10	15	16	8	12	13
	Bank 3	23	27	39	20	23	33
	Bank 6	26	30	39	22	25	33
	Bank 7	14	20	22	11	16	18
	Bank 8	12	12	12	12	12	12
High-Speed Differential I/O per Bank	Bank 0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0
	Bank 2	4	6	6	6	9	9
	Bank 3	6	8	10	9	12	16
	Bank 6	7	9	10	11	14	16
	Bank 7	6	8	9	9	12	13
	Bank 8	0	0	0	0	0	0
Total Single-Ended/ Total Differential I/O per Bank	Bank 0	42/21	60/30	86/43	42/21	60/30	86/43
	Bank 1	36/18	48/24	78/39	36/18	48/24	78/39
	Bank 2	28/14	42/21	44/22	28/14	42/21	44/22
	Bank 3	58/29	71/35	98/49	58/29	71/35	98/49
	Bank 6	67/33	79/38	98/49	67/33	78/39	98/49
	Bank 7	40/20	56/28	62/31	40/20	56/28	62/31
	Bank 8	24/12	24/12	24/12	24/12	24/12	24/12
DDR Groups Bonded per Bank	Bank 0	3	5	7	3	5	7
	Bank 1	3	4	7	3	4	7
	Bank 2	2	3	3	2	3	3
	Bank 3	3	4	5	3	4	5
	Bank 6	4	4	5	4	4	5
	Bank 7	3	4	4	3	4	4
	Configuration Bank 8	0	0	0	0	0	0
SERDES Quads		1	2	3	1	2	3

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-70E-6FN484I[1]	1.2V	-6	Lead-Free fpBGA	484	IND	67
LFE3-70E-7FN484I[1]	1.2V	-7	Lead-Free fpBGA	484	IND	67
LFE3-70E-8FN484I[1]	1.2V	-8	Lead-Free fpBGA	484	IND	67
LFE3-70E-6FN672I[1]	1.2V	-6	Lead-Free fpBGA	672	IND	67
LFE3-70E-7FN672I[1]	1.2V	-7	Lead-Free fpBGA	672	IND	67
LFE3-70E-8FN672I[1]	1.2V	-8	Lead-Free fpBGA	672	IND	67
LFE3-70E-6FN1156I[1]	1.2V	-6	Lead-Free fpBGA	1156	IND	67
LFE3-70E-7FN1156I[1]	1.2V	-7	Lead-Free fpBGA	1156	IND	67
LFE3-70E-8FN1156I[1]	1.2V	-8	Lead-Free fpBGA	1156	IND	67

1.This device has associated errata. View www.latticesemi.com/documents/ds1021.zip for a description of the errata.

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-95EA-6FN484I	1.2V	-6	Lead-Free fpBGA	484	IND	92
LFE3-95EA-7FN484I	1.2V	-7	Lead-Free fpBGA	484	IND	92
LFE3-95EA-8FN484I	1.2V	-8	Lead-Free fpBGA	484	IND	92
LFE3-95EA-6FN672I	1.2V	-6	Lead-Free fpBGA	672	IND	92
LFE3-95EA-7FN672I	1.2V	-7	Lead-Free fpBGA	672	IND	92
LFE3-95EA-8FN672I	1.2V	-8	Lead-Free fpBGA	672	IND	92
LFE3-95EA-6FN1156I	1.2V	-6	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-7FN1156I	1.2V	-7	Lead-Free fpBGA	1156	IND	92
LFE3-95EA-8FN1156I	1.2V	-8	Lead-Free fpBGA	1156	IND	92

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-95E-6FN484I[1]	1.2V	-6	Lead-Free fpBGA	484	IND	92
LFE3-95E-7FN484I[1]	1.2V	-7	Lead-Free fpBGA	484	IND	92
LFE3-95E-8FN484I[1]	1.2V	-8	Lead-Free fpBGA	484	IND	92
LFE3-95E-6FN672I[1]	1.2V	-6	Lead-Free fpBGA	672	IND	92
LFE3-95E-7FN672I[1]	1.2V	-7	Lead-Free fpBGA	672	IND	92
LFE3-95E-8FN672I[1]	1.2V	-8	Lead-Free fpBGA	672	IND	92
LFE3-95E-6FN1156I[1]	1.2V	-6	Lead-Free fpBGA	1156	IND	92
LFE3-95E-7FN1156I[1]	1.2V	-7	Lead-Free fpBGA	1156	IND	92
LFE3-95E-8FN1156I[1]	1.2V	-8	Lead-Free fpBGA	1156	IND	92

1.This device has associated errata. View www.latticesemi.com/documents/ds1021.zip for a description of the errata.