Understanding Embedded - FPGAs (Field Programmable Gate Array)

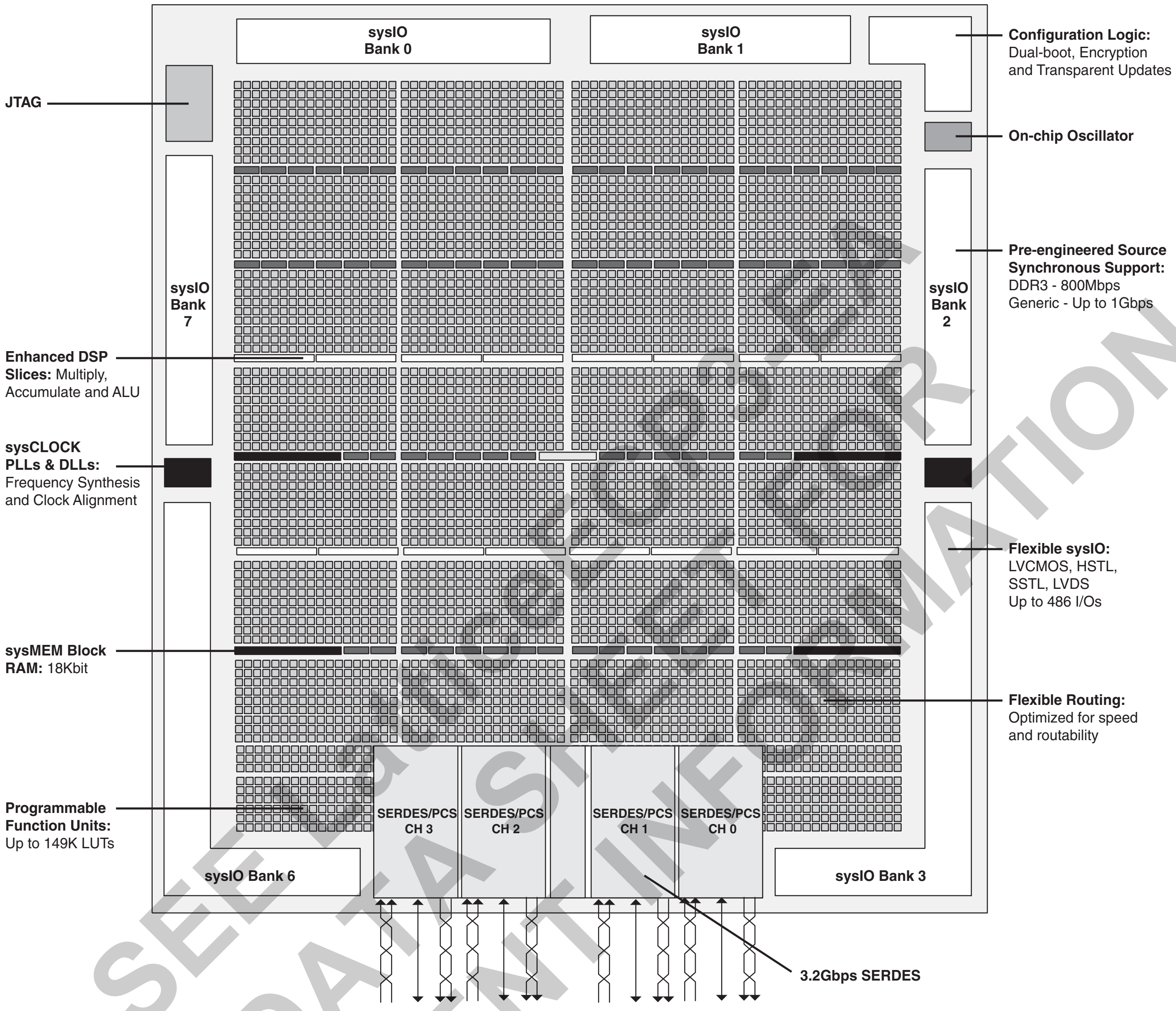
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	11500
Number of Logic Elements/Cells	92000
Total RAM Bits	4526080
Number of I/O	295
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95e-6fn484c

Figure 2-1. Simplified Block Diagram, LatticeECP3-35 Device (Top Level)



Note: There is no Bank 4 or Bank 5 in LatticeECP3 devices.

PFU Blocks

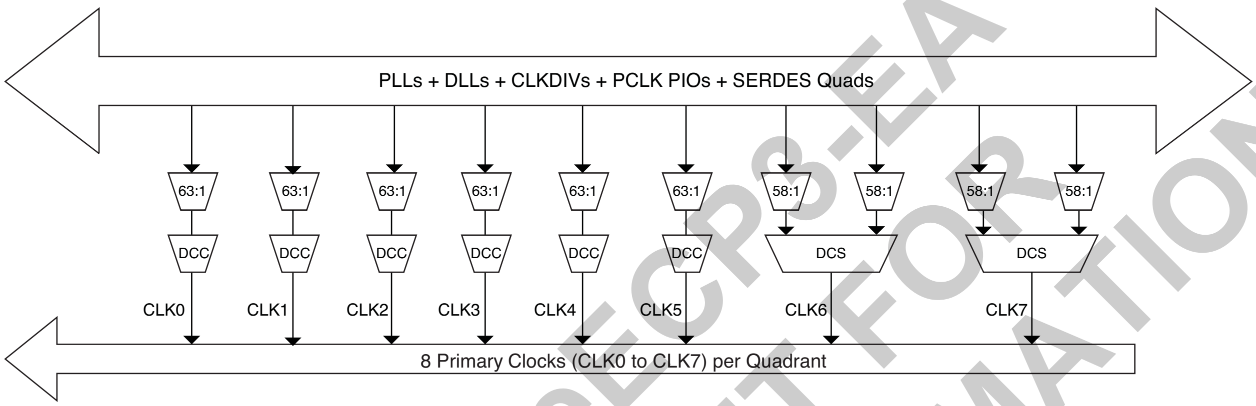
The core of the LatticeECP3 device consists of PFU blocks, which are provided in two forms, the PFU and PFF. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices numbered 0-3 as shown in Figure 2-2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

Primary Clock Routing

The purpose of the primary clock routing is to distribute primary clock sources to the destination quadrants of the device. A global primary clock is a primary clock that is distributed to all quadrants. The clock routing structure in LatticeECP3 devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 2-12 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally.

Figure 2-12. Per Quadrant Primary Clock Selection



Dynamic Clock Control (DCC)

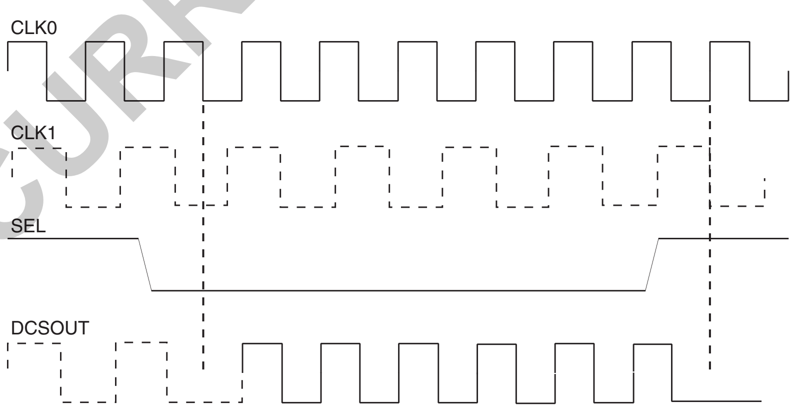
The DCC (Quadrant Clock Enable/Disable) feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, all the logic fed by that clock does not toggle, reducing the overall power consumption of the device.

Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved regardless of when the select signal is toggled. There are two DCS blocks per quadrant; in total, there are eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 2-12).

Figure 2-13 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, please see the list of technical documentation at the end of this data sheet.

Figure 2-13. DCS Waveforms

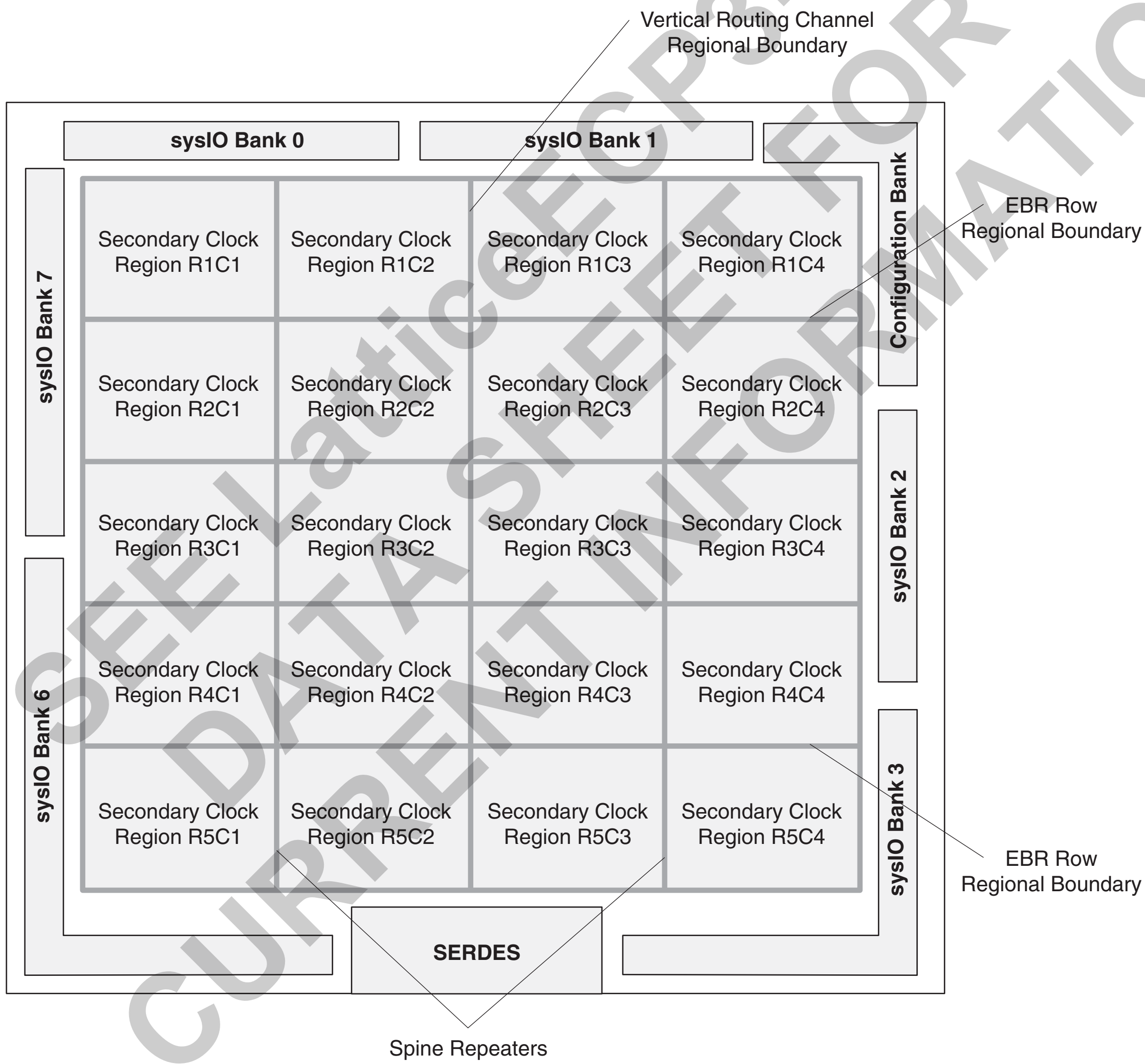


secondary clock resources per region (SC0 to SC7). The same secondary clock routing can be used for control signals.

Table 2-6. Secondary Clock Regions

Device	Number of Secondary Clock Regions
ECP3-17	16
ECP3-35	16
ECP3-70	20
ECP3-95	20
ECP3-150	36

Figure 2-15. LatticeECP3-70 and LatticeECP3-95 Secondary Clock Regions



Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

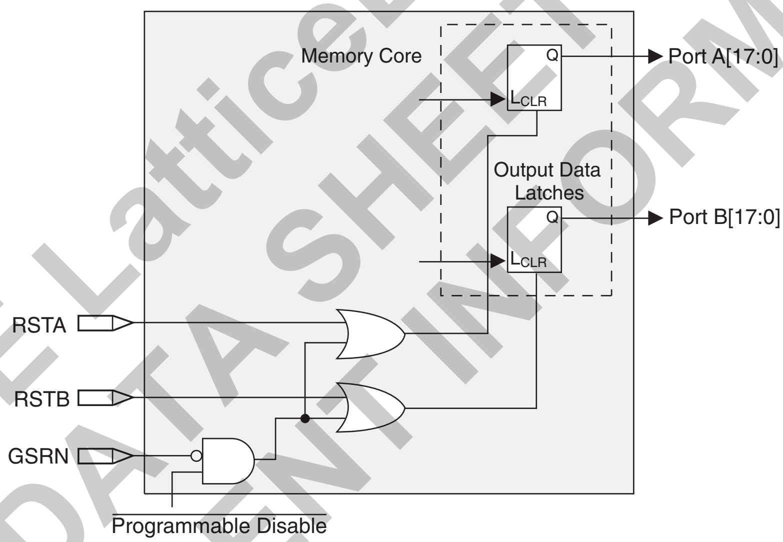
EBR memory supports the following forms of write behavior for single port or dual port operation:

1. **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write (EA devices only)** – When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2-22.

Figure 2-22. Memory Core Reset



For further information on the sysMEM EBR block, please see the list of technical documentation at the end of this data sheet.

sysDSP™ Slice

The LatticeECP3 family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

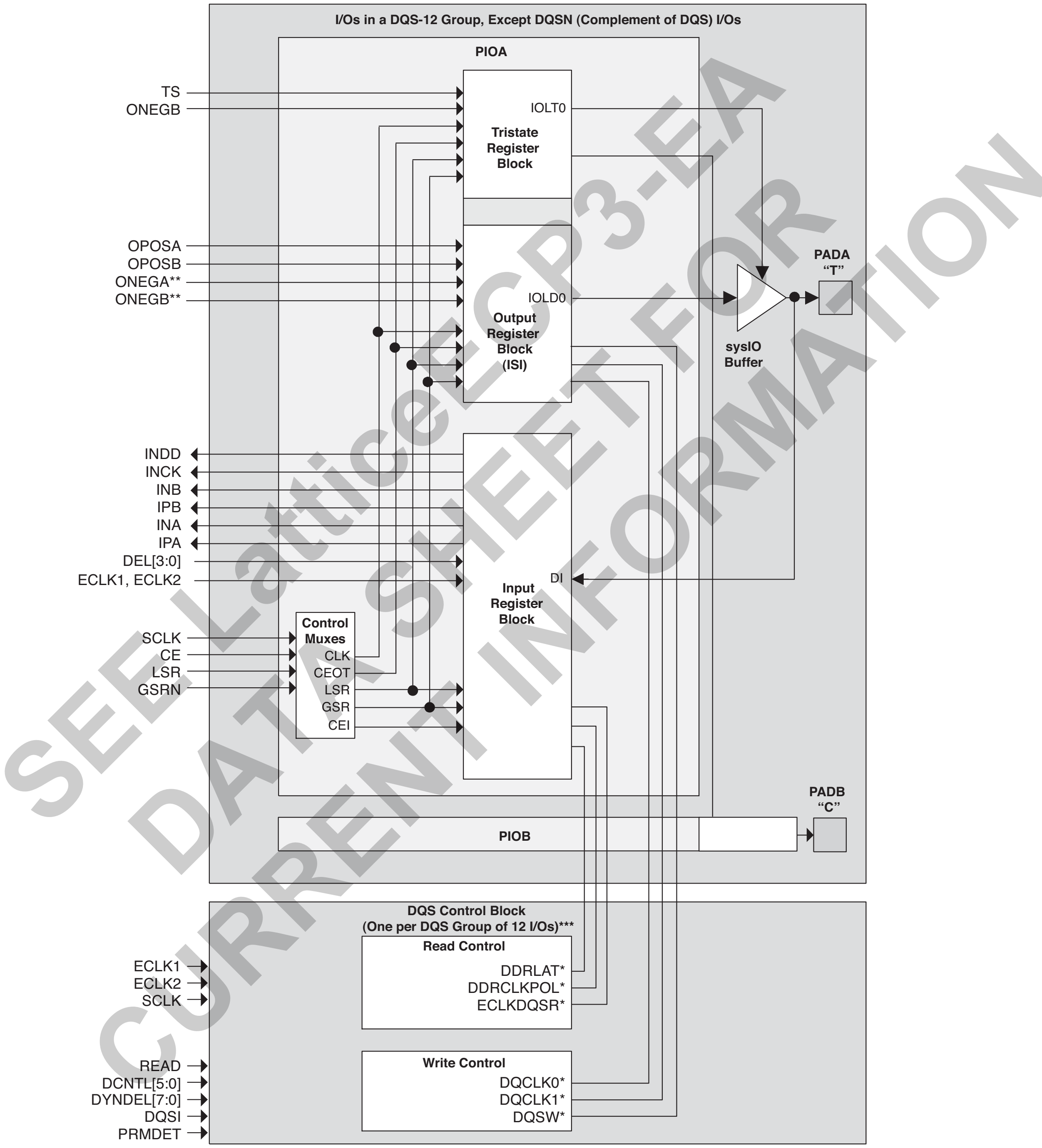
sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP3, on the other hand, has many DSP slices that support different data widths.

Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O buffers as shown in Figure 2-32. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysI/O buffer and receives input from the buffer. Table 2-11 provides the PIO signal list.

Figure 2-32. PIC Diagram



* Signals are available on left/right/top edges only.
** Signals are available on the left and right sides only
*** Selected PIO.

Table 2-14. Available SERDES Quads per LatticeECP3 Devices

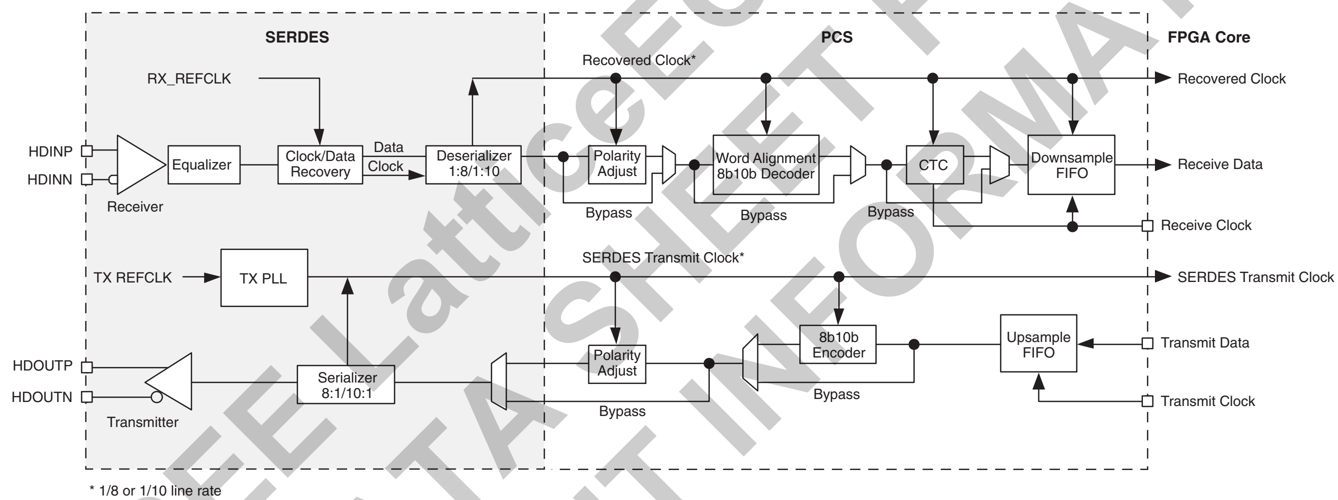
Package	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
256 ftBGA	1	1	—	—	—
484 ftBGA	1	1	1	1	
672 ftBGA	—	1	2	2	2
1156 ftBGA	—	—	3	3	4

SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2-41 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCOB and VCCIB).

Figure 2-41. Simplified Channel Block Diagram for SERDES/PCS Block



PCS

As shown in Figure 2-41, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

SCI (SERDES Client Interface) Bus

The SERDES Client Interface (SCI) is an IP interface that allows the SERDES/PCS Quad block to be controlled by registers rather than the configuration memory cells. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

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Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC} . . . . -0.5 to 1.32V

Supply Voltage V_{CCAUX} . . . . -0.5 to 3.75V

Supply Voltage V_{CCJ} . . . . -0.5 to 3.75V

Output Supply Voltage V_{CCIO} . . . . -0.5 to 3.75V

Input or I/O Tristate Voltage Applied[4]. . . . . . -0.5 to 3.75V

Storage Temperature (Ambient) . . . . -65 to 150°C

Junction Temperature (Tj) . . . . +125°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to (V_{IHMAX} + 2) volts is permitted for a duration of <20ns.

Recommended Operating Conditions[1]

Symbol	Parameter	Min.	Max.	Units
V_{CC}[2]	Core Supply Voltage	1.14	1.26	V
V_{CCAUX}[2, 4]	Auxiliary Supply Voltage, Terminating Resistor Switching Power Supply (SERDES)	3.135	3.465	V
V_{CCPLL}	PLL Supply Voltage	3.135	3.465	V
V_{CCIO}[2, 3]	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ}[2]	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
V_{REF1} and V_{REF2}	Input Reference Voltage	0.5	1.7	V
V_{TT}[5]	Termination Voltage	0.5	1.3125	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature, Industrial Operation	-40	100	°C
SERDES External Power Supply[6]				
V_{CCIB}	Input Buffer Power Supply (1.2V)	1.14	1.26	V
	Input Buffer Power Supply (1.5V)	1.425	1.575	V
V_{CCOB}	Output Buffer Power Supply (1.2V)	1.14	1.26	V
	Output Buffer Power Supply (1.5V)	1.425	1.575	V
V_{CCA}	Transmit, Receive, PLL and Reference Clock Buffer Power Supply	1.14	1.26	V

1. For correct operation, all supplies except V_{REF} and V_{TT} must be held in their valid operation range. This is true independent of feature usage.
2. If V_{CCIO} or V_{CCJ} is set to 1.2V, they must be connected to the same power supply as $V_{CC.}$ If V_{CCIO} or V_{CCJ} is set to 3.3V, they must be connected to the same power supply as V_{CCAUX}.
3. See recommended voltages by I/O standard in subsequent table.
4. V_{CCAUX} ramp rate must not exceed 30mV/µs during power-up when transitioning between 0V and 3.3V.
5. If not used, V_{TT} should be left floating.
6. See TN1176, LatticeECP3 SERDES/PCS Usage Guide for information on board considerations for SERDES power supplies.

sysI/O Differential Electrical Characteristics

LVDS25

Over Recommended Operating Conditions

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage		0	—	2.4	V
V_{CM}	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	+/-100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	+/-10	µA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.9V	1.03	—	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low		—	—	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100 Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50	mV
I_{SAB}	Output Short Circuit Current	V_{OD} = 0V Driver Outputs Shorted to Each Other	—	—	12	mA

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

Typical Building Block Function Performance

Pin-to-Pin Performance (LVCMOS25 12mA Drive)[1, 2]

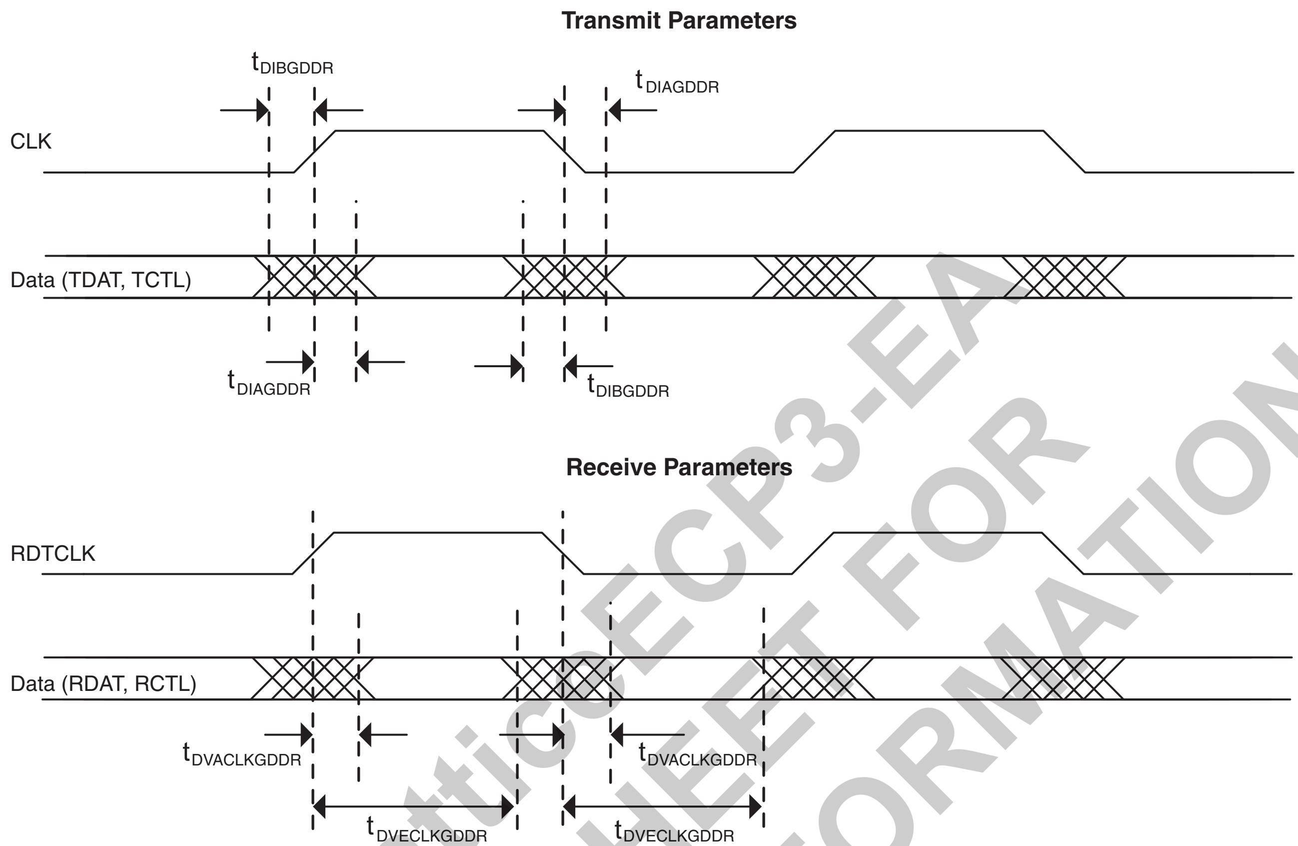
Function	-8 Timing	Units
Basic Functions		
16-bit Decoder	4.7	ns
32-bit Decoder	4.7	ns
64-bit Decoder	5.7	ns
4:1 MUX	4.1	ns
8:1 MUX	4.3	ns
16:1 MUX	4.7	ns
32:1 MUX	4.8	ns

1. These functions were generated using the ispLEVER design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the ispLEVER software.

Register-to-Register Performance[1, 2]

Function	-8 Timing	Units
Basic Functions		
16-bit Decoder	500	MHz
32-bit Decoder	500	MHz
64-bit Decoder	475	MHz
4:1 MUX	500	MHz
8:1 MUX	500	MHz
16:1 MUX	500	MHz
32:1 MUX	445	MHz
8-bit adder	500	MHz
16-bit adder	500	MHz
64-bit adder	305	MHz
16-bit counter	500	MHz
32-bit counter	460	MHz
64-bit counter	320	MHz
64-bit accumulator	315	MHz
Embedded Memory Functions		
512x36 Single Port RAM, EBR Output Registers	340	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	340	MHz
1024x18 True-Dual Port RAM (Read-Before-Write, EBR Output Registers; EA devices only)	130	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	245	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (One PFU)	500	MHz
32x4 Pseudo-Dual Port RAM	500	MHz
64x8 Pseudo-Dual Port RAM	380	MHz
DSP Function		
18x18 Multiplier (All Registers)	400	MHz
9x9 Multiplier (All Registers)	400	MHz
36x36 Multiply (All Registers)	245	MHz

Figure 3-6. Generic DDR/DDR2 (With Clock and Data Edges Aligned)



LatticeECP3 Family Timing Adders[1, 2, 3, 4, 5] (Continued)

Over Recommended Commercial Operating Conditions

Buffer Type	Description	-8	-7	-6	Units
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, fast slew rate	0.09	0.10	0.10	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, fast slew rate	0.01	0.01	0.00	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, fast slew rate	0.08	0.08	0.08	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, fast slew rate	-0.02	-0.02	-0.02	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, slow slew rate	1.64	1.71	1.77	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, slow slew rate	1.39	1.45	1.51	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, slow slew rate	1.21	1.27	1.33	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, slow slew rate	1.43	1.49	1.55	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, slow slew rate	1.23	1.28	1.34	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, slow slew rate	1.66	1.70	1.74	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, slow slew rate	1.39	1.43	1.46	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, slow slew rate	1.20	1.24	1.28	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, slow slew rate	1.42	1.45	1.49	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, slow slew rate	1.22	1.26	1.29	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, slow slew rate	1.61	1.65	1.68	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, slow slew rate	1.32	1.36	1.39	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, slow slew rate	1.14	1.17	1.21	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, slow slew rate	1.35	1.38	1.42	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, slow slew rate	1.57	1.60	1.64	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, slow slew rate	0.01	0.01	0.00	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, slow slew rate	1.51	1.54	1.58	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, slow slew rate	-0.02	-0.02	-0.02	ns
PCI33	PCI, VCCIO = 3.0V	0.19	0.21	0.24	ns

1. Timing adders are characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. Not all I/O standards and drive strengths are supported for all banks. See the Architecture section of this data sheet for details.
5. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the ispLEVER software.

SERDES/PCS Block Latency

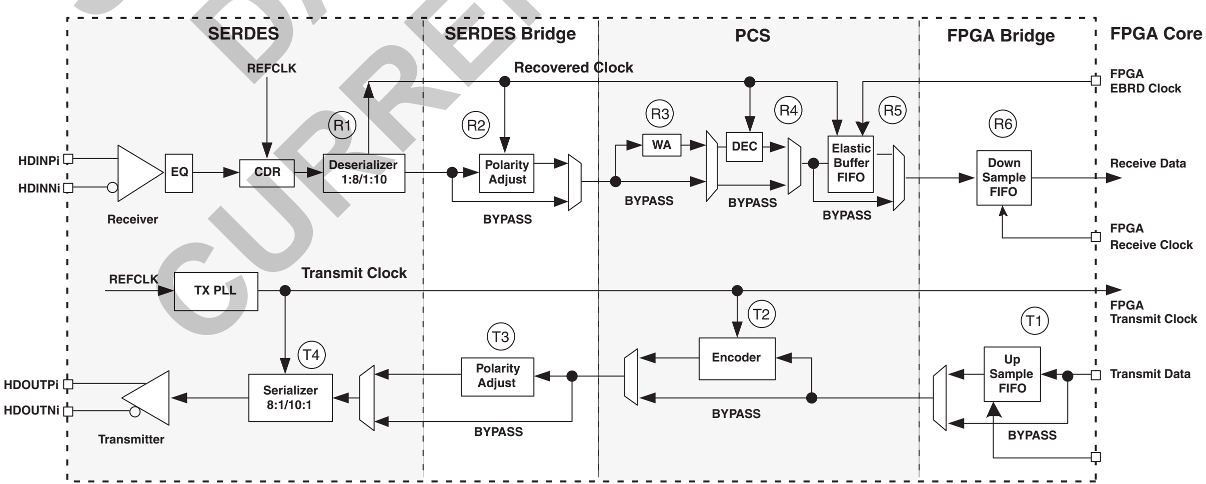
Table 3-8 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3-12 shows the location of each block.

Table 3-8. SERDES/PCS Latency Breakdown

Item	Description	Min.	Avg.	Max.	Fixed	Bypass	Units
Transmit Data Latency[1]							
T1	FPGA Bridge - Gearing disabled with different clocks	1	3	5	—	1	word clk
	FPGA Bridge - Gearing disabled with same clocks	—	—	—	3	1	word clk
	FPGA Bridge - Gearing enabled	1	3	5	—	—	word clk
T2	8b10b Encoder	—	—	—	2	1	word clk
T3	SERDES Bridge transmit	—	—	—	2	1	word clk
T4	Serializer: 8-bit mode	—	—	—	15 + Δ1	—	UI + ps
	Serializer: 10-bit mode	—	—	—	18 + Δ1	—	UI + ps
T5	Pre-emphasis ON	—	—	—	1 + Δ2	—	UI + ps
	Pre-emphasis OFF	—	—	—	0 + Δ3	—	UI + ps
Receive Data Latency[2]							
R1	Equalization ON	—	—	—	Δ1	—	UI + ps
	Equalization OFF	—	—	—	Δ2	—	UI + ps
R2	Deserializer: 8-bit mode	—	—	—	10 + Δ3	—	UI + ps
	Deserializer: 10-bit mode	—	—	—	12 + Δ3	—	UI + ps
R3	SERDES Bridge receive	—	—	—	2	—	word clk
R4	Word alignment	3.1	—	4	—	—	word clk
R5	8b10b decoder	—	—	—	1	—	word clk
R6	Clock Tolerance Compensation	7	15	23	1	1	word clk
R7	FPGA Bridge - Gearing disabled with different clocks	1	3	5	—	1	word clk
	FPGA Bridge - Gearing disabled with same clocks	—	—	—	3	1	word clk
	FPGA Bridge - Gearing enabled	1	3	5	—	—	word clk

1. Δ1 = -245ps, Δ2 = +88ps, Δ3 = +112ps.
2. Δ1 = +118ps, Δ2 = +132ps, Δ3 = +700ps.

Figure 3-12. Transmitter and Receiver Latency Block Diagram



SERDES High Speed Data Receiver

Table 3-9. Serial Input Data Specifications

Symbol	Description		Min.	Typ.	Max.	Units
$RX\text{-}CID_S$	Stream of nontransitions[1] (CID = Consecutive Identical Digits) @ 10^{-12} BER	3.125G	—	—	136	Bits
		2.5G	—	—	144	
		1.485G	—	—	160	
		622M	—	—	204	
		270M	—	—	228	
		155M	—	—	296	
$V_{RX\text{-}DIFF\text{-}S}$	Differential input sensitivity		150	—	1760	mV, p-p
$V_{RX\text{-}IN}$	Input levels		0	—	V_{CCA} +0.5[4]	V
$V_{RX\text{-}CM\text{-}DC}$	Input common mode range (DC coupled)		0.6	—	V_{CCA}	V
$V_{RX\text{-}CM\text{-}AC}$	Input common mode range (AC coupled)[3]		0.1	—	V_{CCA} +0.2	V
$T_{RX\text{-}RELOCK}$	SCDR re-lock time[2]		—	1000	—	Bits
$Z_{RX\text{-}TERM}$	Input termination 50/75 Ohm/High Z		-20%	50/75/HiZ	+20%	Ohms
$RL_{RX\text{-}RL}$	Return loss (without package)		10	—	—	dB

1. This is the number of bits allowed without a transition on the incoming data stream when using DC coupling.
2. This is the typical number of bit times to re-lock to a new phase or frequency within +/- 300 ppm, assuming 8b10b encoded data.
3. AC coupling is used to interface to LVPECL and LVDS. LVDS interfaces are found in laser drivers and Fibre Channel equipment. LVDS interfaces are generally found in 622 Mbps SERDES devices.
4. Up to 1.76V.

Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

Table 3-10. Receiver Total Jitter Tolerance Specification

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	2.5 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	1.25 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	622 Mbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p

Note: Values are measured with CJPAT, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.

HDMI (High-Definition Multimedia Interface) Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-22. Transmit and Receive[1, 2]

Symbol	Description	Spec. Compliance		Units
		Min. Spec.	Max. Spec.	
Transmit				
Intra-pair Skew		—	75	ps
Inter-pair Skew		—	800	ps
TMDS Differential Clock Jitter		—	0.25	UI
Receive				
R_T	Termination Resistance	40	60	Ohms
V_{ICM}	Input AC Common Mode Voltage (50-ohm Setting)	—	50	mV
TMDS Clock Jitter	Clock Jitter Tolerance	—	0.25	UI

1. Output buffers must drive a translation device. Max. speed is 2Gbps. If translation device does not modify rise/fall time, the maximum speed is 1.5Gbps.
2. Input buffers must be AC coupled in order to support the 3.3V common mode. Generally, HDMI inputs are terminated by an external cable equalizer before data/clock is forwarded to the LatticeECP3 device.

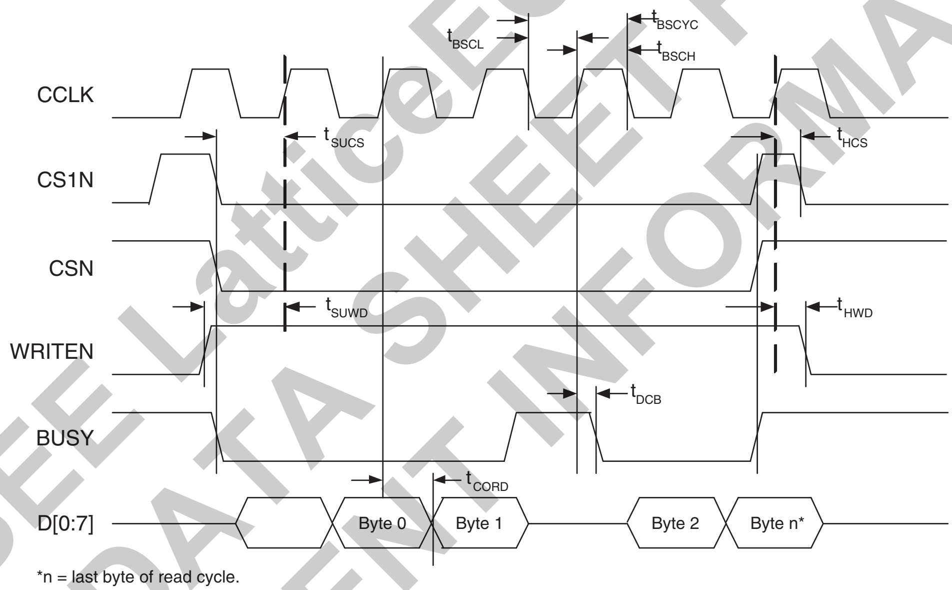
LatticeECP3 sysCONFIG Port Timing Specifications (Continued)

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
t_{CHHH}	HOLDN Low Hold Time (Relative to CCLK)	5	—	ns
Master and Slave SPI (Continued)				
t_{CHHL}	HOLDN High Hold Time (Relative to CCLK)	5	—	ns
t_{HHCH}	HOLDN High Setup Time (Relative to CCLK)	5	—	ns
t_{HLQZ}	HOLDN to Output High-Z	—	9	ns
t_{HHQX}	HOLDN to Output Low-Z	—	9	ns

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value - 15%	Selected value + 15%	MHz
Duty Cycle	40	60	%

Figure 3-16. sysCONFIG Parallel Port Read Cycle



Pin Information Summary (Cont.)

Pin Information Summary		ECP3-70E			ECP3-70EA		
Pin Type		484 fpBGA	672 fpBGA	1156 fpBGA	484 fpBGA	672 fpBGA	1156 fpBGA
Emulated Differential I/O per Bank	Bank 0	21	30	43	21	30	43
	Bank 1	18	24	39	18	24	39
	Bank 2	10	15	16	8	12	13
	Bank 3	23	27	39	20	23	33
	Bank 6	26	30	39	22	25	33
	Bank 7	14	20	22	11	16	18
	Bank 8	12	12	12	12	12	12
High-Speed Differential I/O per Bank	Bank 0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0
	Bank 2	4	6	6	6	9	9
	Bank 3	6	8	10	9	12	16
	Bank 6	7	9	10	11	14	16
	Bank 7	6	8	9	9	12	13
	Bank 8	0	0	0	0	0	0
Total Single-Ended/ Total Differential I/O per Bank	Bank 0	42/21	60/30	86/43	42/21	60/30	86/43
	Bank 1	36/18	48/24	78/39	36/18	48/24	78/39
	Bank 2	28/14	42/21	44/22	28/14	42/21	44/22
	Bank 3	58/29	71/35	98/49	58/29	71/35	98/49
	Bank 6	67/33	79/38	98/49	67/33	78/39	98/49
	Bank 7	40/20	56/28	62/31	40/20	56/28	62/31
	Bank 8	24/12	24/12	24/12	24/12	24/12	24/12
DDR Groups Bonded per Bank	Bank 0	3	5	7	3	5	7
	Bank 1	3	4	7	3	4	7
	Bank 2	2	3	3	2	3	3
	Bank 3	3	4	5	3	4	5
	Bank 6	4	4	5	4	4	5
	Bank 7	3	4	4	3	4	4
	Configuration Bank 8	0	0	0	0	0	0
SERDES Quads		1	2	3	1	2	3

LatticeECP3 Devices, Lead-Free Packaging

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Commercial

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-17EA-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	17
LFE3-17EA-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	17
LFE3-17EA-8FTN256C	1.2V	-8	Lead-Free ftBGA	256	COM	17
LFE3-17EA-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	17
LFE3-17EA-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	17
LFE3-17EA-8FN484C	1.2V	-8	Lead-Free fpBGA	484	COM	17

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-35EA-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	33
LFE3-35EA-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	33
LFE3-35EA-8FTN256C	1.2V	-8	Lead-Free ftBGA	256	COM	33
LFE3-35EA-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	33
LFE3-35EA-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	33
LFE3-35EA-8FN484C	1.2V	-8	Lead-Free fpBGA	484	COM	33
LFE3-35EA-6FN672C	1.2V	-6	Lead-Free fpBGA	672	COM	33
LFE3-35EA-7FN672C	1.2V	-7	Lead-Free fpBGA	672	COM	33
LFE3-35EA-8FN672C	1.2V	-8	Lead-Free fpBGA	672	COM	33

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-70EA-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	67
LFE3-70EA-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	67
LFE3-70EA-8FN484C	1.2V	-8	Lead-Free fpBGA	484	COM	67
LFE3-70EA-6FN672C	1.2V	-6	Lead-Free fpBGA	672	COM	67
LFE3-70EA-7FN672C	1.2V	-7	Lead-Free fpBGA	672	COM	67
LFE3-70EA-8FN672C	1.2V	-8	Lead-Free fpBGA	672	COM	67
LFE3-70EA-6FN1156C	1.2V	-6	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-7FN1156C	1.2V	-7	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-8FN1156C	1.2V	-8	Lead-Free fpBGA	1156	COM	67

Industrial

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-17EA-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	17
LFE3-17EA-7FTN256I	1.2V	-7	Lead-Free ftBGA	256	IND	17
LFE3-17EA-8FTN256I	1.2V	-8	Lead-Free ftBGA	256	IND	17
LFE3-17EA-6FN484I	1.2V	-6	Lead-Free fpBGA	484	IND	17
LFE3-17EA-7FN484I	1.2V	-7	Lead-Free fpBGA	484	IND	17
LFE3-17EA-8FN484I	1.2V	-8	Lead-Free fpBGA	484	IND	17

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-35EA-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	33
LFE3-35EA-7FTN256I	1.2V	-7	Lead-Free ftBGA	256	IND	33
LFE3-35EA-8FTN256I	1.2V	-8	Lead-Free ftBGA	256	IND	33
LFE3-35EA-6FN484I	1.2V	-6	Lead-Free fpBGA	484	IND	33
LFE3-35EA-7FN484I	1.2V	-7	Lead-Free fpBGA	484	IND	33
LFE3-35EA-8FN484I	1.2V	-8	Lead-Free fpBGA	484	IND	33
LFE3-35EA-6FN672I	1.2V	-6	Lead-Free fpBGA	672	IND	33
LFE3-35EA-7FN672I	1.2V	-7	Lead-Free fpBGA	672	IND	33
LFE3-35EA-8FN672I	1.2V	-7	Lead-Free fpBGA	672	IND	33

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-70EA-6FN484I	1.2V	-6	Lead-Free fpBGA	484	IND	67
LFE3-70EA-7FN484I	1.2V	-7	Lead-Free fpBGA	484	IND	67
LFE3-70EA-8FN484I	1.2V	-8	Lead-Free fpBGA	484	IND	67
LFE3-70EA-6FN672I	1.2V	-6	Lead-Free fpBGA	672	IND	67
LFE3-70EA-7FN672I	1.2V	-7	Lead-Free fpBGA	672	IND	67
LFE3-70EA-8FN672I	1.2V	-8	Lead-Free fpBGA	672	IND	67
LFE3-70EA-6FN1156I	1.2V	-6	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-7FN1156I	1.2V	-7	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-8FN1156I	1.2V	-8	Lead-Free fpBGA	1156	IND	67

LatticeECP3 Family Data Sheet Revision History

Date	Version	Section	Change Summary
February 2009	01.0	—	Initial release.
May 2009	01.1	All	Removed references to Parallel burst mode Flash.
		Introduction	Features - Changed 250 Mbps to 230 Mbps in Embedded SERDES bulleted section and added a footnote to indicate 230 Mbps applies to 8b10b and 10b12b applications.
			Updated data for ECP3-17 in LatticeECP3 Family Selection Guide table.
			Changed embedded memory from 552 to 700 Kbits in LatticeECP3 Family Selection Guide table.
		Architecture	Updated description for CLKFB in General Purpose PLL Diagram.
			Corrected Primary Clock Sources text section.
			Corrected Secondary Clock/Control Sources text section.
			Corrected Secondary Clock Regions table.
			Corrected note below Detailed sysDSP Slice Diagram.
			Corrected Clock, Clock Enable, and Reset Resources text section.
			Corrected ECP3-17 EBR number in Embedded SRAM in the LatticeECP3 Family table.
			Added On-Chip Termination Options for Input Modes table.
			Updated Available SERDES Quads per LatticeECP3 Devices table.
			Updated Simplified Channel Block Diagram for SERDES/PCS Block diagram.
			Updated Device Configuration text section.
			Corrected software default value of MCLK to be 2.5 MHz.
		DC and Switching Characteristics	Updated VCCOB Min/Max data in Recommended Operating Conditions table.
			Corrected footnote 2 in sysIO Recommended Operating Conditions table.
			Added added footnote 7 for t_{SKEW_PRIB} to External Switching Characteristics table.
			Added 2-to-1 Gearing text section and table.
			Updated External Reference Clock Specification (refclkp/refclkn) table.
			LatticeECP3 sysCONFIG Port Timing Specifications - updated t_{DINIT} information.
			Added sysCONFIG Port Timing waveform.
			Serial Input Data Specifications table, delete Typ data for $V_{RX-DIFF-S}$.
			Added footnote 4 to sysCLOCK PLL Timing table for t_{PFD}.
			Added SERDES/PCS Block Latency Breakdown table.
			External Reference Clock Specifications table, added footnote 4, add symbol name vREF-IN-DIFF.
			Added SERDES External Reference Clock Waveforms.
			Updated Serial Output Timing and Levels table.
			Pin-to-pin performance table, changed "typically 3% slower" to "typically slower".

Date	Version	Section	Change Summary
May 2009 (cont.)	01.1 (cont.)	DC and Switching Characteristics (cont.)	Updated timing information
			Updated SERDES minimum frequency.
			Added data to the following tables: External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, Maximum I/O Buffer Speed, DLL Timing, High Speed Data Transmitter, Channel Output Jitter, Typical Building Block Function Performance, Register-to-Register Performance, and Power Supply Requirements.
			Updated Serial Input Data Specifications table.
			Updated Transmit table, Serial Rapid I/O Type 2 Electrical and Timing Characteristics section.
		Pinout Information	Updated Signal Description tables.
			Updated Pin Information Summary tables and added footnote 1.
July 2009	01.2	Multiple	Changed references of “multi-boot” to “dual-boot” throughout the data sheet.
		Architecture	Updated On-Chip Programmable Termination bullets.
			Updated On-Chip Termination Options for Input Modes table.
			Updated On-Chip Termination figure.
		DC and Switching Characterisitcs	Changed min/max data for FREF_PPM and added footnote 4 in SERDES External Reference Clock Specification table.
			Updated SERDES minimum frequency.
		Pinout Information	Corrected MCLK to be I/O and CCLK to be I in Signal Descriptions table
August 2009	01.3	DC and Switching Characterisitcs	Corrected truncated numbers for V_{CCIB} and V_{CCOB} in Recommended Operating Conditions table.
September 2009	01.4	Architecture	Corrected link in sysMEM Memory Block section.
			Updated information for On-Chip Programmable Termination and modified corresponding figure.
			Added footnote 2 to On-Chip Programmable Termination Options for Input Modes table.
			Corrected Per Quadrant Primary Clock Selection figure.
		DC and Switching Characterisitcs	Modified -8 Timing data for 1024x18 True-Dual Port RAM (Read-Before-Write, EBR Output Registers)
			Added ESD Performance table.
			LatticeECP3 External Switching Characteristics table - updated data for $t_{DIBGDDR}$, t_{W_PRI}, t_{W_EDGE} and $t_{SKEW\_EDGE\_DQS}$.
			LatticeECP3 Internal Switching Characteristics table - updated data for t_{COO_PIO} and added footnote #4.
			sysCLOCK PLL Timing table - updated data for f_{OUT}.
			External Reference Clock Specification (refclkp/refclkn) table - updated data for $V_{REF-IN-SE}$ and $V_{REF-IN-DIFF}$
			LatticeECP3 sysCONFIG Port Timing Specifications table - updated data for t_{MWC}.
			Added TRLVDS DC Specification table and diagram.
			Updated Mini LVDS table.
November 2009	01.5	Introduction	Updated Embedded SERDES features.
			Added SONET/SDH to Embedded SERDES protocols.
		Architecture	Updated Figure 2-4, General Purpose PLL Diagram.
			Updated SONET/SDH to SERDES and PCS protocols.