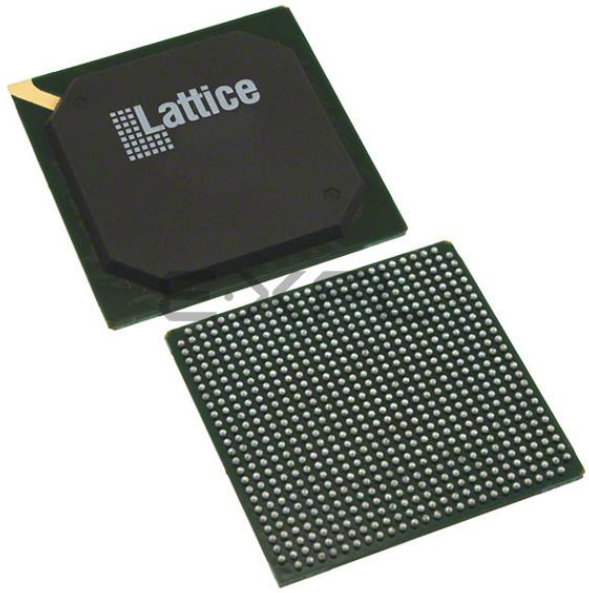
# Lattice Semiconductor Corporation - LFE3-95E-6FN672I Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

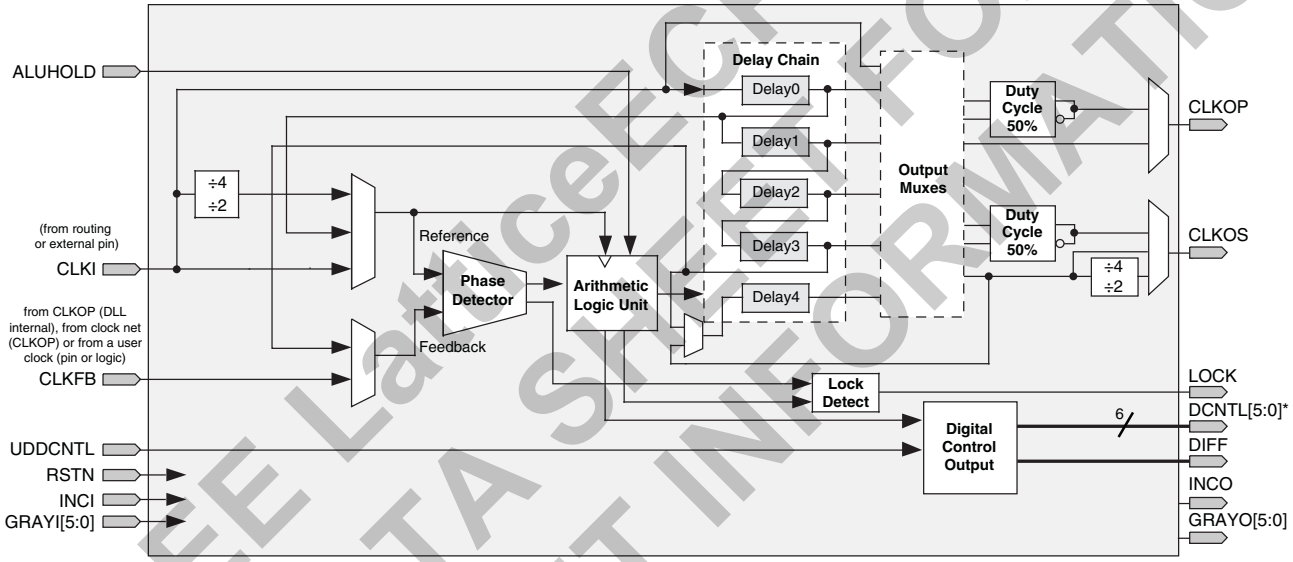
| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 11500 |
| Number of Logic Elements/Cells | 92000 |
| Total RAM Bits | 4526080 |
| Number of I/O | 380 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 672-BBGA |
| Supplier Device Package | 672-FPBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95e-6fn672i |

chain in order to better match the reference and feedback signals. This digital code from the ALU is also transmitted via the Digital Control bus (DCNTL) bus to its associated Slave Delay lines (two per DLL). The ALUHOLD input allows the user to suspend the ALU output at its current value. The UDDCNTL signal allows the user to latch the current value on the DCNTL bus.

The DLL has two clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine delay shift and divider blocks to allow this output to be further modified, if required. The fine delay shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. Both the CLKOS and CLKOP outputs are available with optional duty cycle correction. Divide by two and divide by four frequencies are available at CLKOS. The LOCK output signal is asserted when the DLL is locked. Figure 2-5 shows the DLL block diagram and Table 2-5 provides a description of the DLL inputs and outputs.

The user can configure the DLL for many common functions such as time reference delay mode and clock injection removal mode. Lattice provides primitives in its design tools for these functions.

***Figure 2-5. Delay Locked Loop Diagram (DLL)***

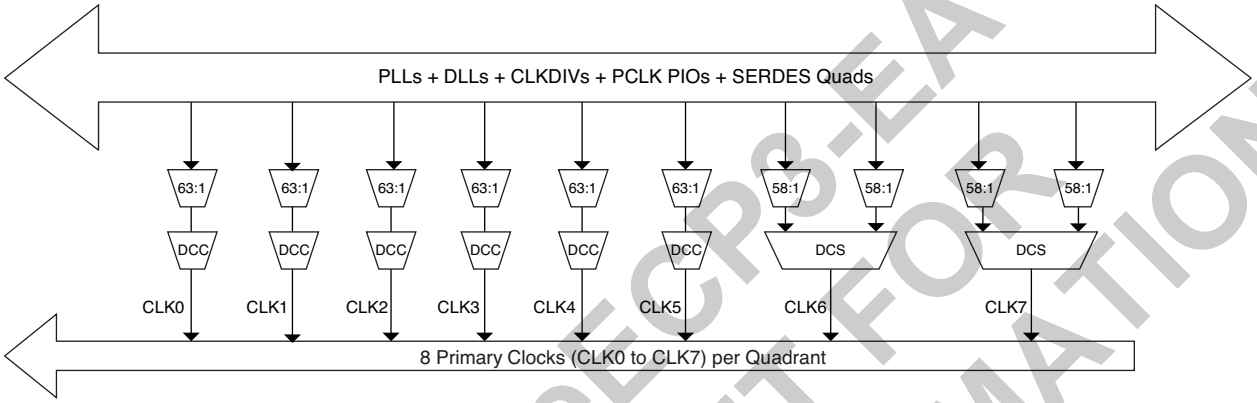



* This signal is not user accessible. This can only be used to feed the slave delay line.

## Primary Clock Routing

The purpose of the primary clock routing is to distribute primary clock sources to the destination quadrants of the device. A global primary clock is a primary clock that is distributed to all quadrants. The clock routing structure in LatticeECP3 devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 2-12 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally.

***Figure 2-12. Per Quadrant Primary Clock Selection***




## Dynamic Clock Control (DCC)

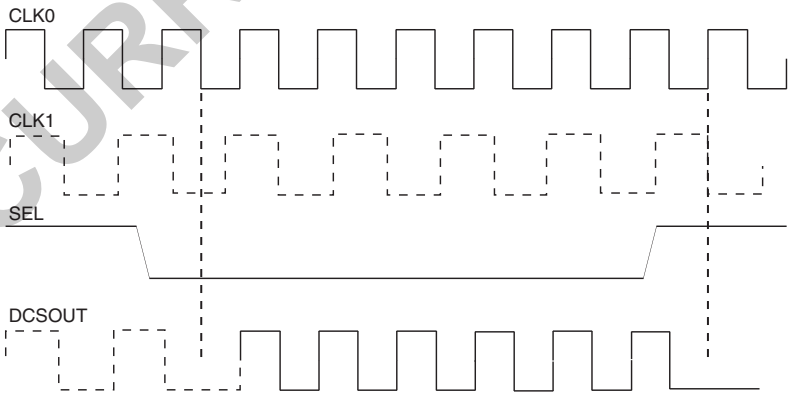
The DCC (Quadrant Clock Enable/Disable) feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, all the logic fed by that clock does not toggle, reducing the overall power consumption of the device.

## Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved regardless of when the select signal is toggled. There are two DCS blocks per quadrant; in total, there are eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 2-12).

Figure 2-13 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, please see the list of technical documentation at the end of this data sheet.

***Figure 2-13. DCS Waveforms***

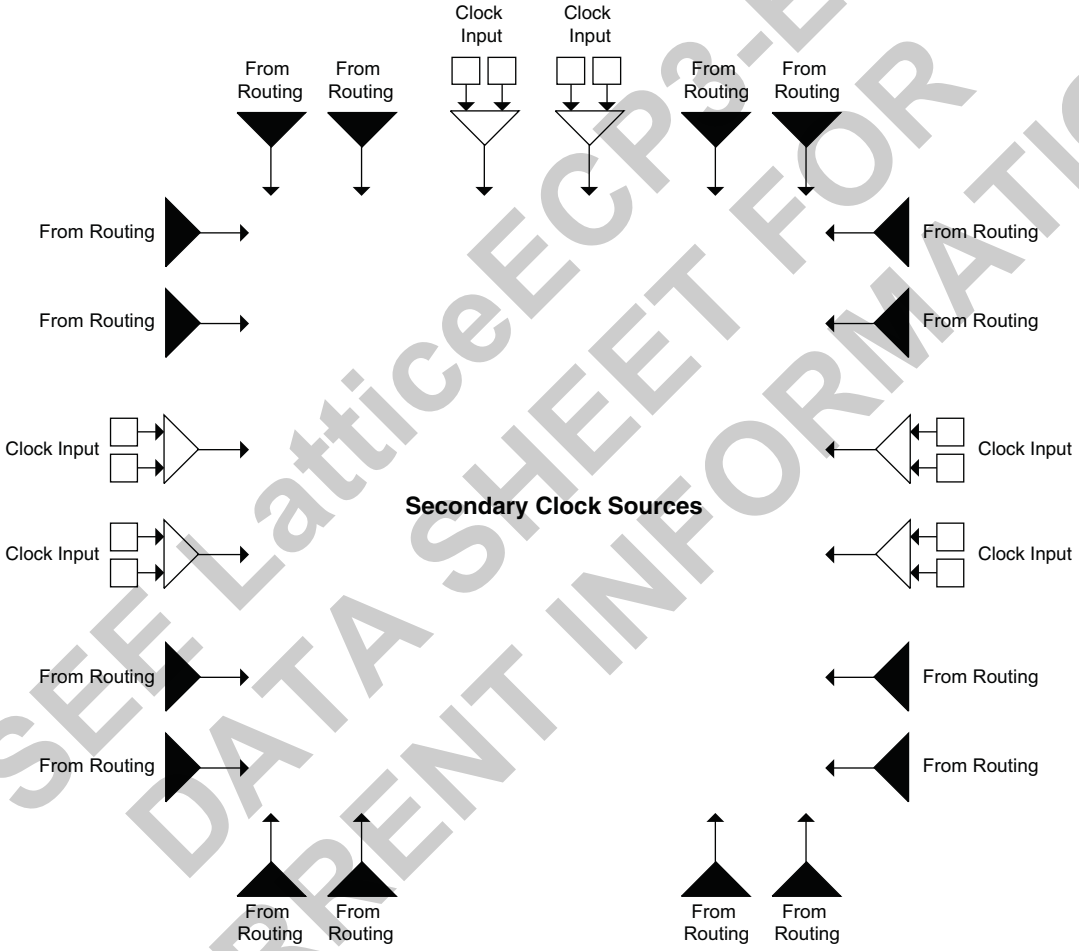


## Secondary Clock/Control Sources

LatticeECP3 devices derive eight secondary clock sources (SC0 through SC7) from six dedicated clock input pads and the rest from routing. Figure 2-14 shows the secondary clock sources. All eight secondary clock sources are defined as inputs to a per-region mux SC0-SC7. SC0-SC3 are primary for control signals (CE and/or LSR), and SC4-SC7 are for clock and high fanout data.

In an actual implementation, there is some overlap to maximize routability. In addition to SC0-SC3, SC7 is also an input to the control signals (LSR or CE). SC0-SC2 are also inputs to clocks along with SC4-SC7. High fanout logic signals (LUT inputs) will utilize the X2 and X0 switches where SC0-SC7 are inputs to X2 switches, and SC4-SC7 are inputs to X0 switches. Note that through X0 switches, SC4-SC7 can also access control signals CE/LSR.

***Figure 2-14. Secondary Clock Sources***

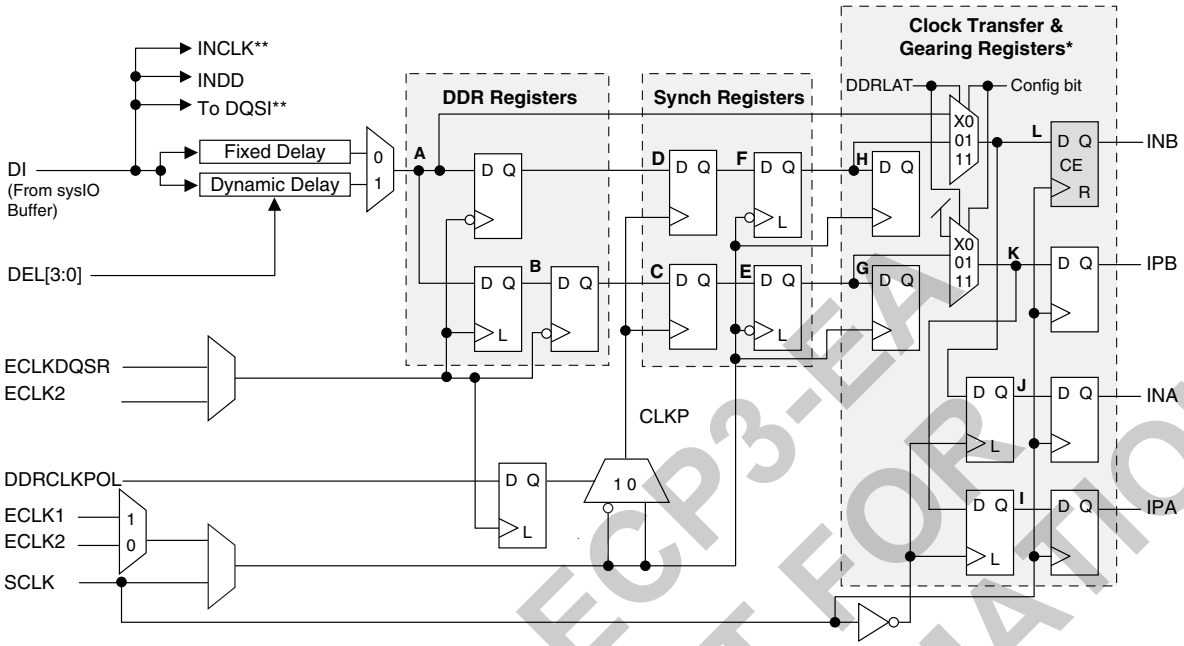



Note: Clock inputs can be configured in differential or single-ended mode.

## Secondary Clock/Control Routing

Global secondary clock is a secondary clock that is distributed to all regions. The purpose of the secondary clock routing is to distribute the secondary clock sources to the secondary clock regions. Secondary clocks in the LatticeECP3 devices are region-based resources. Certain EBR rows and special vertical routing channels bind the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP slice in the DSP row or the center of the DSP row. Figure 2-15 shows this special vertical routing channel and the 20 secondary clock regions for the LatticeECP3 family of devices. All devices in the LatticeECP3 family have eight

*Figure 2-33. ECP3-70/95 (E or EA) Input Register Block for Left, Right and Top Edges*




* Only on the left and right sides.
** Selected PIO.
Note: Simplified diagram does not show CE/SET/REST details.

## Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysI/O buffers. The blocks on the left and right PIOs contain registers for SDR and full DDR operation. The topside PIO block is the same as the left and right sides except it does not support ODDRX2 gearing of output logic. ODDRX2 gearing is used in DDR3 memory interfaces.The PIO blocks on the bottom contain the SDR registers and generic DDR interface without gearing.

Figure 2-34 shows the Output Register Block for PIOs on the left and right edges.

In SDR mode, OPOSA feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a Dtype or latch. In DDR mode, two of the inputs are fed into registers on the positive edge of the clock. At the next clock cycle, one of the registered outputs is also latched.

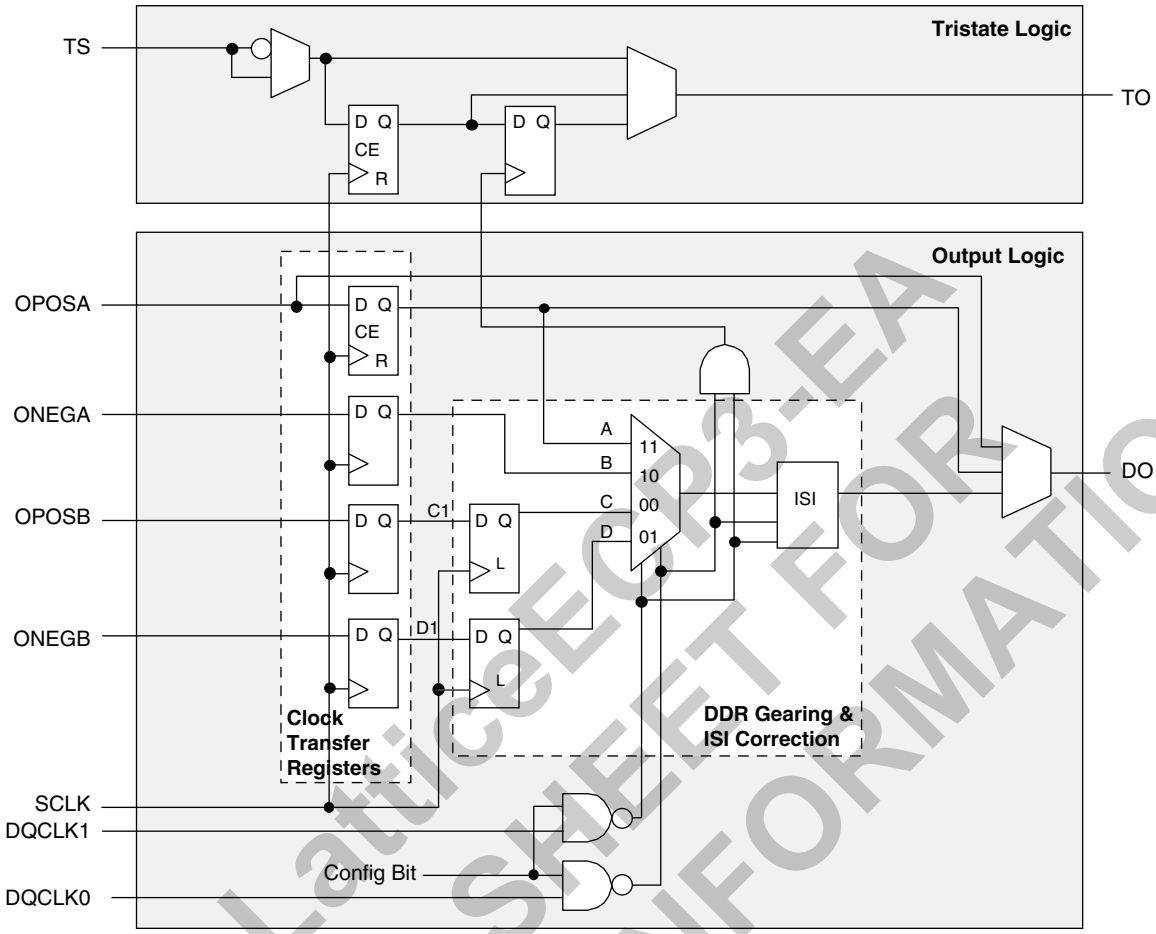
A multiplexer running off the same clock is used to switch the mux between the 11 and 01 inputs that will then feed the output.

A gearbox function can be implemented in the output register block that takes four data streams: OPOSA, ONEGA, OPOSB and ONEGB. All four data inputs are registered on the positive edge of the system clock and two of them are also latched. The data is then output at a high rate using a multiplexer that runs off the DQCLK0 and DQCLK1 clocks. DQCLK0 and DQCLK1 are used in this case to transfer data from the system clock to the edge clock domain. These signals are generated in the DQS Write Control Logic block. See Figure 2-37 for an overview of the DQS write control logic.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.

Further discussion on using the DQS strobe in this module is discussed in the DDR Memory section of this data sheet.

*Figure 2-34. ECP3-70/95 (E or EA) Output and Tristate Block for Left and Right Edges*




## Tristate Register Block

The tristate register block registers tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation and an additional register for DDR operation.

In SDR and non-gearing DDR modes, TS input feeds one of the flip-flops that then feeds the output. In DDRX2 mode, the register TS input is fed into another register that is clocked using the DQCLK0 and DQCLK1 signals. The output of this register is used as a tristate control.

## ISI Calibration

The setting for Inter-Symbol Interference (ISI) cancellation occurs in the output register block. ISI correction is only available in the DDRX2 modes. ISI calibration settings exist once per output register block, so each I/O in a DQS-12 group may have a different ISI calibration setting.

The ISI block extends output signals at certain times, as a function of recent signal history. So, if the output pattern consists of a long strings of 0's to long strings of 1's, there are no delays on output signals. However, if there are quick, successive transitions from 010, the block will stretch out the binary 1. This is because the long trail of 0's will cause these symbols to interfere with the logic 1. Likewise, if there are quick, successive transitions from 101, the block will stretch out the binary 0. This block is controlled by a 3-bit delay control that can be set in the DQS control logic block.

For more information about this topic, please see the list of technical documentation at the end of this data sheet.

### Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block.

## DDR Memory Support

Certain PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR1, DDR2 and DDR3 memory interfaces. The support varies by the edge of the device as detailed below.

### Left and Right Edges

The left and right sides of the PIC have fully functional elements supporting DDR1, DDR2, and DDR3 memory interfaces. One of every 12 PIOs supports the dedicated DQS pins with the DQS control logic block. Figure 2-35 shows the DQS bus spanning 11 I/O pins. Two of every 12 PIOs support the dedicated DQS and DQS# pins with the DQS control logic block.

### Bottom Edge

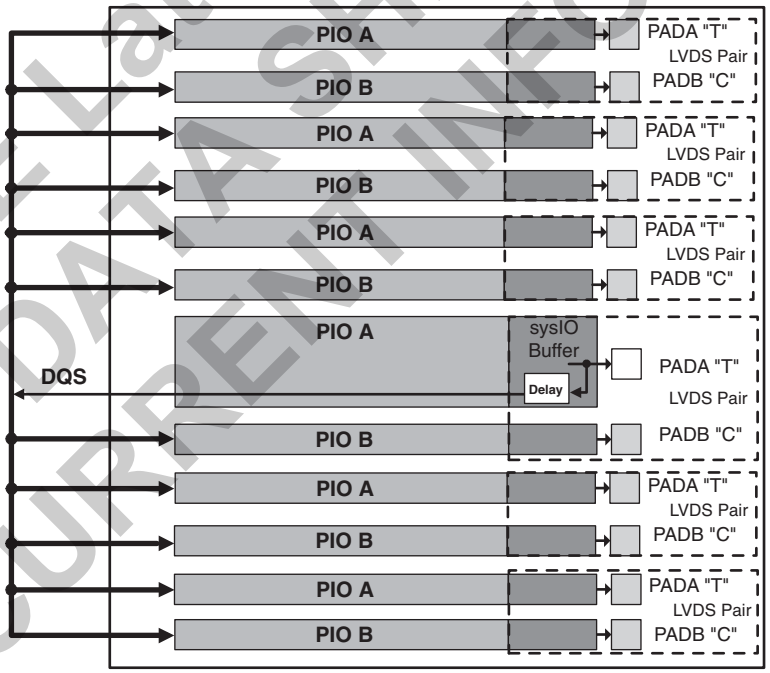
PICs on the bottom edge of the device do not support DDR memory and Generic DDR interfaces.

### Top Edge

PICs on the top side are similar to the PIO elements on the left and right sides but do not support gearing on the output registers. Hence, the modes to support output/tristate DDR3 memory are removed on the top side.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left, right and top edges are designed for DDR memories that support 10 bits of data.

***Figure 2-35. DQS Grouping on the Left, Right and Top Edges***




### DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces, a PLL is used for this adjustment. However, in DDR memories the clock

(referred to as DQS) is not free-running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The delay required for the DQS signal is generated by two dedicated DLLs (DDR DLL) on opposite side of the device. Each DLL creates DQS delays in its half of the device as shown in Figure 2-36. The DDR DLL on the left side will generate delays for all the DQS Strobe pins on Banks 0, 7 and 6 and DDR DLL on the right will generate delays for all the DQS pins on Banks 1, 2 and 3. The DDR DLL loop compensates for temperature, voltage and process variations by using the system clock and DLL feedback loop. DDR DLL communicates the required delay to the DQS delay block using a 7-bit calibration bus (DCNTL[6:0])

The DQS signal (selected PIOs only, as shown in Figure 2-35) feeds from the PAD through a DQS control logic block to a dedicated DQS routing resource. The DQS control logic block consists of DQS Read Control logic block that generates control signals for the read side and DQS Write Control logic that generates the control signals required for the write side. A more detailed DQS control diagram is shown in Figure 2-37, which shows how the DQS control blocks interact with the data paths.

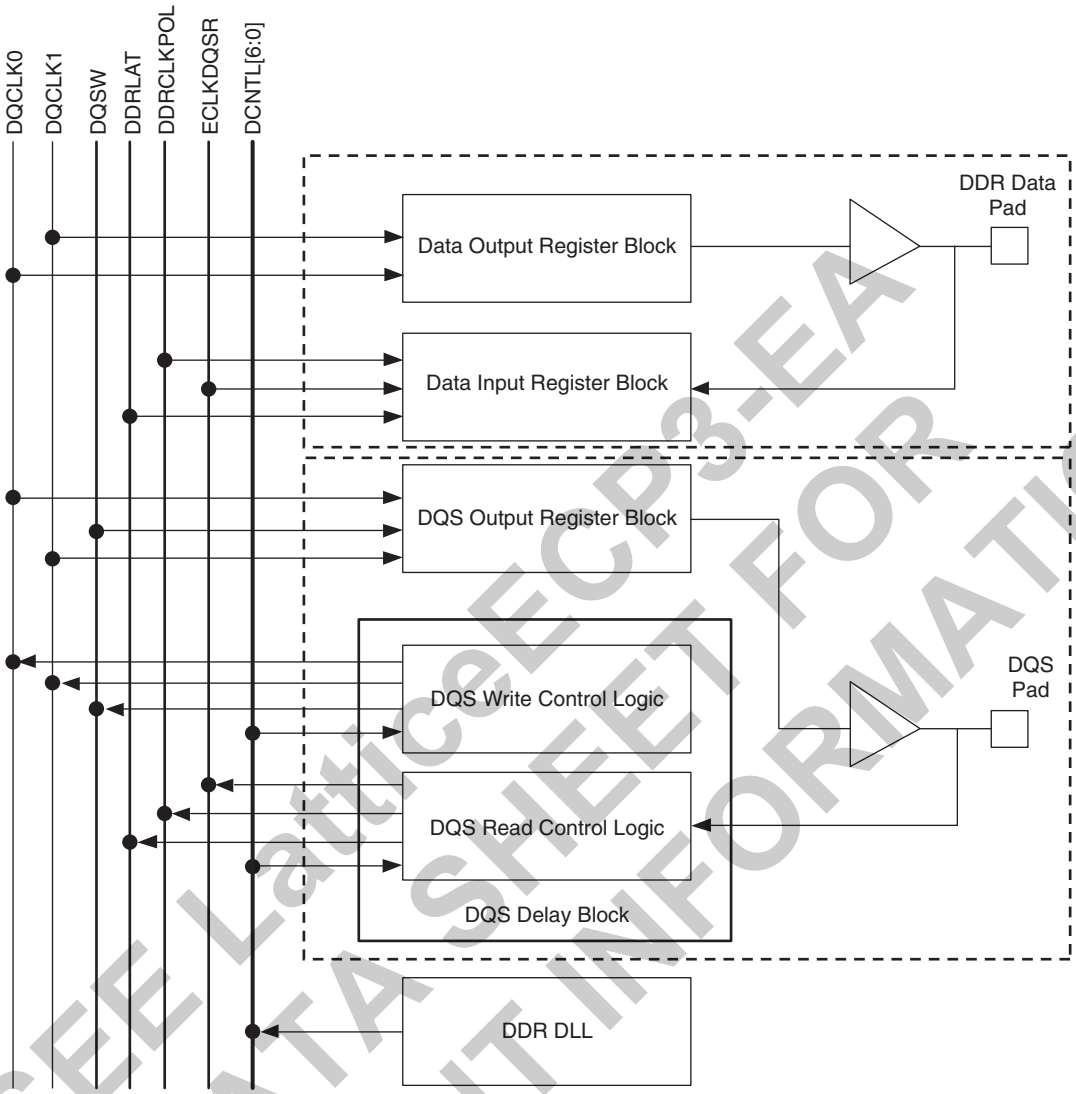
The DQS Read control logic receives the delay generated by the DDR DLL on its side and delays the incoming DQS signal by 90 degrees. This delayed ECLKDQSR is routed to 10 or 11 DQ pads covered by that DQS signal. This block also contains a polarity control logic that generates a DDRCLKPOL signal, which controls the polarity of the clock to the sync registers in the input register blocks. The DQS Read control logic also generates a DDRLAT signal that is in the input register block to transfer data from the first set of DDR register to the second set of DDR registers when using the DDRX2 gearbox mode for DDR3 memory interface.

The DQS Write control logic block generates the DQCLK0 and DQCLK1 clocks used to control the output gearing in the Output register block which generates the DDR data output and the DQS output. They are also used to control the generation of the DQS output through the DQS output register block. In addition to the DCNTL [6:0] input from the DDR DLL, the DQS Write control block also uses a Dynamic Delay DYN DEL [7:0] attribute which is used to further delay the DQS to accomplish the write leveling found in DDR3 memory. Write leveling is controlled by the DDR memory controller implementation. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock. This will generate the DQSW signal used to generate the DQS output in the DQS output register block.

Figure 2-36 and Figure 2-37 show how the DQS transition signals that are routed to the PIOs.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.

*Figure 2-37. DQS Local Bus*






## Polarity Control Logic

In a typical DDR Memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LatticeECP3 family contains dedicated circuits to transfer data between these domains. A clock polarity selector is used to prevent set-up and hold violations at the domain transfer between DQS (delayed) and the system clock. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects the first DQS rising edge after the preamble state. This signal is used to control the polarity of the clock to the synchronizing registers.

## DDR3 Memory Support

LatticeECP3 supports the read and write leveling required for DDR3 memory interfaces.

Read leveling is supported by the use of the DDRCLKPOL and the DDRLAT signals generated in the DQS Read Control logic block. These signals dynamically control the capture of the data with respect to the DQS at the input register block.

To accomplish write leveling in DDR3, each DQS group has a slightly different delay that is set by DYN DELAY[7:0] in the DQS Write Control logic block. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock.

LatticeECP3 input and output registers can also support DDR gearing that is used to receive and transmit the high speed DDR data from and to the DDR3 Memory.

LatticeECP3 supports the 1.5V SSTL I/O standard required for the DDR3 memory interface. In addition, it supports on-chip termination to VTT on the DDR3 memory input pins. For more information, refer to the sysIO section of this data sheet.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on DDR Memory interface implementation in LatticeECP3.

## sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVDS, BLVDS, HSTL, SSTL Class I & II, LVCMOS, LVTTL, LVPECL, PCI.

### sysI/O Buffer Banks

LatticeECP3 devices have six sysI/O buffer banks: six banks for user I/Os arranged two per side. The banks on the bottom side are wraparounds of the banks on the lower right and left sides. The seventh sysI/O buffer bank (Configuration Bank) is located adjacent to Bank 2 and has dedicated/shared I/Os for configuration. When a shared pin is not used for configuration it is available as a user I/O. Each bank is capable of supporting multiple I/O standards. Each sysI/O bank has its own I/O supply voltage ($V_{CCIO}$). In addition, each bank, except the Configuration Bank, has voltage references, $V_{REF1}$ and $V_{REF2}$, which allow it to be completely independent from the others. The Configuration Bank top side shares $V_{REF1}$ and $V_{REF2}$ from sysI/O bank 1 and right side shares $V_{REF1}$ and $V_{REF2}$ from sysI/O bank 2. Figure 2-38 shows the seven banks and their associated supplies.

In LatticeECP3 devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using $V_{CCIO}$. LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of $V_{CCIO}$.

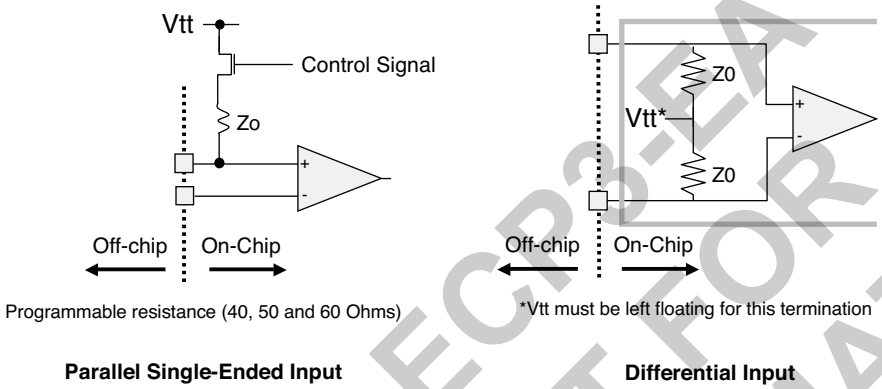
Each bank can support up to two separate $V_{REF}$ voltages, $V_{REF1}$ and $V_{REF2}$, that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

## On-Chip Programmable Termination

The LatticeECP3 supports a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single Ended Termination for SSTL15 inputs with programmable resistor values of 40, 50, or 60 ohms. This is particularly useful for low power JEDEC compliant DDR3 memory controller implementations. External termination to Vtt should be used for DDR2 memory controller implementation.
- Common mode termination of 80, 100, 120 ohms for differential inputs

***Figure 2-39. On-Chip Termination***




See Table 2-12 for termination options for input modes.

***Table 2-12. On-Chip Termination Options for Input Modes***

| IO_TYPE | TERMINATE to VTT[1, 2] | DIFFRENTIAL TERMINATION RESISTOR[1] |
|---|---|---|
| LVDS25 | þ | 80, 100, 120 |
| BLVDS25 | þ | 80, 100, 120 |
| MLVDS | þ | 80, 100, 120 |
| HSTL18_I | 40, 50, 60 | þ |
| HSTL18_II | 40, 50, 60 | þ |
| HSTL18D_I | 40, 50, 60 | þ |
| HSTL18D_II | 40, 50, 60 | þ |
| HSTL15_I | 40, 50, 60 | þ |
| HSTL15D_I | 40, 50, 60 | þ |
| SSTL25_I | 40, 50, 60 | þ |
| SSTL25_II | 40, 50, 60 | þ |
| SSTL25D_I | 40, 50, 60 | þ |
| SSTL25D_II | 40, 50, 60 | þ |
| SSTL18_I | 40, 50, 60 | þ |
| SSTL18_II | 40, 50, 60 | þ |
| SSTL18D_I | 40, 50, 60 | þ |
| SSTL18D_II | 40, 50, 60 | þ |
| SSTL15 | 40, 50, 60 | þ |
| SSTL15D | 40, 50, 60 | þ |

1. TERMINATE to VTT and DIFFRENTIAL TERMINATION RESISTOR when turn on can only have one setting per bank. Only left and right banks have this feature.
   Use of TERMINATE to VTT and DIFFRENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank.
   On-chip termination tolerance +/- 20%
2. External termination to VTT should be used when implementing DDR2 memory controller.

The ispLEVER design tools from Lattice support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With ispLEVER, the user can define the mode for each quad in a design.

Popular standards such as 10Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), a single quad (Four SERDES channels and PCS) and some additional logic from the core.

The LatticeECP3 family also supports a wide range of primary and secondary protocols. Within the same quad, the LatticeECP3 family can support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. Table 2-15 lists the allowable combination of primary and secondary protocol combinations.

## Flexible Quad SERDES Architecture

The LatticeECP3 family SERDES architecture is a quad-based architecture. For most SERDES settings and standards, the whole quad (consisting of four SERDES) is treated as a unit. This helps in silicon area savings, better utilization and overall lower cost.

However, for some specific standards, the LatticeECP3 quad architecture provides flexibility; more than one standard can be supported within the same quad.

Table 2-15 shows the standards can be mixed and matched within the same quad. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same quad. In Table 2-15, the Primary Protocol column refers to the standard that determines the reference clock and PLL settings. The Secondary Protocol column shows the other standard that can be supported within the same quad.

Furthermore, Table 2-15 also implies that more than two standards in the same quad can be supported, as long as they conform to the data rate and reference clock requirements. For example, a quad may contain PCI Express 1.1, SGMII, Serial RapidIO Type I and Serial RapidIO Type II, all in the same quad.

***Table 2-15. LatticeECP3 Primary and Secondary Protocol Support***

| Primary Protocol | Secondary Protocol |
|---|---|
| PCI Express 1.1 | SGMII |
| PCI Express 1.1 | Gigabit Ethernet |
| PCI Express 1.1 | Serial RapidIO Type I |
| PCI Express 1.1 | Serial RapidIO Type II |
| Serial RapidIO Type I | SGMII |
| Serial RapidIO Type I | Gigabit Ethernet |
| Serial RapidIO Type II | SGMII |
| Serial RapidIO Type II | Gigabit Ethernet |
| Serial RapidIO Type II | Serial RapidIO Type I |
| CPRI-3 | CPRI-2 and CPRI-1 |
| 3G-SDI | HD-SDI and SD-SDI |

For further information on SERDES, please see TN1176, LatticeECP3 SERDES/PCS Usage Guide.

## IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeECP3 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test

## Hot Socketing Specifications[1, 3, 4]

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| IDK_HS[2] | Input or I/O Leakage Current | $0 \le V_{IN} \le V_{IH}$ (Max.) | — | — | +/-1 | mA |
| IDK[5] | Input or I/O Leakage Current | $0 \le V_{IN} < V_{CCIO}$ | — | — | +/-1 | mA |
| | | $V_{CCIO} \le V_{IN} \le V_{CCIO}$ + 0.5V | — | 18 | — | mA |

1. $V_{CC}$, $V_{CCAUX}$ and $V_{CCIO}$ should rise/fall monotonically.
2. Applicable to general purpose I/O pins in top I/O banks only.
3. $I_{DK}$ is additive to $I_{PU}$, $I_{PW}$ or $I_{BH}$.
4. LVCMOS and LVTTL only.
5. Applicable to general purpose I/O pins in left and right I/O banks only.

## Hot Socketing Requirements[1, 2]

| Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Input current per SERDES I/O pin when device is powered down and inputs driven. | — | — | 8 | mA |

1. Assumes the device is powered down, all supplies grounded, both P and N inputs driven by CML driver with maximum allowed VCCOB (1.575V), 8b10b data, internal AC coupling.
2. Each P and N input must have less than the specified maximum input current. For a 16-channel device, the total input current would be 8mA*16 channels *2 input pins per channel = 256mA

## ESD Performance

| Pin Group | ESD Stress | Min. | Units |
|---|---|---|---|
| All pins | HBM | 1000 | V |
| All pins except high-speed serial and XRES[1] | CDM | 500 | V |
| High-speed serial inputs | CDM | 400 | V |

1. The XRES pin on the TW device passes CDM testing at 250V.

# LatticeECP3 External Switching Characteristics (Continued)[1, 2]

**Over Recommended Commercial Operating Conditions**

| Parameter | Description | Device | -8 | | -7 | | -6 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $f_{MAX\_IO}$ | Clock Frequency of I/O and PFU Register | ECP3-70E/95E | — | 500 | — | 420 | — | 375 | Mhz |
| **General I/O Pin Parameters Using Dedicated Clock Input Primary Clock with PLL with Clock Injection Removal Setting[2]** | | | | | | | | | |
| $t_{COPLL}$ | Clock to Output - PIO Output Register | ECP3-150EA | — | 2.5 | — | 2.7 | — | 3.1 | ns |
| $t_{SUPLL}$ | Clock to Data Setup - PIO Input Register | ECP3-150EA | 0.6 | — | 0.6 | — | 0.7 | — | ns |
| $t_{HPLL}$ | Clock to Data Hold - PIO Input Register | ECP3-150EA | 0.9 | — | 1.0 | — | 1.1 | — | ns |
| $t_{SU\_DELPLL}$ | Clock to Data Setup - PIO Input Register with Data Input Delay | ECP3-150EA | 1.5 | — | 1.6 | — | 1.8 | — | ns |
| $t_{H\_DELPLL}$ | Clock to Data Hold - PIO Input Register with Input Data Delay | ECP3-150EA | — | 0.1 | — | 0.1 | — | 0.1 | ns |
| $t_{COPLL}$ | Clock to Output - PIO Output Register | ECP3-70E/95E | — | 2.2 | — | 2.3 | — | 2.5 | ns |
| $t_{SUPLL}$ | Clock to Data Setup - PIO Input Register | ECP3-70E/95E | 0.6 | — | 0.7 | — | 0.8 | — | ns |
| $t_{HPLL}$ | Clock to Data Hold - PIO Input Register | ECP3-70E/95E | 0.9 | — | 1.1 | — | 1.3 | — | ns |
| $t_{SU\_DELPLL}$ | Clock to Data Setup - PIO Input Register with Data Input Delay | ECP3-70E/95E | 1.6 | — | 1.9 | — | 2.1 | — | ns |
| $t_{H\_DELPLL}$ | Clock to Data Hold - PIO Input Register with Input Data Delay | ECP3-70E/95E | 0.0 | — | 0.0 | — | 0.0 | — | ns |

| Parameter | Description | Device | -8 | | -7 | | -6 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Generic DDR** | | | | | | | | | |
| **Generic DDRX1 Inputs with Clock and Data (>10 Bits Wide) Centered at Pin (GDDRX1_RX.SCLK.Centered) Using PCLK Pin for Clock Input** | | | | | | | | | |
| **Data Left, Right and Top Sides & Clock Left, Right and Top Sides** | | | | | | | | | |
| $t_{SUGDDR}$ | Data Setup Before CLK | ECP3-150EA | | — | | — | | — | ps |
| $t_{HGDDR}$ | Data Hold After CLK | ECP3-150EA | | — | | — | | — | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-150EA | — | | — | | — | | MHz |
| **Generic DDRX1 Inputs with Clock in the Center of Data Window, without DLL (GDDRX1_RX.ECLK.Centered)** | | | | | | | | | |
| $t_{SUGDDR}$ | Data Setup Before CLK | ECP3-70E/95E | 515 | — | 515 | — | 515 | — | ps |
| $t_{HOGDDR}$ | Data Hold After CLK | ECP3-70E/95E | 515 | — | 515 | — | 515 | — | ps |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-70E/95E | — | 250 | — | 250 | — | 250 | MHz |
| **Generic DDRX1 Inputs with Clock and Data (> 10 Bits Wide) Aligned at Pin (GDDRX1_RX.SCLK.Aligned) using DLL-CLKIN Pin for Clock Input** | | | | | | | | | |
| **Data Left, Right and Top Sides & Clock Left and Right Sides** | | | | | | | | | |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | ECP3-150EA | — | | — | | — | | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | ECP3-150EA | | — | | — | | — | UI |
| $f_{MAX\_GDDR}$ | DDRX1 Clock Frequency | ECP3-150EA | — | | — | | — | | MHz |
| **Generic DDRX1 Inputs with Clock and Data Aligned, with DLL (GDDRX1_RX.ECLK.Aligned)** | | | | | | | | | |
| $t_{DVACLKGDDR}$ | Data Setup Before CLK | ECP3-70E/95E | — | 0.235 | — | 0.235 | — | 0.235 | UI |
| $t_{DVECLKGDDR}$ | Data Hold After CLK | ECP3-70E/95E | 0.765 | — | 0.765 | — | 0.765 | — | UI |

# LatticeECP3 External Switching Characteristics (Continued)[1, 2]

**Over Recommended Commercial Operating Conditions**

| Parameter | Description | Device | -8 | | -7 | | -6 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Generic DDRX2 Output with Clock and Data (> 10 Bits Wide) Aligned at Pin (GDDRX2_TX.ECLK.Aligned)** | | | | | | | | | |
| **Left and Right Sides** | | | | | | | | | |
| $t_{DIBGDDR}$ | Data Setup Before CLK | ECP3-150EA | — | | — | | — | | ps |
| $t_{DIAGDDR}$ | Data Hold After CLK | ECP3-150EA | — | | — | | — | | ps |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-150EA | — | | — | | — | | MHz |
| **Generic DDRX2 Outputs with Clock and Data Edges Aligned, Without PLL 90-degree shifted clock output[5] (GDDRX2_TX.Aligned)** | | | | | | | | | |
| $t_{DIBGDDR}$ | Data Invalid Before Clock | ECP3-70E/95E | — | 200 | — | 225 | — | 250 | ps |
| $t_{DIAGDDR}$ | Data Invalid After Clock | ECP3-70E/95E | — | 200 | — | 225 | — | 250 | ps |
| $f_{MAX\_GDDR}$ | DDR/DDRX2 Clock Frequency[8] | ECP3-70E/95E | — | 500 | — | 420 | — | 375 | MHz |
| **Generic DDRX2 Output with Clock and Data (> 10 Bits Wide) Centered at Pin Using DQSDLL (GDDRX2_TX.DQS-DLL.Centered)** | | | | | | | | | |
| **Left and Right Sides** | | | | | | | | | |
| $t_{DVBGDDR}$ | Data Valid Before CLK | ECP3-150EA | | — | | — | | — | ns |
| $t_{DVAGDDR}$ | Data Valid After CLK | ECP3-150EA | | — | | — | | — | ns |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-150EA | — | | — | | — | | ns |
| **Generic DDRX2 Output with Clock and Data (> 10 Bits Wide) Centered at Pin Using PLL (GDDRX2_TX.PLL.Centered)** | | | | | | | | | |
| **Left and Right Sides** | | | | | | | | | |
| $t_{DVBGDDR}$ | Data Valid Before CLK | ECP3-150EA | | — | | — | | — | ns |
| $t_{DVAGDDR}$ | Data Valid After CLK | ECP3-150EA | | — | | — | | — | ns |
| $f_{MAX\_GDDR}$ | DDRX2 Clock Frequency | ECP3-150EA | — | | — | | — | | ns |
| **Generic DDRX2 Outputs with Clock Edge in the Center of Data Window, with PLL 90-degree Shifted Clock Output[6] (GDDRX2_TX.PLL.Centered)** | | | | | | | | | |
| $t_{DVBGDDR}$ | Data Valid Before CLK | ECP3-70E/95E | 300 | — | 370 | — | 417 | — | ps |
| $t_{DVAGDDR}$ | Data Valid After CLK | ECP3-70E/95E | 300 | — | 370 | — | 417 | — | ps |
| $f_{MAX\_GDDR}$ | DDR/DDRX2 Clock Frequency[8] | ECP3-70E/95E | — | 500 | — | 420 | — | 375 | MHz |

| Parameter | Description | Device | -8 | | -7 | | -6 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Memory Interface** | | | | | | | | | |
| **DDR/DDR2 SDRAM I/O Pin Parameters (Input Data are Strobe Edge Aligned, Output Strobe Edge is Data Centered)[4]** | | | | | | | | | |
| $t_{DVADQ}$ | Data Valid After DQS (DDR Read) | ECP3-150EA | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVEDQ}$ | Data Hold After DQS (DDR Read) | ECP3-150EA | 0.64 | — | 0.64 | — | 0.64 | — | UI |
| $t_{DQVBS}$ | Data Valid Before DQS | ECP3-150EA | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Data Valid After DQS | ECP3-150EA | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{MAX\_DDR}$ | DDR Clock Frequency | ECP3-150EA | 95 | 200 | 95 | 200 | 95 | 166 | MHz |
| $f_{MAX\_DDR2}$ | DDR2 clock frequency | ECP3-150EA | 133 | 266 | 133 | 200 | 133 | 166 | MHz |
| $t_{DVADQ}$ | Data Valid After DQS (DDR Read) | ECP3-70E/95E | — | 0.225 | — | 0.225 | — | 0.225 | UI |
| $t_{DVEDQ}$ | Data Hold After DQS (DDR Read) | ECP3-70E/95E | 0.64 | — | 0.64 | — | 0.64 | — | UI |
| $t_{DQVBS}$ | Data Valid Before DQS | ECP3-70E/95E | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $t_{DQVAS}$ | Data Valid After DQS | ECP3-70E/95E | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| $f_{MAX\_DDR}$ | DDR Clock Frequency | ECP3-70E/95E | 95 | 200 | 95 | 200 | 95 | 133 | MHz |

# PCI Express Electrical and Timing Characteristics

## AC and DC Characteristics

**Over Recommended Operating Conditions**

| Symbol | Description | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Transmit**[1] | | | | | | |
| UI | Unit interval | | 399.88 | 400 | 400.12 | ps |
| $V_{TX-DIFF\_P-P}$ | Differential peak-to-peak output voltage | | 0.8 | 1.0 | 1.2 | V |
| $V_{TX-DE-RATIO}$ | De-emphasis differential output voltage ratio | | -3 | -3.5 | -4 | dB |
| $V_{TX-CM-AC\_P}$ | RMS AC peak common-mode output voltage | | — | — | 20 | mV |
| $V_{TX-RCV-DETECT}$ | Amount of voltage change allowed during receiver detection | | — | — | 600 | mV |
| $V_{TX-DC-CM}$ | Tx DC common mode voltage | | 0 | — | $V_{CCOB}$ + 5% | V |
| $I_{TX-SHORT}$ | Output short circuit current | $V_{TX-D+}$=0.0V $V_{TX-D-}$=0.0V | — | — | 90 | mA |
| $Z_{TX-DIFF-DC}$ | Differential output impedance | | 80 | 100 | 120 | Ohms |
| $RL_{TX-DIFF}$ | Differential return loss | | 10 | — | — | dB |
| $RL_{TX-CM}$ | Common mode return loss | | 6.0 | — | — | dB |
| $T_{TX-RISE}$ | Tx output rise time | 20 to 80% | 0.125 | — | — | UI |
| $T_{TX-FALL}$ | Tx output fall time | 20 to 80% | 0.125 | — | — | UI |
| $L_{TX-SKEW}$ | Lane-to-lane static output skew for all lanes in port/link | | — | — | 1.3 | ns |
| $T_{TX-EYE}$ | Transmitter eye width | | 0.75 | — | — | UI |
| $T_{TX-EYE-MEDIAN-TO-MAX-JITTER}$ | Maximum time between jitter median and maximum deviation from median | | — | — | 0.125 | UI |
| **Receive**[1, 2] | | | | | | |
| UI | Unit Interval | | 399.88 | 400 | 400.12 | ps |
| $V_{RX-DIFF\_P-P}$ | Differential peak-to-peak input voltage | | 0.34[3] | — | 1.2 | V |
| $V_{RX-IDLE-DET-DIFF\_P-P}$ | Idle detect threshold voltage | | 65 | — | 340[3] | mV |
| $V_{RX-CM-AC\_P}$ | Receiver common mode voltage for AC coupling | | — | — | 150 | mV |
| $Z_{RX-DIFF-DC}$ | DC differential input impedance | | 80 | 100 | 120 | Ohms |
| $Z_{RX-DC}$ | DC input impedance | | 40 | 50 | 60 | Ohms |
| $Z_{RX-HIGH-IMP-DC}$ | Power-down DC input impedance | | 200K | — | — | Ohms |
| $RL_{RX-DIFF}$ | Differential return loss | | 10 | — | — | dB |
| $RL_{RX-CM}$ | Common mode return loss | | 6.0 | — | — | dB |
| $T_{RX-IDLE-DET-DIFF-ENTERTIME}$ | Maximum time required for receiver to recognize and signal an unexpected idle on link | | — | — | — | ms |

1. Values are measured at 2.5 Gbps.
2. Measured with external AC-coupling on the receiver.
3.Not in compliance with PCI Express 1.1 standard.

# SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

## AC and DC Characteristics

***Table 3-19. Transmit***

| Symbol | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $BR_{SDO}$ | Serial data rate | | 270 | — | 2975 | Mbps |
| $T_{JALIGNMENT}$ [2] | Serial output jitter, alignment | 270 Mbps | — | — | 0.20 | UI |
| $T_{JALIGNMENT}$ [2] | Serial output jitter, alignment | 1485 Mbps | — | — | 0.20 | UI |
| $T_{JALIGNMENT}$ [1, 2] | Serial output jitter, alignment | 2970Mbps | — | — | 0.30 | UI |
| $T_{JTIMING}$ | Serial output jitter, timing | 270 Mbps | — | — | 0.20 | UI |
| $T_{JTIMING}$ | Serial output jitter, timing | 1485 Mbps | — | — | 1.0 | UI |
| $T_{JTIMING}$ | Serial output jitter, timing | 2970 Mbps | — | — | 2.0 | UI |

Notes:
1. Timing jitter is measured in accordance with SMPTE RP 184-1996, SMPTE RP 192-1996 and the applicable serial data transmission standard, SMPTE 259M-1997 or SMPTE 292M (proposed). A color bar test pattern is used.The value of $f_{SCLK}$ is 270 MHz or 360 MHz for SMPTE 259M, 540 MHz for SMPTE 344M or 1485 MHz for SMPTE 292M serial data rates. See the Timing Jitter Bandpass section.
2. Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.
3. All Tx jitter is measured at the output of an industry standard cable driver; connection to the cable driver is via a 50 ohm impedance differential signal from the Lattice SERDES device.
4. The cable driver drives: RL=75 ohm, AC-coupled at 270, 1485, or 2970 Mbps, RREFLVL=RREFPRE=4.75kohm 1%.

***Table 3-20. Receive***

| Symbol | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $BR_{SDI}$ | Serial input data rate | | 270 | — | 2970 | Mbps |
| CID | Stream of non-transitions (=Consecutive Identical Digits) | | 7(3G)/26(SMPTE Triple rates) @ 10-12 BER | — | — | Bits |

***Table 3-21. Reference Clock***

| Symbol | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $F_{VCLK}$ | Video output clock frequency | | 27 | — | 74.25 | MHz |
| $DC_V$ | Duty cycle, video clock | | 45 | 50 | 55 | % |

## Pin Information Summary

| Pin Information Summary | | ECP3-17EA | | ECP3-35EA | | | ECP3-70E/EA | | |
|---|---|---|---|---|---|---|---|---|---|
| Pin Type | | 256 ftBGA | 484 fpBGA | 256 ftBGA | 484 fpBGA | 672 fpBGA | 484 fpBGA | 672 fpBGA | 1156 fpBGA |
| General Purpose Inputs/Outputs per Bank | Bank 0 | 26 | 36 | 26 | 42 | 48 | 42 | 60 | 86 |
| | Bank 1 | 14 | 24 | 14 | 36 | 36 | 36 | 48 | 78 |
| | Bank 2 | 6 | 12 | 6 | 24 | 24 | 24 | 34 | 36 |
| | Bank 3 | 18 | 44 | 16 | 54 | 59 | 54 | 59 | 86 |
| | Bank 6 | 20 | 44 | 18 | 63 | 61 | 63 | 67 | 86 |
| | Bank 7 | 19 | 32 | 19 | 36 | 42 | 36 | 48 | 54 |
| | Bank 8 | 24 | 24 | 24 | 24 | 24 | 24 | 24 | 24 |
| General Purpose Inputs per Bank | Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 2 | 2 | 2 | 2 | 4 | 4 | 4 | 8 | 8 |
| | Bank 3 | 0 | 0 | 2 | 4 | 4 | 4 | 12 | 12 |
| | Bank 6 | 0 | 0 | 2 | 4 | 4 | 4 | 12 | 12 |
| | Bank 7 | 4 | 4 | 4 | 4 | 4 | 4 | 8 | 8 |
| | Bank 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| General Purpose Outputs per Bank | Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 6 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Total Single-Ended User I/O | | 133 | 222 | 133 | 295 | 310 | 295 | 380 | 490 |
| VCC | | 6 | 16 | 6 | 16 | 32 | 16 | 32 | 32 |
| VCCAUX | | 4 | 8 | 4 | 8 | 12 | 8 | 12 | 16 |
| VTT | | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 8 |
| VCCA | | 4 | 4 | 4 | 4 | 8 | 4 | 8 | 16 |
| VCCPLL | | 2 | 4 | 2 | 4 | 4 | 4 | 4 | 4 |
| VCCIO | Bank 0 | 2 | 2 | 2 | 2 | 4 | 2 | 4 | 4 |
| | Bank 1 | 2 | 2 | 2 | 2 | 4 | 2 | 4 | 4 |
| | Bank 2 | 2 | 2 | 2 | 2 | 4 | 2 | 4 | 4 |
| | Bank 3 | 2 | 2 | 2 | 2 | 4 | 2 | 4 | 4 |
| | Bank 6 | 2 | 2 | 2 | 2 | 4 | 2 | 4 | 4 |
| | Bank 7 | 2 | 2 | 2 | 2 | 4 | 2 | 4 | 4 |
| | Bank 8 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| VCCJ | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| TAP | | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| GND, GNDIO | | 50 | 98 | 50 | 98 | 139 | 98 | 139 | 233 |
| NC | | 0 | 73 | 0 | 0 | 96 | 0 | 0 | 238 |
| Reserved[1] | | 0 | 2 | 0 | 2 | 2 | 2 | 2 | 2 |
| SERDES | | 26 | 26 | 26 | 26 | 26 | 26 | 52 | 78 |
| Miscellaneous Pins | | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| Total Bonded Pins | | 256 | 484 | 256 | 484 | 672 | 484 | 672 | 1156 |

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|
| LFE3-70E-6FN484C[1] | 1.2V | -6 | Lead-Free fpBGA | 484 | COM | 67 |
| LFE3-70E-7FN484C[1] | 1.2V | -7 | Lead-Free fpBGA | 484 | COM | 67 |
| LFE3-70E-8FN484C[1] | 1.2V | -8 | Lead-Free fpBGA | 484 | COM | 67 |
| LFE3-70E-6FN672C[1] | 1.2V | -6 | Lead-Free fpBGA | 672 | COM | 67 |
| LFE3-70E-7FN672C[1] | 1.2V | -7 | Lead-Free fpBGA | 672 | COM | 67 |
| LFE3-70E-8FN672C[1] | 1.2V | -8 | Lead-Free fpBGA | 672 | COM | 67 |
| LFE3-70E-6FN1156C[1] | 1.2V | -6 | Lead-Free fpBGA | 1156 | COM | 67 |
| LFE3-70E-7FN1156C[1] | 1.2V | -7 | Lead-Free fpBGA | 1156 | COM | 67 |
| LFE3-70E-8FN1156C[1] | 1.2V | -8 | Lead-Free fpBGA | 1156 | COM | 67 |

1.This device has associated errata. View www.latticesemi.com/documents/ds1021.zip for a description of the errata.

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|
| LFE3-95EA-6FN484C | 1.2V | -6 | Lead-Free fpBGA | 484 | COM | 92 |
| LFE3-95EA-7FN484C | 1.2V | -7 | Lead-Free fpBGA | 484 | COM | 92 |
| LFE3-95EA-8FN484C | 1.2V | -8 | Lead-Free fpBGA | 484 | COM | 92 |
| LFE3-95EA-6FN672C | 1.2V | -6 | Lead-Free fpBGA | 672 | COM | 92 |
| LFE3-95EA-7FN672C | 1.2V | -7 | Lead-Free fpBGA | 672 | COM | 92 |
| LFE3-95EA-8FN672C | 1.2V | -8 | Lead-Free fpBGA | 672 | COM | 92 |
| LFE3-95EA-6FN1156C | 1.2V | -6 | Lead-Free fpBGA | 1156 | COM | 92 |
| LFE3-95EA-7FN1156C | 1.2V | -7 | Lead-Free fpBGA | 1156 | COM | 92 |
| LFE3-95EA-8FN1156C | 1.2V | -8 | Lead-Free fpBGA | 1156 | COM | 92 |

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|
| LFE3-95E-6FN484C[1] | 1.2V | -6 | Lead-Free fpBGA | 484 | COM | 92 |
| LFE3-95E-7FN484C[1] | 1.2V | -7 | Lead-Free fpBGA | 484 | COM | 92 |
| LFE3-95E-8FN484C[1] | 1.2V | -8 | Lead-Free fpBGA | 484 | COM | 92 |
| LFE3-95E-6FN672C[1] | 1.2V | -6 | Lead-Free fpBGA | 672 | COM | 92 |
| LFE3-95E-7FN672C[1] | 1.2V | -7 | Lead-Free fpBGA | 672 | COM | 92 |
| LFE3-95E-8FN672C[1] | 1.2V | -8 | Lead-Free fpBGA | 672 | COM | 92 |
| LFE3-95E-6FN1156C[1] | 1.2V | -6 | Lead-Free fpBGA | 1156 | COM | 92 |
| LFE3-95E-7FN1156C[1] | 1.2V | -7 | Lead-Free fpBGA | 1156 | COM | 92 |
| LFE3-95E-8FN1156C[1] | 1.2V | -8 | Lead-Free fpBGA | 1156 | COM | 92 |

1.This device has associated errata. View www.latticesemi.com/documents/ds1021.zip for a description of the errata.

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|
| LFE3-150EA-6FN672C | 1.2V | -6 | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-7FN672C | 1.2V | -7 | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-8FN672C | 1.2V | -8 | Lead-Free fpBGA | 672 | COM | 149 |
| LFE3-150EA-6FN1156C | 1.2V | -6 | Lead-Free fpBGA | 1156 | COM | 149 |
| LFE3-150EA-7FN1156C | 1.2V | -7 | Lead-Free fpBGA | 1156 | COM | 149 |
| LFE3-150EA-8FN1156C | 1.2V | -8 | Lead-Free fpBGA | 1156 | COM | 149 |

# LatticeECP3 Family Data Sheet Supplemental Information



## For Further Information

A variety of technical notes for the LatticeECP3 family are available on the Lattice website at www.latticesemi.com.

- TN1169, LatticeECP3 sysCONFIG Usage Guide
- TN1176, LatticeECP3 SERDES/PCS Usage Guide
- TN1177, LatticeECP3 sysIO Usage Guide
- TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide
- TN1179, LatticeECP3 Memory Usage Guide
- TN1180, LatticeECP3 High-Speed I/O Interface
- TN1181, Power Consumption and Management for LatticeECP3 Devices
- TN1182, LatticeECP3 sysDSP Usage Guide
- TN1184, LatticeECP3 Soft Error Detection (SED) Usage Guide
- TN1189, LatticeECP3 Hardware Checklist

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com

| Date | Version | Section | Change Summary |
|---|---|---|---|
| November 2009 (cont.) | 01.5 (cont.) | Architecture (cont.) | Updated Table 2-13, SERDES Standard Support to include SONET/ SDH and updated footnote 2. |
| | | DC and Switching Characterisitcs | Added footnote to ESD Performance table. |
| | | | Updated SERDES Power Supply Requirements table and footnotes. |
| | | | Updated Maximum I/O Buffer Speed table. |
| | | | Updated Pin-to-Pin Peformance table. |
| | | | Updated sysCLOCK PLL Timing table. |
| | | | Updated DLL timing table. |
| | | | Updated High-Speed Data Transmitter tables. |
| | | | Updated High-Speed Data Receiver table. |
| | | | Updated footnote for Receiver Total Jitter Tolerance Specification table. |
| | | | Updated Periodic Receiver Jitter Tolerance Specification table. |
| | | | Updated SERDES External Reference Clock Specification table. |
| | | | Updated PCI Express Electrical and Timing AC and DC Characteristics. |
| | | | Deleted Reference Clock table for PCI Express Electrical and Timing AC and DC Characteristics. |
| | | | Updated SMPTE AC/DC Characteristics Transmit table. |
| | | | Updated Mini LVDS table. |
| | | | Updated RSDS table. |
| | | | Added Supply Current (Standby) table for EA devices. |
| | | | Updated Internal Switching Characteristics table. |
| | | | Updated Register-to-Register Performance table. |
| | | | Added HDMI Electrical and Timing Characteristics data. |
| | | | Updated Family Timing Adders table. |
| | | | Updated sysCONFIG Port Timing Specifications table. |
| | | | Updated Recommended Operating Conditions table. |
| | | | Updated Hot Socket Specifications table. |
| | | | Updated Single-Ended DC table. |
| | | | Updated TRLVDS table and figure. |
| | | | Updated Serial Data Input Specifications table. |
| | | | Updated HDMI Transmit and Receive table. |
| | | Ordering Information | Added LFE3-150EA “TW” devices and footnotes to the Commercial and Industrial tables. |
| March 2010 | 01.6 | Architecture | Added Read-Before-Write information. |
| | | DC and Switching Characteristics | Added footnote #6 to Maximum I/O Buffer Speed table. |
| | | | Corrected minimum operating conditions for input and output differential voltages in the Point-to-Point LVDS table. |
| | | Pinout Information | Added pin information for the LatticeECP3-70EA and LatticeECP3-95EA devices. |
| | | Ordering Information | Added ordering part numbers for the LatticeECP3-70EA and LatticeECP3-95EA devices. |
| | | | Removed dual mark information. |