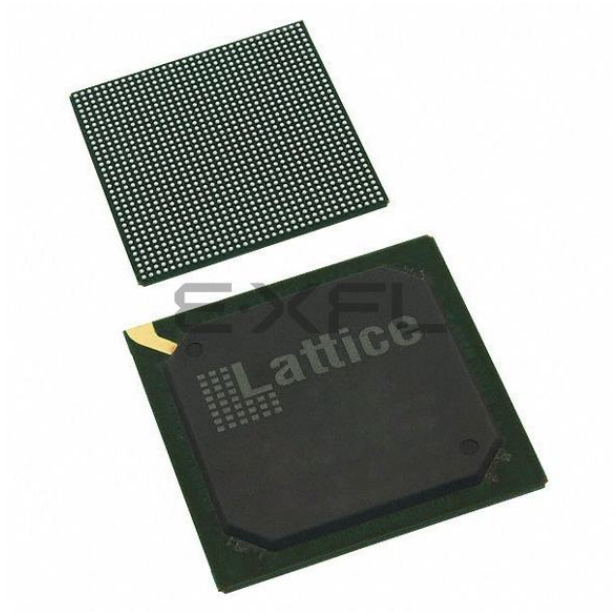
Lattice Semiconductor Corporation - LFE3-95E-7FN1156C Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

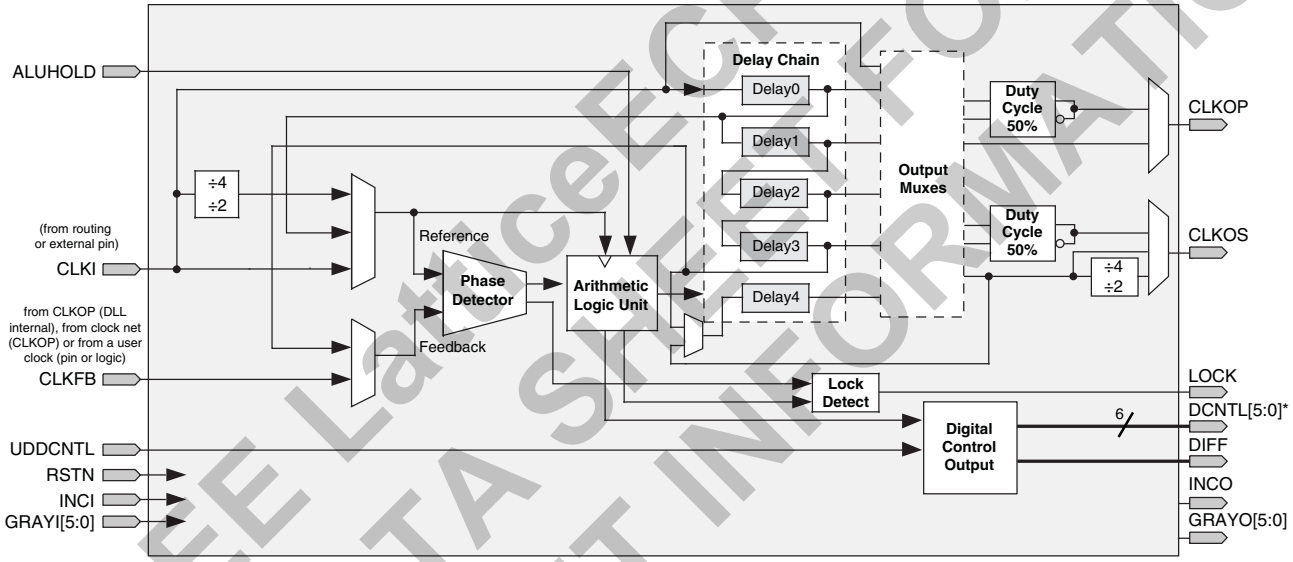
Details	
Product Status	Obsolete
Number of LABs/CLBs	11500
Number of Logic Elements/Cells	92000
Total RAM Bits	4526080
Number of I/O	490
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95e-7fn1156c

chain in order to better match the reference and feedback signals. This digital code from the ALU is also transmitted via the Digital Control bus (DCNTL) bus to its associated Slave Delay lines (two per DLL). The ALUHOLD input allows the user to suspend the ALU output at its current value. The UDDCNTL signal allows the user to latch the current value on the DCNTL bus.

The DLL has two clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine delay shift and divider blocks to allow this output to be further modified, if required. The fine delay shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. Both the CLKOS and CLKOP outputs are available with optional duty cycle correction. Divide by two and divide by four frequencies are available at CLKOS. The LOCK output signal is asserted when the DLL is locked. Figure 2-5 shows the DLL block diagram and Table 2-5 provides a description of the DLL inputs and outputs.

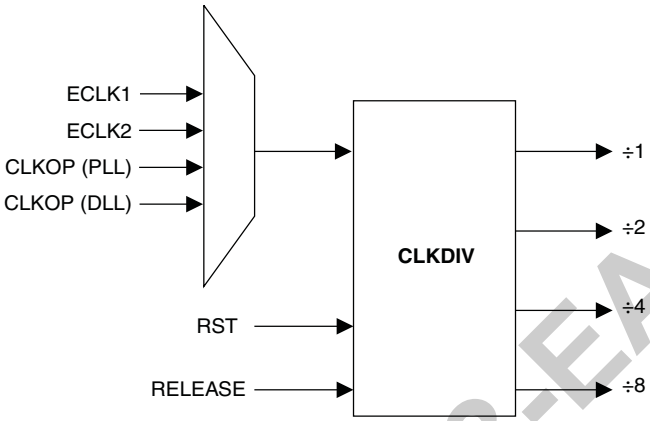
The user can configure the DLL for many common functions such as time reference delay mode and clock injection removal mode. Lattice provides primitives in its design tools for these functions.

Figure 2-5. Delay Locked Loop Diagram (DLL)



* This signal is not user accessible. This can only be used to feed the slave delay line.

Figure 2-8. Clock Divider Connections



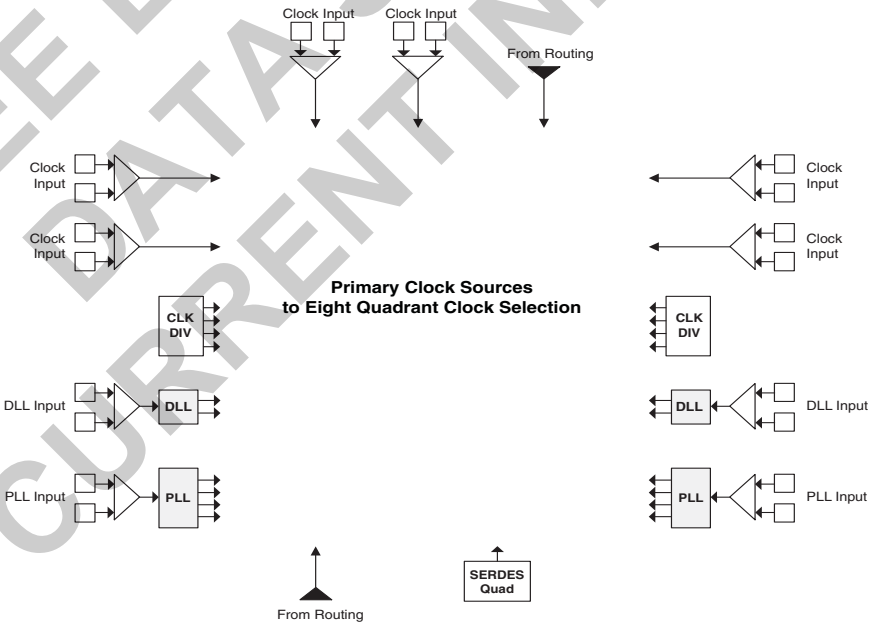
Clock Distribution Network

LatticeECP3 devices have eight quadrant-based primary clocks and eight secondary clock/control sources. Two high performance edge clocks are available on the top, left, and right edges of the device to support high speed interfaces. These clock sources are selected from external I/Os, the sysCLOCK PLLs, DLLs or routing. These clock sources are fed throughout the chip via a clock distribution system.

Primary Clock Sources

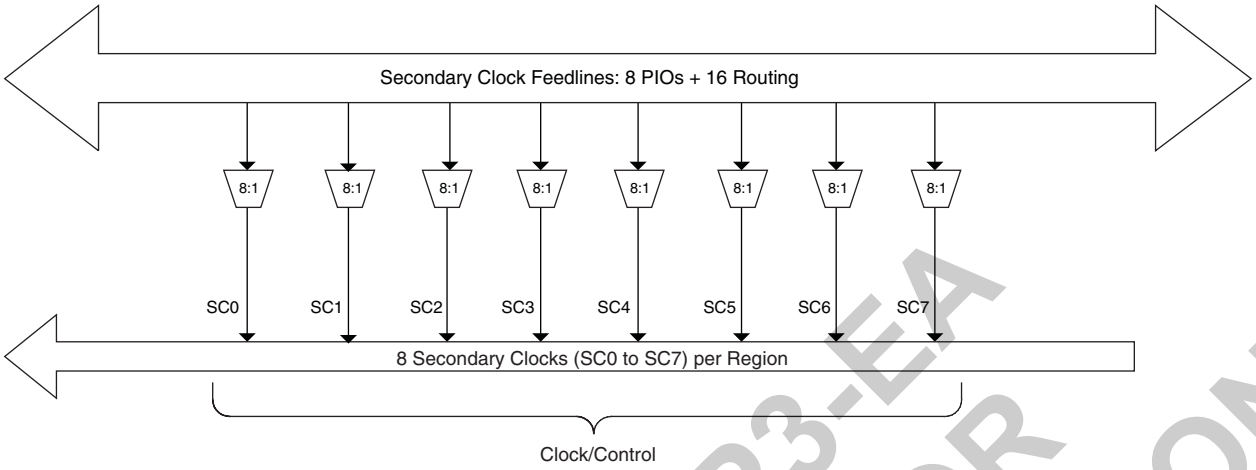
LatticeECP3 devices derive clocks from six primary source types: PLL outputs, DLL outputs, CLKDIV outputs, dedicated clock inputs, routing and SERDES Quads. LatticeECP3 devices have two to ten sysCLOCK PLLs and two DLLs, located on the left and right sides of the device. There are six dedicated clock inputs: two on the top side, two on the left side and two on the right side of the device. Figures 2-9, 2-10 and 2-11 show the primary clock sources for LatticeECP3 devices.

Figure 2-9. Primary Clock Sources for LatticeECP3-17



Note: Clock inputs can be configured in differential or single-ended mode.

Figure 2-16. Per Region Secondary Clock Selection



Slice Clock Selection

Figure 2-17 shows the clock selections and Figure 2-18 shows the control selections for Slice0 through Slice2. All the primary clocks and seven secondary clocks are routed to this clock selection mux. Other signals can be used as a clock input to the slices via routing. Slice controls are generated from the secondary clocks/controls or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-17. Slice0 through Slice2 Clock Selection

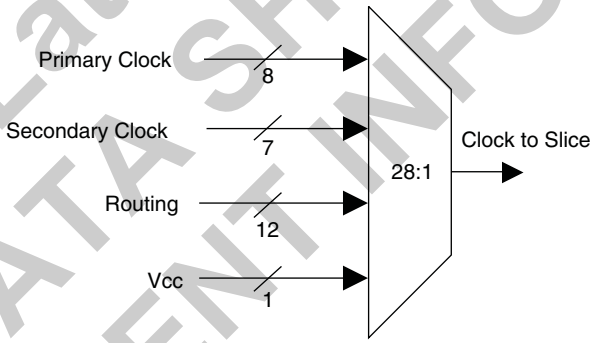
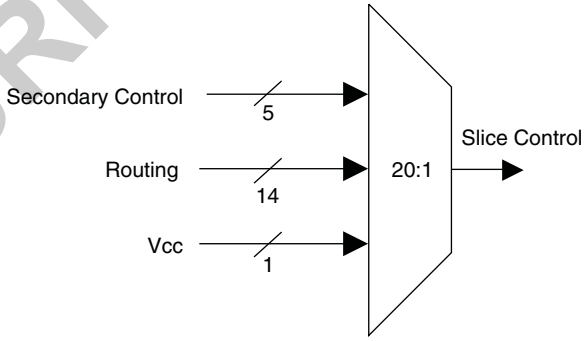


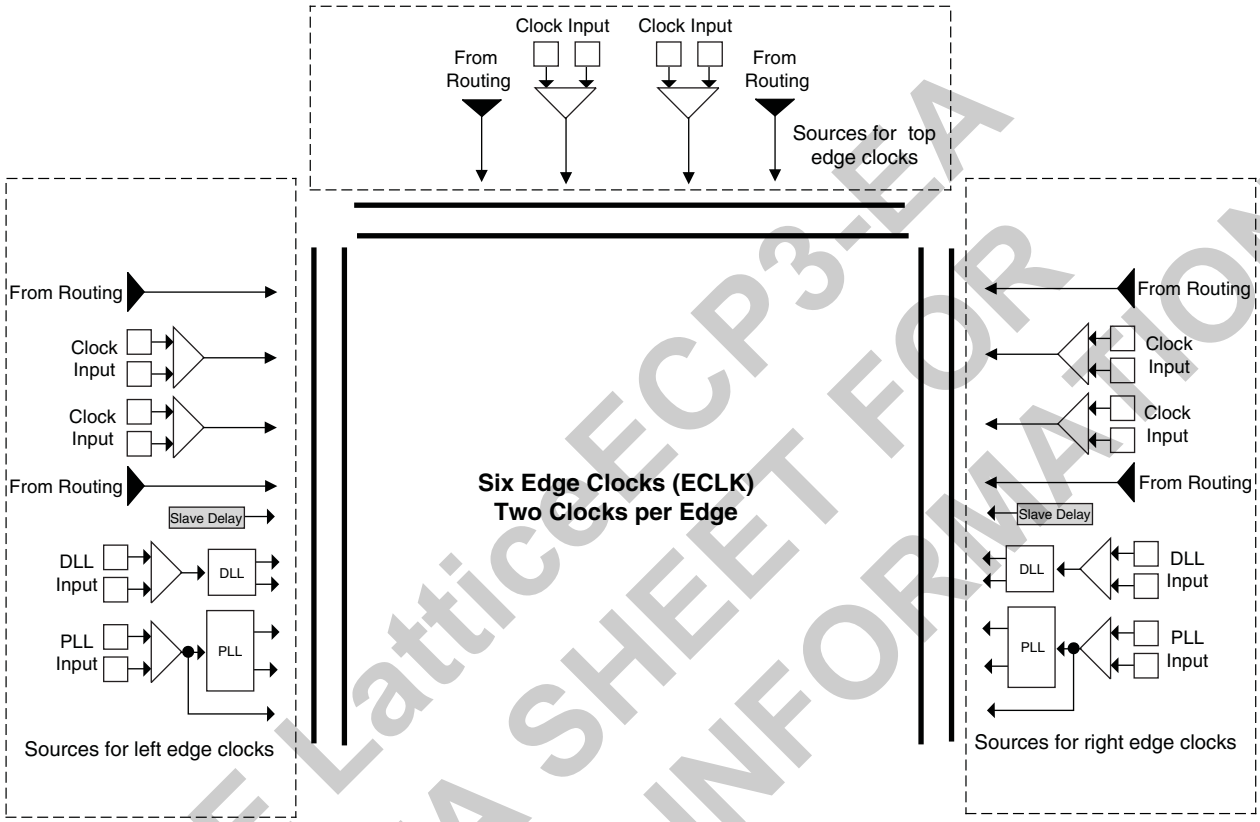
Figure 2-18. Slice0 through Slice2 Control Selection



Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs, DLLs, Slave Delay and clock dividers as shown in Figure 2-19.

Figure 2-19. Edge Clock Sources



Notes:
1. Clock inputs can be configured in differential or single ended mode.
2. The two DLLs can also drive the two top edge clocks.
3. The top left and top right PLL can also drive the two top edge clocks.

Edge Clock Routing

LatticeECP3 devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are six edge clocks per device: two edge clocks on each of the top, left, and right edges. Different PLL and DLL outputs are routed to the two muxes on the left and right sides of the device. In addition, the CLKINDEL signal (generated from the DLL Slave Delay Line block) is routed to all the edge clock muxes on the left and right sides of the device. Figure 2-20 shows the selection muxes for these clocks.

Figure 2-20. Sources of Edge Clock (Left and Right Edges)

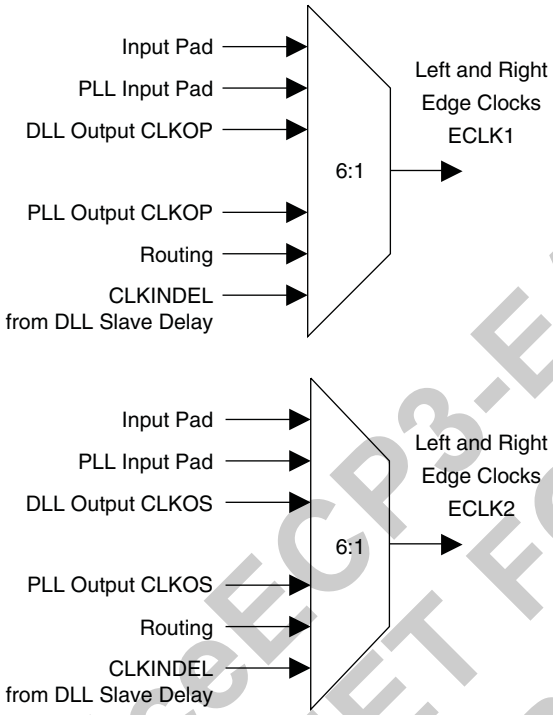
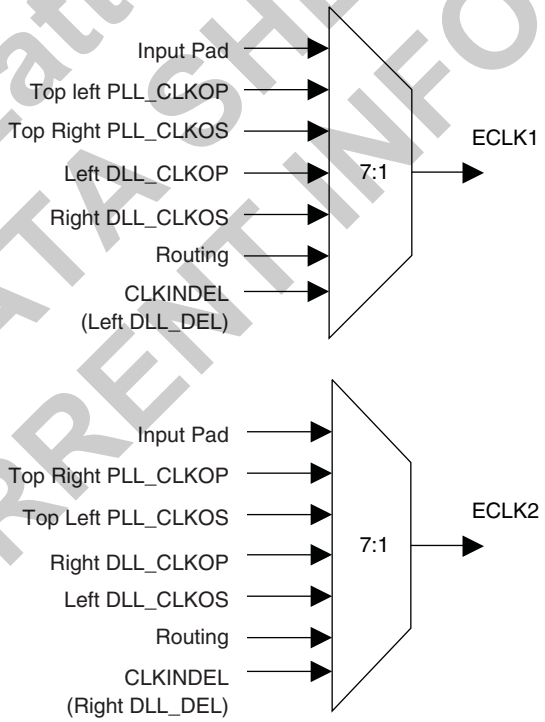


Figure 2-21. Sources of Edge Clock (Top Edge)

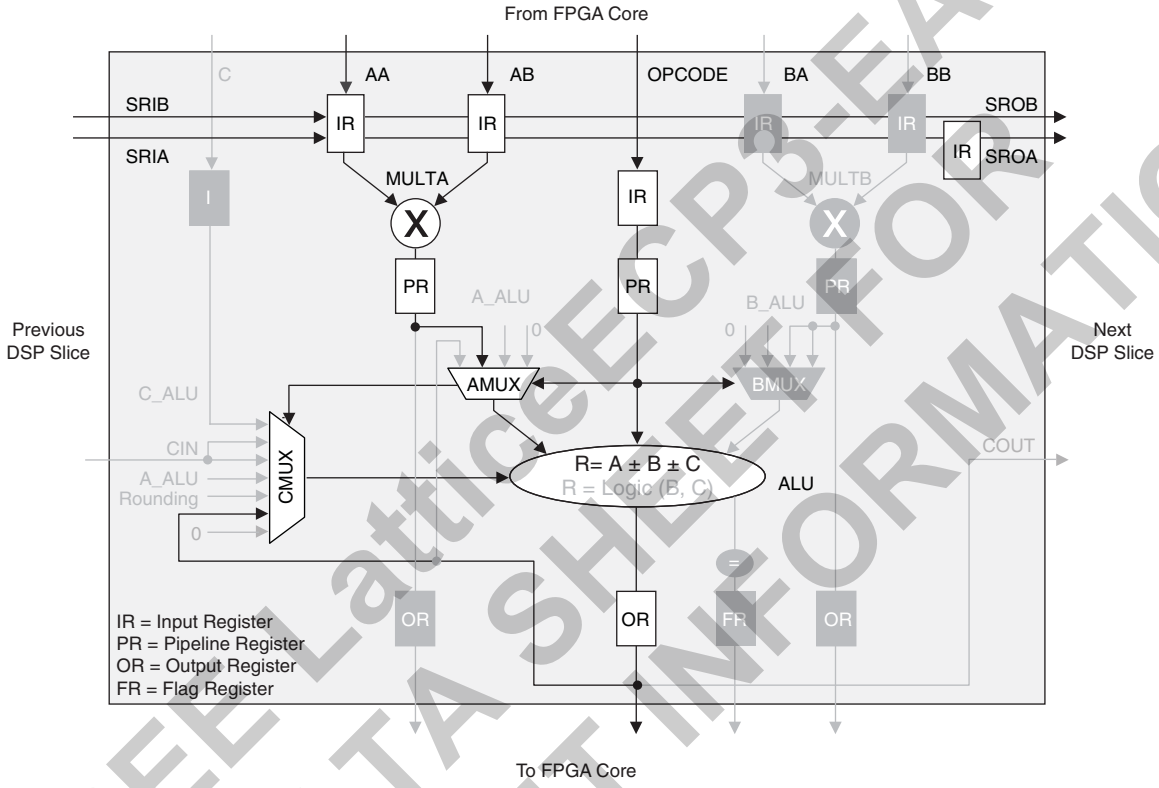


The edge clocks have low injection delay and low skew. They are used to clock the I/O registers and thus are ideal for creating I/O interfaces with a single clock signal and a wide data bus. They are also used for DDR Memory or Generic DDR interfaces.

MAC DSP Element

In this case, the two operands, AA and AB, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The ALU is configured as the accumulator in the sysDSP slice in the LatticeECP3 family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-27 shows the MAC sysDSP element.

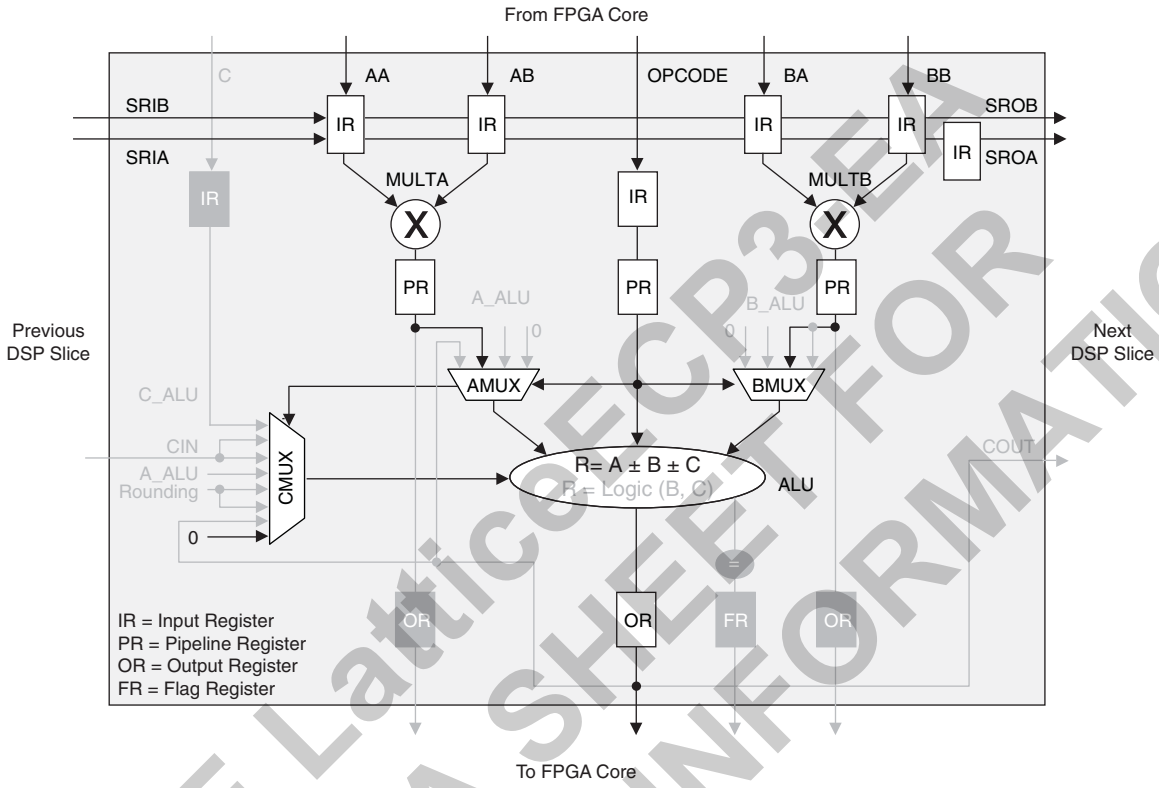
Figure 2-27. MAC DSP Element



MULTADDSUB DSP Element

In this case, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB. The user can enable the input, output and pipeline registers. Figure 2-29 shows the MULTADDSUB sysDSP element.

Figure 2-29. MULTADDSUB



ALU Flags

The sysDSP slice provides a number of flags from the ALU including:

- Equal to zero (EQZ)
- Equal to zero with mask (EQZM)
- Equal to one with mask (EQOM)
- Equal to pattern with mask (EQPAT)
- Equal to bit inverted pattern with mask (EQPATB)
- Accumulator Overflow (OVER)
- Accumulator Underflow (UNDER)
- Either over or under flow supporting LatticeECP2 legacy designs (OVERUNDER)

Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every sysDSP slice. From four clock sources (CLK0, CLK1, CLK2, and CLK3) one clock is selected for each input register, pipeline register and output register. Similarly Clock Enable (CE) and Reset (RST) are selected at each input register, pipeline register and output register.

Resources Available in the LatticeECP3 Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP3 family. Table 2-10 shows the maximum available EBR RAM Blocks in each LatticeECP3 device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Table 2-9. Maximum Number of DSP Slices in the LatticeECP3 Family

Device	DSP Slices	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
ECP3-17	12	48	24	6
ECP3-35	32	128	64	16
ECP3-70	64	256	128	32
ECP3-95	64	256	128	32
ECP3-150	160	640	320	80

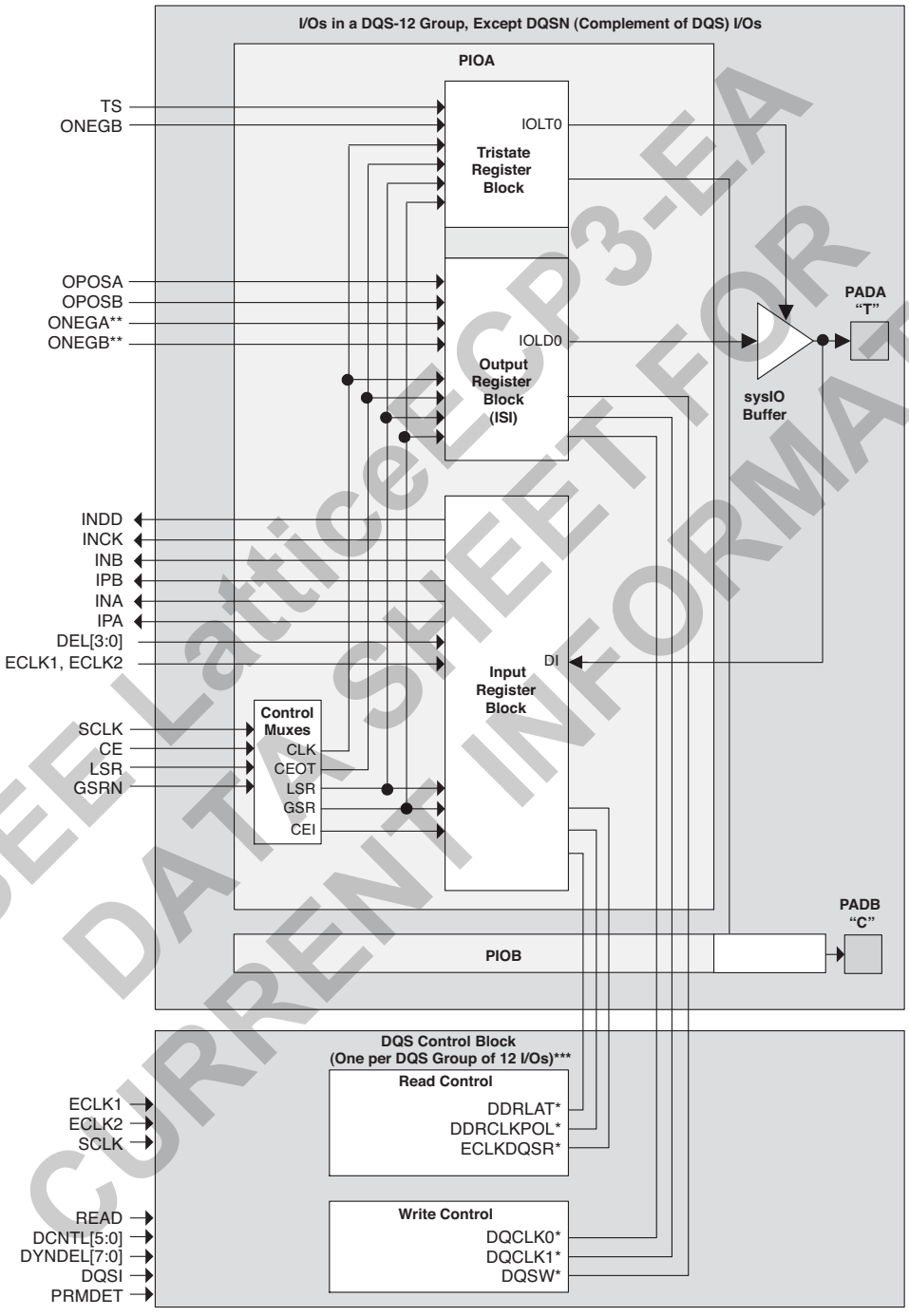
Table 2-10. Embedded SRAM in the LatticeECP3 Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
ECP3-17	38	700
ECP3-35	72	1327
ECP3-70	240	4420
ECP3-95	240	4420
ECP3-150	372	6850

Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O buffers as shown in Figure 2-32. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysI/O buffer and receives input from the buffer. Table 2-11 provides the PIO signal list.

Figure 2-32. PIC Diagram



* Signals are available on left/right/top edges only.
** Signals are available on the left and right sides only
*** Selected PIO.

sysI/O Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS33[2]	3.135	3.3	3.465	—	—	—
LVCMOS25[2]	2.375	2.5	2.625	—	—	—
LVCMOS18	1.71	1.8	1.89	—	—	—
LVCMOS15	1.425	1.5	1.575	—	—	—
LVCMOS12[2]	1.14	1.2	1.26	—	—	—
LVTTL33[2]	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
SSTL15[3]	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, II[2]	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I, II[2]	2.375	2.5	2.625	1.15	1.25	1.35
SSTL33_I, II[2]	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15_I[2]	1.425	1.5	1.575	0.68	0.75	0.9
HSTL18_I, II[2]	1.71	1.8	1.89	0.816	0.9	1.08
LVDS25[2]	2.375	2.5	2.625	—	—	—
MLVDS25[1]	2.375	2.5	2.625	—	—	—
LVPECL33[1, 2]	3.135	3.3	3.465	—	—	—
Mini LVDS	—	—	—	—	—	—
BLVDS25[1, 2]	2.375	2.5	2.625	—	—	—
RSDS25[1, 2]	2.375	2.5	2.625	—	—	—
RSDS25E[1, 2]	2.375	2.5	2.625	—	—	—
TRLVDS	3.14	3.3	3.47	—	—	—
PPLVDS	3.14/2.25	3.3/2.5	3.47/2.75	—	—	—
SSTL15D	1.43	1.5	1.57	—	—	—
SSTL18D_I[2], II[2]	1.71	1.8	1.89	—	—	—
SSTL25D_ I[2], II[2]	2.375	2.5	2.625	—	—	—
SSTL33D_ I[2], II[2]	3.135	3.3	3.465	—	—	—
HSTL15D_ I[2]	1.425	1.5	1.575	—	—	—
HSTL18D_ I[2], II[2]	1.71	1.8	1.89	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.
2. For input voltage compatibility, refer to the "Mixed Voltage Support" section of TN1177, LatticeECP3 sysIO Usage Guide.

LatticeECP3 External Switching Characteristics (Continued)[1, 2]

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	ECP3-70E/95E	—	500	—	420	—	375	Mhz
General I/O Pin Parameters Using Dedicated Clock Input Primary Clock with PLL with Clock Injection Removal Setting[2]									
t_{COPLL}	Clock to Output - PIO Output Register	ECP3-150EA	—	2.5	—	2.7	—	3.1	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	ECP3-150EA	0.6	—	0.6	—	0.7	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	ECP3-150EA	0.9	—	1.0	—	1.1	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-150EA	1.5	—	1.6	—	1.8	—	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-150EA	—	0.1	—	0.1	—	0.1	ns
t_{COPLL}	Clock to Output - PIO Output Register	ECP3-70E/95E	—	2.2	—	2.3	—	2.5	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	ECP3-70E/95E	0.6	—	0.7	—	0.8	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	ECP3-70E/95E	0.9	—	1.1	—	1.3	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	ECP3-70E/95E	1.6	—	1.9	—	2.1	—	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	ECP3-70E/95E	0.0	—	0.0	—	0.0	—	ns

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDR									
Generic DDRX1 Inputs with Clock and Data (>10 Bits Wide) Centered at Pin (GDDRX1_RX.SCLK.Centered) Using PCLK Pin for Clock Input									
Data Left, Right and Top Sides & Clock Left, Right and Top Sides									
t_{SUGDDR}	Data Setup Before CLK	ECP3-150EA		—		—		—	ps
t_{HGDDR}	Data Hold After CLK	ECP3-150EA		—		—		—	ps
f_{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-150EA	—		—		—		MHz
Generic DDRX1 Inputs with Clock in the Center of Data Window, without DLL (GDDRX1_RX.ECLK.Centered)									
t_{SUGDDR}	Data Setup Before CLK	ECP3-70E/95E	515	—	515	—	515	—	ps
t_{HOGDDR}	Data Hold After CLK	ECP3-70E/95E	515	—	515	—	515	—	ps
f_{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-70E/95E	—	250	—	250	—	250	MHz
Generic DDRX1 Inputs with Clock and Data (> 10 Bits Wide) Aligned at Pin (GDDRX1_RX.SCLK.Aligned) using DLL-CLKIN Pin for Clock Input									
Data Left, Right and Top Sides & Clock Left and Right Sides									
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-150EA	—		—		—		UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-150EA		—		—		—	UI
f_{MAX_GDDR}	DDRX1 Clock Frequency	ECP3-150EA	—		—		—		MHz
Generic DDRX1 Inputs with Clock and Data Aligned, with DLL (GDDRX1_RX.ECLK.Aligned)									
$t_{DVACLKGDDR}$	Data Setup Before CLK	ECP3-70E/95E	—	0.235	—	0.235	—	0.235	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	ECP3-70E/95E	0.765	—	0.765	—	0.765	—	UI

LatticeECP3 External Switching Characteristics (Continued)[1, 2]

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Output with Clock and Data (> 10 Bits Wide) Aligned at Pin (GDDRX2_TX.ECLK.Aligned)									
Left and Right Sides									
$t_{DIBGDDR}$	Data Setup Before CLK	ECP3-150EA	—		—		—		ps
$t_{DIAGDDR}$	Data Hold After CLK	ECP3-150EA	—		—		—		ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	—		—		—		MHz
Generic DDRX2 Outputs with Clock and Data Edges Aligned, Without PLL 90-degree shifted clock output[5] (GDDRX2_TX.Aligned)									
$t_{DIBGDDR}$	Data Invalid Before Clock	ECP3-70E/95E	—	200	—	225	—	250	ps
$t_{DIAGDDR}$	Data Invalid After Clock	ECP3-70E/95E	—	200	—	225	—	250	ps
f_{MAX_GDDR}	DDR/DDRX2 Clock Frequency[8]	ECP3-70E/95E	—	500	—	420	—	375	MHz
Generic DDRX2 Output with Clock and Data (> 10 Bits Wide) Centered at Pin Using DQSDLL (GDDRX2_TX.DQS-DLL.Centered)									
Left and Right Sides									
$t_{DVBGDDR}$	Data Valid Before CLK	ECP3-150EA		—		—		—	ns
$t_{DVAGDDR}$	Data Valid After CLK	ECP3-150EA		—		—		—	ns
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	—		—		—		ns
Generic DDRX2 Output with Clock and Data (> 10 Bits Wide) Centered at Pin Using PLL (GDDRX2_TX.PLL.Centered)									
Left and Right Sides									
$t_{DVBGDDR}$	Data Valid Before CLK	ECP3-150EA		—		—		—	ns
$t_{DVAGDDR}$	Data Valid After CLK	ECP3-150EA		—		—		—	ns
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	—		—		—		ns
Generic DDRX2 Outputs with Clock Edge in the Center of Data Window, with PLL 90-degree Shifted Clock Output[6] (GDDRX2_TX.PLL.Centered)									
$t_{DVBGDDR}$	Data Valid Before CLK	ECP3-70E/95E	300	—	370	—	417	—	ps
$t_{DVAGDDR}$	Data Valid After CLK	ECP3-70E/95E	300	—	370	—	417	—	ps
f_{MAX_GDDR}	DDR/DDRX2 Clock Frequency[8]	ECP3-70E/95E	—	500	—	420	—	375	MHz

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Memory Interface									
DDR/DDR2 SDRAM I/O Pin Parameters (Input Data are Strobe Edge Aligned, Output Strobe Edge is Data Centered)[4]									
t_{DVADQ}	Data Valid After DQS (DDR Read)	ECP3-150EA	—	0.225	—	0.225	—	0.225	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	ECP3-150EA	0.64	—	0.64	—	0.64	—	UI
t_{DQVBS}	Data Valid Before DQS	ECP3-150EA	0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Data Valid After DQS	ECP3-150EA	0.25	—	0.25	—	0.25	—	UI
f_{MAX_DDR}	DDR Clock Frequency	ECP3-150EA	95	200	95	200	95	166	MHz
f_{MAX_DDR2}	DDR2 clock frequency	ECP3-150EA	133	266	133	200	133	166	MHz
t_{DVADQ}	Data Valid After DQS (DDR Read)	ECP3-70E/95E	—	0.225	—	0.225	—	0.225	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	ECP3-70E/95E	0.64	—	0.64	—	0.64	—	UI
t_{DQVBS}	Data Valid Before DQS	ECP3-70E/95E	0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Data Valid After DQS	ECP3-70E/95E	0.25	—	0.25	—	0.25	—	UI
f_{MAX_DDR}	DDR Clock Frequency	ECP3-70E/95E	95	200	95	200	95	133	MHz

LatticeECP3 Internal Switching Characteristics[1, 2] (Continued)

Over Recommended Commercial Operating Conditions

Parameter	Description	-8		-7		-6		Units.
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{HWREN_EBR}	Hold Write/Read Enable to PFU Memory	0.141	—	0.145	—	0.149	—	ns
t_{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.087		0.096		0.104		ns
t_{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.066		-0.080		-0.094		ns
t_{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	-0.071		-0.070		-0.068		ns
t_{HBE_EBR}	Byte Enable Hold Time to EBR Output Register	0.118		0.098		0.077		ns
DSP Block Timing[3]								
t_{SUI_DSP}	Input Register Setup Time	0.32	—	0.36	—	0.39	—	ns
t_{HI_DSP}	Input Register Hold Time	-0.17	—	-0.19	—	-0.21	—	ns
t_{SUP_DSP}	Pipeline Register Setup Time	2.23	—	2.30	—	2.37	—	ns
t_{HP_DSP}	Pipeline Register Hold Time	-1.02	—	-1.09	—	-1.15	—	ns
t_{SUO_DSP}	Output Register Setup Time	3.09	—	3.22	—	3.34	—	ns
t_{HO_DSP}	Output Register Hold Time	-1.67	—	-1.76	—	-1.84	—	ns
t_{COI_DSP}	Input Register Clock to Output Time	—	3.68	—	4.03	—	4.38	ns
t_{COP_DSP}	Pipeline Register Clock to Output Time	—	1.30	—	1.47	—	1.64	ns
t_{COO_DSP}	Output Register Clock to Output Time	—	0.58	—	0.60	—	0.62	ns
t_{SUOPT_DSP}	Opcode Register Setup Time	0.31	—	0.35	—	0.39	—	ns
t_{HOPT_DSP}	Opcode Register Hold Time	-0.20	—	-0.24	—	-0.27	—	ns
t_{SUDATA_DSP}	Cascade_data through ALU to Output Register Setup Time	1.55	—	1.67	—	1.78	—	ns
t_{HPDATA_DSP}	Cascade_data through ALU to Output Register Hold Time	-0.44	—	-0.53	—	-0.61	—	ns

1. Internal parameters are characterized but not tested on every device.
2. Commercial timing numbers are shown. Industrial timing numbers are typically slower and can be extracted from the ispLEVER software.
3. DSP slice is configured in Multiply Add/Sub 18x18 mode.
4. The output register is in Flip-flop mode.

LatticeECP3 Family Timing Adders[1, 2, 3, 4, 5] (Continued)

Over Recommended Commercial Operating Conditions

Buffer Type	Description	-8	-7	-6	Units
RSDS25	RSDS, VCCIO = 2.5V	0.05	0.10	0.16	ns
PPLVDS	Point-to-Point LVDS, Emulated, VCCIO = 2.5V	-0.10	-0.05	0.01	ns
LVPECL33	LVPECL, Emulated, VCCIO = 3.0V	-0.02	-0.04	-0.06	ns
HSTL18_I	HSTL_18 class I 8mA drive, VCCIO = 1.8V	-0.19	-0.16	-0.12	ns
HSTL18_II	HSTL_18 class II, VCCIO = 1.8V	-0.30	-0.28	-0.25	ns
HSTL18D_I	Differential HSTL 18 class I 8mA drive	-0.19	-0.16	-0.12	ns
HSTL18D_II	Differential HSTL 18 class II	-0.30	-0.28	-0.25	ns
HSTL15_I	HSTL_15 class I 4mA drive, VCCIO = 1.5V	-0.22	-0.19	-0.16	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	-0.22	-0.19	-0.16	ns
SSTL33_I	SSTL_3 class I, VCCIO = 3.0V	0.08	0.13	0.19	ns
SSTL33_II	SSTL_3 class II, VCCIO = 3.0V	-0.20	-0.17	-0.14	ns
SSTL33D_I	Differential SSTL_3 class I	0.08	0.13	0.18	ns
SSTL33D_II	Differential SSTL_3 class II	-0.20	-0.17	-0.14	ns
SSTL25_I	SSTL_2 class I 8mA drive, VCCIO = 2.5V	-0.06	-0.02	0.02	ns
SSTL25_II	SSTL_2 class II 16mA drive, VCCIO = 2.5V	-0.19	-0.15	-0.12	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.06	-0.02	0.02	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.19	-0.15	-0.12	ns
SSTL18_I	SSTL_1.8 class I, VCCIO = 1.8V	-0.14	-0.10	-0.07	ns
SSTL18_II	SSTL_1.8 class II 8mA drive, VCCIO = 1.8V	-0.20	-0.17	-0.14	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.14	-0.10	-0.07	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.20	-0.17	-0.14	ns
SSTL15	SSTL_1.5, VCCIO = 1.5V	0.07	0.08	0.08	ns
SSTL15D	Differential SSTL_15	0.07	0.08	0.08	ns
LVTTL33_4mA	LVTTL 4mA drive, VCCIO = 3.0V	0.21	0.23	0.25	ns
LVTTL33_8mA	LVTTL 8mA drive, VCCIO = 3.0V	0.09	0.09	0.10	ns
LVTTL33_12mA	LVTTL 12mA drive, VCCIO = 3.0V	0.02	0.03	0.03	ns
LVTTL33_16mA	LVTTL 16mA drive, VCCIO = 3.0V	0.12	0.13	0.13	ns
LVTTL33_20mA	LVTTL 20mA drive, VCCIO = 3.0V	0.08	0.08	0.09	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, fast slew rate	0.21	0.23	0.25	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, fast slew rate	0.09	0.09	0.10	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, fast slew rate	0.02	0.03	0.03	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, fast slew rate	0.12	0.13	0.13	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, fast slew rate	0.08	0.08	0.09	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, fast slew rate	0.12	0.12	0.12	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, fast slew rate	0.05	0.05	0.05	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, fast slew rate	0.08	0.08	0.08	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, fast slew rate	0.04	0.04	0.04	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, fast slew rate	0.08	0.09	0.09	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, fast slew rate	0.02	0.01	0.01	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, fast slew rate	-0.03	-0.03	-0.03	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, fast slew rate	0.03	0.03	0.03	ns

SERDES External Reference Clock

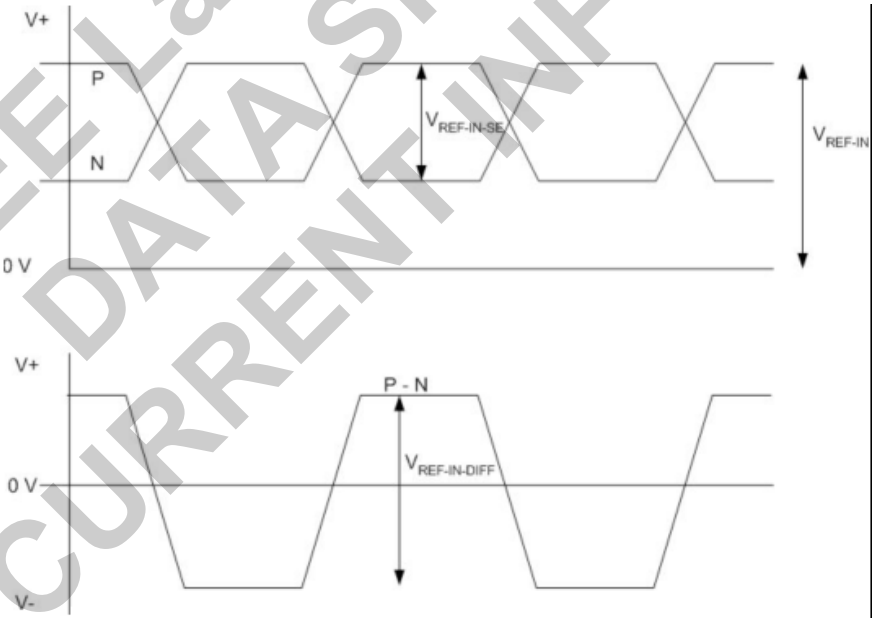
The external reference clock selection and its interface are a critical part of system applications for this product. Table 3-12 specifies reference clock requirements, over the full range of operating conditions.

Table 3-12. External Reference Clock Specification (refclkp/refclkn)

Symbol	Description	Min.	Typ.	Max.	Units
F_{REF}	Frequency range	15	—	320	MHz
$F_{REF-PPM}$	Frequency tolerance[4]	-1000	—	1000	ppm
$V_{REF-IN-SE}$	Input swing, single-ended clock[1]	200	—	V_{CCA}	mV, p-p
$V_{REF-IN-DIFF}$	Input swing, differential clock	200	—	$2*V_{CCA}$	mV, p-p differential
V_{REF-IN}	Input levels	0	—	V_{CCA} + 0.3	V
$V_{REF-CM-AC}$	Input common mode range (AC coupled)[2]	0.125	—	V_{CCA}	V
D_{REF}	Duty cycle[3]	40	—	60	%
T_{REF-R}	Rise time (20% to 80%)	200	500	1000	ps
T_{REF-F}	Fall time (80% to 20%)	200	500	1000	ps
$Z_{REF-IN-TERM-DIFF}$	Differential input termination	-20%	100/2K	+20%	Ohms
$C_{REF-IN-CAP}$	Input capacitance	—	—	7	pF

1. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.
2. When AC coupled, the input common mode range is determined by:
(Min input level) + (Peak-to-peak input swing)/2 ≤ (Input common mode voltage) ≤ (Max input level) - (Peak-to-peak input swing)/2
3. Measured at 50% amplitude.
4. Depending on the application, the PLL_LOL_SET and CDR_LOL_SET control registers may be adjusted for other tolerance values as described in TN1176, LatticeECP3 SERDES/PCS Usage Guide.

Figure 3-13. SERDES External Reference Clock Waveforms



SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-19. Transmit

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
BR_{SDO}	Serial data rate		270	—	2975	Mbps
$T_{JALIGNMENT}$ [2]	Serial output jitter, alignment	270 Mbps	—	—	0.20	UI
$T_{JALIGNMENT}$ [2]	Serial output jitter, alignment	1485 Mbps	—	—	0.20	UI
$T_{JALIGNMENT}$ [1, 2]	Serial output jitter, alignment	2970Mbps	—	—	0.30	UI
$T_{JTIMING}$	Serial output jitter, timing	270 Mbps	—	—	0.20	UI
$T_{JTIMING}$	Serial output jitter, timing	1485 Mbps	—	—	1.0	UI
$T_{JTIMING}$	Serial output jitter, timing	2970 Mbps	—	—	2.0	UI

Notes:
1. Timing jitter is measured in accordance with SMPTE RP 184-1996, SMPTE RP 192-1996 and the applicable serial data transmission standard, SMPTE 259M-1997 or SMPTE 292M (proposed). A color bar test pattern is used.The value of f_{SCLK} is 270 MHz or 360 MHz for SMPTE 259M, 540 MHz for SMPTE 344M or 1485 MHz for SMPTE 292M serial data rates. See the Timing Jitter Bandpass section.
2. Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.
3. All Tx jitter is measured at the output of an industry standard cable driver; connection to the cable driver is via a 50 ohm impedance differential signal from the Lattice SERDES device.
4. The cable driver drives: RL=75 ohm, AC-coupled at 270, 1485, or 2970 Mbps, RREFLVL=RREFPRE=4.75kohm 1%.

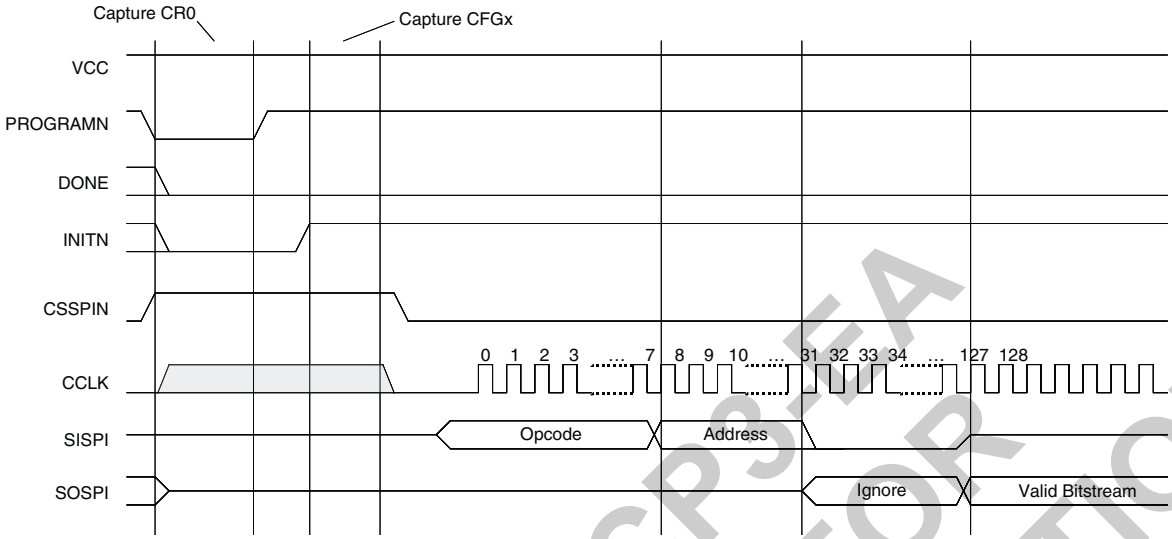
Table 3-20. Receive

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
BR_{SDI}	Serial input data rate		270	—	2970	Mbps
CID	Stream of non-transitions (=Consecutive Identical Digits)		7(3G)/26(SMPTE Triple rates) @ 10-12 BER	—	—	Bits

Table 3-21. Reference Clock

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
F_{VCLK}	Video output clock frequency		27	—	74.25	MHz
DC_V	Duty cycle, video clock		45	50	55	%

Figure 3-24. Master SPI Configuration Waveforms



Industrial

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-17EA-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	17
LFE3-17EA-7FTN256I	1.2V	-7	Lead-Free ftBGA	256	IND	17
LFE3-17EA-8FTN256I	1.2V	-8	Lead-Free ftBGA	256	IND	17
LFE3-17EA-6FN484I	1.2V	-6	Lead-Free fpBGA	484	IND	17
LFE3-17EA-7FN484I	1.2V	-7	Lead-Free fpBGA	484	IND	17
LFE3-17EA-8FN484I	1.2V	-8	Lead-Free fpBGA	484	IND	17

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-35EA-6FTN256I	1.2V	-6	Lead-Free ftBGA	256	IND	33
LFE3-35EA-7FTN256I	1.2V	-7	Lead-Free ftBGA	256	IND	33
LFE3-35EA-8FTN256I	1.2V	-8	Lead-Free ftBGA	256	IND	33
LFE3-35EA-6FN484I	1.2V	-6	Lead-Free fpBGA	484	IND	33
LFE3-35EA-7FN484I	1.2V	-7	Lead-Free fpBGA	484	IND	33
LFE3-35EA-8FN484I	1.2V	-8	Lead-Free fpBGA	484	IND	33
LFE3-35EA-6FN672I	1.2V	-6	Lead-Free fpBGA	672	IND	33
LFE3-35EA-7FN672I	1.2V	-7	Lead-Free fpBGA	672	IND	33
LFE3-35EA-8FN672I	1.2V	-7	Lead-Free fpBGA	672	IND	33

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-70EA-6FN484I	1.2V	-6	Lead-Free fpBGA	484	IND	67
LFE3-70EA-7FN484I	1.2V	-7	Lead-Free fpBGA	484	IND	67
LFE3-70EA-8FN484I	1.2V	-8	Lead-Free fpBGA	484	IND	67
LFE3-70EA-6FN672I	1.2V	-6	Lead-Free fpBGA	672	IND	67
LFE3-70EA-7FN672I	1.2V	-7	Lead-Free fpBGA	672	IND	67
LFE3-70EA-8FN672I	1.2V	-8	Lead-Free fpBGA	672	IND	67
LFE3-70EA-6FN1156I	1.2V	-6	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-7FN1156I	1.2V	-7	Lead-Free fpBGA	1156	IND	67
LFE3-70EA-8FN1156I	1.2V	-8	Lead-Free fpBGA	1156	IND	67

LatticeECP3 Family Data Sheet Revision History

Date	Version	Section	Change Summary
February 2009	01.0	—	Initial release.
May 2009	01.1	All	Removed references to Parallel burst mode Flash.
		Introduction	Features - Changed 250 Mbps to 230 Mbps in Embedded SERDES bulleted section and added a footnote to indicate 230 Mbps applies to 8b10b and 10b12b applications.
			Updated data for ECP3-17 in LatticeECP3 Family Selection Guide table.
			Changed embedded memory from 552 to 700 Kbits in LatticeECP3 Family Selection Guide table.
		Architecture	Updated description for CLKFB in General Purpose PLL Diagram.
			Corrected Primary Clock Sources text section.
			Corrected Secondary Clock/Control Sources text section.
			Corrected Secondary Clock Regions table.
			Corrected note below Detailed sysDSP Slice Diagram.
			Corrected Clock, Clock Enable, and Reset Resources text section.
			Corrected ECP3-17 EBR number in Embedded SRAM in the LatticeECP3 Family table.
			Added On-Chip Termination Options for Input Modes table.
			Updated Available SERDES Quads per LatticeECP3 Devices table.
			Updated Simplified Channel Block Diagram for SERDES/PCS Block diagram.
			Updated Device Configuration text section.
			Corrected software default value of MCLK to be 2.5 MHz.
		DC and Switching Characteristics	Updated VCCOB Min/Max data in Recommended Operating Conditions table.
			Corrected footnote 2 in sysIO Recommended Operating Conditions table.
			Added added footnote 7 for t_{SKEW_PRIB} to External Switching Characteristics table.
			Added 2-to-1 Gearing text section and table.
			Updated External Reference Clock Specification (refclkp/refclkn) table.
			LatticeECP3 sysCONFIG Port Timing Specifications - updated t_{DINIT} information.
			Added sysCONFIG Port Timing waveform.
			Serial Input Data Specifications table, delete Typ data for $V_{RX\text{-}DIFF\text{-}S}$.
			Added footnote 4 to sysCLOCK PLL Timing table for t_{PFD}.
			Added SERDES/PCS Block Latency Breakdown table.
			External Reference Clock Specifications table, added footnote 4, add symbol name vREF-IN-DIFF.
			Added SERDES External Reference Clock Waveforms.
			Updated Serial Output Timing and Levels table.
			Pin-to-pin performance table, changed "typically 3% slower" to "typically slower".

Date	Version	Section	Change Summary
May 2009 (cont.)	01.1 (cont.)	DC and Switching Characteristics (cont.)	Updated timing information
			Updated SERDES minimum frequency.
			Added data to the following tables: External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, Maximum I/O Buffer Speed, DLL Timing, High Speed Data Transmitter, Channel Output Jitter, Typical Building Block Function Performance, Register-to-Register Performance, and Power Supply Requirements.
			Updated Serial Input Data Specifications table.
			Updated Transmit table, Serial Rapid I/O Type 2 Electrical and Timing Characteristics section.
		Pinout Information	Updated Signal Description tables.
			Updated Pin Information Summary tables and added footnote 1.
July 2009	01.2	Multiple	Changed references of “multi-boot” to “dual-boot” throughout the data sheet.
		Architecture	Updated On-Chip Programmable Termination bullets.
			Updated On-Chip Termination Options for Input Modes table.
			Updated On-Chip Termination figure.
		DC and Switching Characterisitcs	Changed min/max data for FREF_PPM and added footnote 4 in SERDES External Reference Clock Specification table.
			Updated SERDES minimum frequency.
		Pinout Information	Corrected MCLK to be I/O and CCLK to be I in Signal Descriptions table
August 2009	01.3	DC and Switching Characterisitcs	Corrected truncated numbers for V_{CCIB} and V_{CCOB} in Recommended Operating Conditions table.
September 2009	01.4	Architecture	Corrected link in sysMEM Memory Block section.
			Updated information for On-Chip Programmable Termination and modified corresponding figure.
			Added footnote 2 to On-Chip Programmable Termination Options for Input Modes table.
			Corrected Per Quadrant Primary Clock Selection figure.
		DC and Switching Characterisitcs	Modified -8 Timing data for 1024x18 True-Dual Port RAM (Read-Before-Write, EBR Output Registers)
			Added ESD Performance table.
			LatticeECP3 External Switching Characteristics table - updated data for $t_{DIBGDDR}$, t_{W_PRI}, t_{W_EDGE} and $t_{SKEW\_EDGE\_DQS}$.
			LatticeECP3 Internal Switching Characteristics table - updated data for t_{COO_PIO} and added footnote #4.
			sysCLOCK PLL Timing table - updated data for f_{OUT}.
			External Reference Clock Specification (refclkp/refclkn) table - updated data for $V_{REF-IN-SE}$ and $V_{REF-IN-DIFF}$.
			LatticeECP3 sysCONFIG Port Timing Specifications table - updated data for t_{MWC}.
			Added TRLVDS DC Specification table and diagram.
			Updated Mini LVDS table.
November 2009	01.5	Introduction	Updated Embedded SERDES features.
			Added SONET/SDH to Embedded SERDES protocols.
		Architecture	Updated Figure 2-4, General Purpose PLL Diagram.
			Updated SONET/SDH to SERDES and PCS protocols.