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Understanding Embedded - FPGAs (Field Programmable Gate Array)

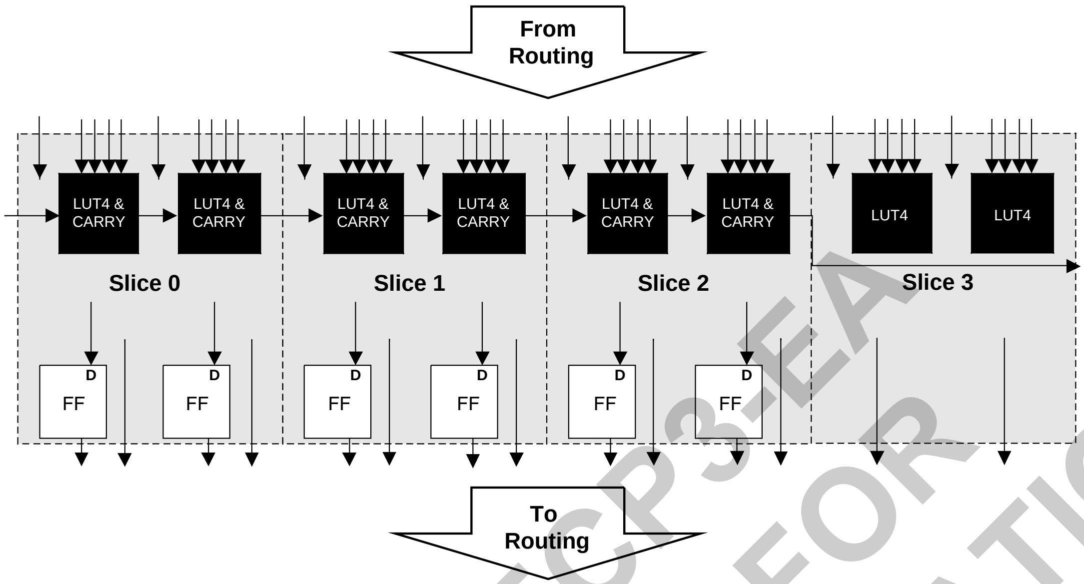
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	11500
Number of Logic Elements/Cells	92000
Total RAM Bits	4526080
Number of I/O	295
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95e-7fn484c

Figure 2-2. PFU Diagram



Slice

Slice 0 through Slice 2 contain two LUT4s feeding two registers, whereas Slice 3 contains two LUT4s only. For PFUs, Slice 0 through Slice 2 can be configured as distributed memory, a capability not available in the PFF. Table 2-1 shows the capability of the slices in both PFF and PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2-1. Resources and Modes Available per Slice

Slice	PFU BLock		PFF Block	
	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s	Logic, ROM	2 LUT4s	Logic, ROM

Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

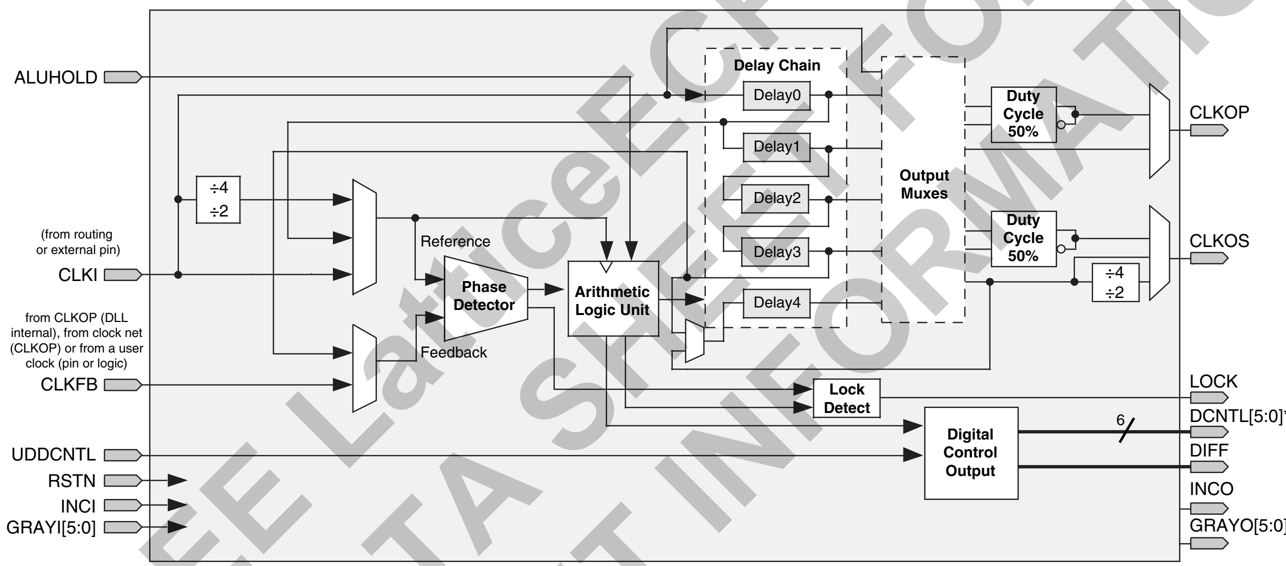
Slices 0, 1 and 2 have 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to the adjacent PFU). Slice 3 has 10 input signals from routing and four signals to routing. Table 2-2 lists the signals associated with Slice 0 to Slice 2.

chain in order to better match the reference and feedback signals. This digital code from the ALU is also transmitted via the Digital Control bus (DCNTL) bus to its associated Slave Delay lines (two per DLL). The ALUHOLD input allows the user to suspend the ALU output at its current value. The UDDCNTL signal allows the user to latch the current value on the DCNTL bus.

The DLL has two clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine delay shift and divider blocks to allow this output to be further modified, if required. The fine delay shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. Both the CLKOS and CLKOP outputs are available with optional duty cycle correction. Divide by two and divide by four frequencies are available at CLKOS. The LOCK output signal is asserted when the DLL is locked. Figure 2-5 shows the DLL block diagram and Table 2-5 provides a description of the DLL inputs and outputs.

The user can configure the DLL for many common functions such as time reference delay mode and clock injection removal mode. Lattice provides primitives in its design tools for these functions.

Figure 2-5. Delay Locked Loop Diagram (DLL)



* This signal is not user accessible. This can only be used to feed the slave delay line.

(referred to as DQS) is not free-running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The delay required for the DQS signal is generated by two dedicated DLLs (DDR DLL) on opposite side of the device. Each DLL creates DQS delays in its half of the device as shown in Figure 2-36. The DDR DLL on the left side will generate delays for all the DQS Strobe pins on Banks 0, 7 and 6 and DDR DLL on the right will generate delays for all the DQS pins on Banks 1, 2 and 3. The DDR DLL loop compensates for temperature, voltage and process variations by using the system clock and DLL feedback loop. DDR DLL communicates the required delay to the DQS delay block using a 7-bit calibration bus (DCNTL[6:0])

The DQS signal (selected PIOs only, as shown in Figure 2-35) feeds from the PAD through a DQS control logic block to a dedicated DQS routing resource. The DQS control logic block consists of DQS Read Control logic block that generates control signals for the read side and DQS Write Control logic that generates the control signals required for the write side. A more detailed DQS control diagram is shown in Figure 2-37, which shows how the DQS control blocks interact with the data paths.

The DQS Read control logic receives the delay generated by the DDR DLL on its side and delays the incoming DQS signal by 90 degrees. This delayed ECLKDQSR is routed to 10 or 11 DQ pads covered by that DQS signal. This block also contains a polarity control logic that generates a DDRCLKPOL signal, which controls the polarity of the clock to the sync registers in the input register blocks. The DQS Read control logic also generates a DDRLAT signal that is in the input register block to transfer data from the first set of DDR register to the second set of DDR registers when using the DDRX2 gearbox mode for DDR3 memory interface.

The DQS Write control logic block generates the DQCLK0 and DQCLK1 clocks used to control the output gearing in the Output register block which generates the DDR data output and the DQS output. They are also used to control the generation of the DQS output through the DQS output register block. In addition to the DCNTL [6:0] input from the DDR DLL, the DQS Write control block also uses a Dynamic Delay DYN DEL [7:0] attribute which is used to further delay the DQS to accomplish the write leveling found in DDR3 memory. Write leveling is controlled by the DDR memory controller implementation. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock. This will generate the DQSW signal used to generate the DQS output in the DQS output register block.

Figure 2-36 and Figure 2-37 show how the DQS transition signals that are routed to the PIOs.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.

Table 2-14. Available SERDES Quads per LatticeECP3 Devices

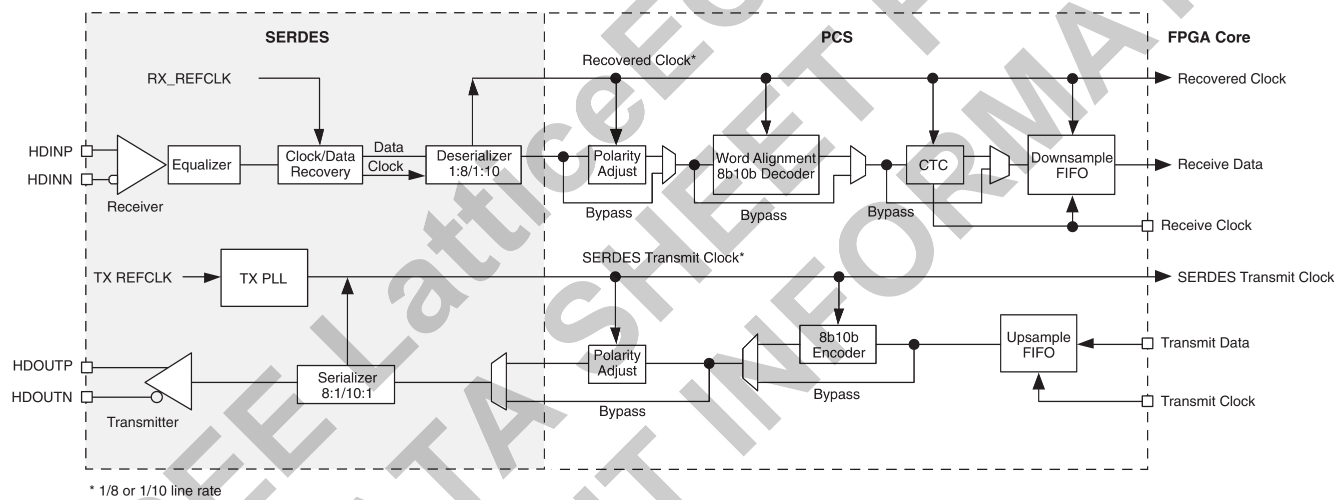
Package	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
256 ftBGA	1	1	—	—	—
484 ftBGA	1	1	1	1	
672 ftBGA	—	1	2	2	2
1156 ftBGA	—	—	3	3	4

SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2-41 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCOB and VCCIB).

Figure 2-41. Simplified Channel Block Diagram for SERDES/PCS Block



PCS

As shown in Figure 2-41, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

SCI (SERDES Client Interface) Bus

The SERDES Client Interface (SCI) is an IP interface that allows the SERDES/PCS Quad block to be controlled by registers rather than the configuration memory cells. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

The ispLEVER design tools from Lattice support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With ispLEVER, the user can define the mode for each quad in a design.

Popular standards such as 10Gb Ethernet, x4 PCI Express and 4x Serial RapidIO can be implemented using IP (available through Lattice), a single quad (Four SERDES channels and PCS) and some additional logic from the core.

The LatticeECP3 family also supports a wide range of primary and secondary protocols. Within the same quad, the LatticeECP3 family can support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. Table 2-15 lists the allowable combination of primary and secondary protocol combinations.

Flexible Quad SERDES Architecture

The LatticeECP3 family SERDES architecture is a quad-based architecture. For most SERDES settings and standards, the whole quad (consisting of four SERDES) is treated as a unit. This helps in silicon area savings, better utilization and overall lower cost.

However, for some specific standards, the LatticeECP3 quad architecture provides flexibility; more than one standard can be supported within the same quad.

Table 2-15 shows the standards can be mixed and matched within the same quad. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same quad. In Table 2-15, the Primary Protocol column refers to the standard that determines the reference clock and PLL settings. The Secondary Protocol column shows the other standard that can be supported within the same quad.

Furthermore, Table 2-15 also implies that more than two standards in the same quad can be supported, as long as they conform to the data rate and reference clock requirements. For example, a quad may contain PCI Express 1.1, SGMII, Serial RapidIO Type I and Serial RapidIO Type II, all in the same quad.

Table 2-15. LatticeECP3 Primary and Secondary Protocol Support

Primary Protocol	Secondary Protocol
PCI Express 1.1	SGMII
PCI Express 1.1	Gigabit Ethernet
PCI Express 1.1	Serial RapidIO Type I
PCI Express 1.1	Serial RapidIO Type II
Serial RapidIO Type I	SGMII
Serial RapidIO Type I	Gigabit Ethernet
Serial RapidIO Type II	SGMII
Serial RapidIO Type II	Gigabit Ethernet
Serial RapidIO Type II	Serial RapidIO Type I
CPRI-3	CPRI-2 and CPRI-1
3G-SDI	HD-SDI and SD-SDI

For further information on SERDES, please see TN1176, LatticeECP3 SERDES/PCS Usage Guide.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeECP3 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test

LatticeECP3 Supply Current (Standby)[1, 2, 3, 4, 5, 6]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical	Units
I_{CC}	Core Power Supply Current	ECP-17EA	89.30	mA
		ECP3-35EA	89.30	mA
		ECP3-70E	226.30	mA
		ECP3-70EA	230.60	mA
		ECP3-95E	226.30	mA
		ECP3-95EA	230.60	mA
		ECP3-150EA	370.80	mA
I_{CCAUX}	Auxiliary Power Supply Current	ECP-17EA	28.20	mA
		ECP3-35EA	28.20	mA
		ECP3-70E	30.60	mA
		ECP3-70EA	30.60	mA
		ECP3-95E	30.60	mA
		ECP3-95EA	30.60	mA
		ECP3-150EA	45.70	mA
I_{CCPLL}	PLL Power Supply Current (Per PLL)	ECP-17EA	0.05	mA
		ECP3-35EA	0.03	mA
		ECP3-70E	0.02	mA
		ECP3-70EA	0.02	mA
		ECP3-95E	0.02	mA
		ECP3-95EA	0.02	mA
		ECP3-150EA	0.02	mA
I_{CCIO}	Bank Power Supply Current (Per Bank)	ECP-17EA	1.38	mA
		ECP3-35EA	1.38	mA
		ECP3-70E	1.43	mA
		ECP3-70EA	1.43	mA
		ECP3-95E	1.43	mA
		ECP3-95EA	1.43	mA
		ECP3-150EA	1.46	mA
I_{CCJ}	JTAG Power Supply Current	All Devices	2.50	mA
I_{CCA}	Transmit, Receive, PLL and Reference Clock Buffer Power Supply	ECP-17EA	5.90	mA
		ECP3-35EA	5.90	mA
		ECP3-70E	17.80	mA
		ECP3-70EA	17.80	mA
		ECP3-95E	17.80	mA
		ECP3-95EA	17.80	mA
		ECP3-150EA	23.80	mA

1. For further information on supply current, please see the list of technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0 MHz.
4. Pattern represents a “blank” configuration data file.
5. T_J = 85°C, power supplies at nominal voltage.
6. To determine the LatticeECP3 peak start-up current data, use the Power Calculator tool in ispLEVER.

LatticeECP3 External Switching Characteristics (Continued)[1, 2]

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Output with Clock and Data (> 10 Bits Wide) Aligned at Pin (GDDRX2_TX.ECLK.Aligned)									
Left and Right Sides									
$t_{DIBGDDR}$	Data Setup Before CLK	ECP3-150EA	—		—		—		ps
$t_{DIAGDDR}$	Data Hold After CLK	ECP3-150EA	—		—		—		ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	—		—		—		MHz
Generic DDRX2 Outputs with Clock and Data Edges Aligned, Without PLL 90-degree shifted clock output[5] (GDDRX2_TX.Aligned)									
$t_{DIBGDDR}$	Data Invalid Before Clock	ECP3-70E/95E	—	200	—	225	—	250	ps
$t_{DIAGDDR}$	Data Invalid After Clock	ECP3-70E/95E	—	200	—	225	—	250	ps
f_{MAX_GDDR}	DDR/DDRX2 Clock Frequency[8]	ECP3-70E/95E	—	500	—	420	—	375	MHz
Generic DDRX2 Output with Clock and Data (> 10 Bits Wide) Centered at Pin Using DQSDLL (GDDRX2_TX.DQS-DLL.Centered)									
Left and Right Sides									
$t_{DVBGDDR}$	Data Valid Before CLK	ECP3-150EA		—		—		—	ns
$t_{DVAGDDR}$	Data Valid After CLK	ECP3-150EA		—		—		—	ns
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	—		—		—		ns
Generic DDRX2 Output with Clock and Data (> 10 Bits Wide) Centered at Pin Using PLL (GDDRX2_TX.PLL.Centered)									
Left and Right Sides									
$t_{DVBGDDR}$	Data Valid Before CLK	ECP3-150EA		—		—		—	ns
$t_{DVAGDDR}$	Data Valid After CLK	ECP3-150EA		—		—		—	ns
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	—		—		—		ns
Generic DDRX2 Outputs with Clock Edge in the Center of Data Window, with PLL 90-degree Shifted Clock Output[6] (GDDRX2_TX.PLL.Centered)									
$t_{DVBGDDR}$	Data Valid Before CLK	ECP3-70E/95E	300	—	370	—	417	—	ps
$t_{DVAGDDR}$	Data Valid After CLK	ECP3-70E/95E	300	—	370	—	417	—	ps
f_{MAX_GDDR}	DDR/DDRX2 Clock Frequency[8]	ECP3-70E/95E	—	500	—	420	—	375	MHz

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Memory Interface									
DDR/DDR2 SDRAM I/O Pin Parameters (Input Data are Strobe Edge Aligned, Output Strobe Edge is Data Centered)[4]									
t_{DVADQ}	Data Valid After DQS (DDR Read)	ECP3-150EA	—	0.225	—	0.225	—	0.225	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	ECP3-150EA	0.64	—	0.64	—	0.64	—	UI
t_{DQVBS}	Data Valid Before DQS	ECP3-150EA	0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Data Valid After DQS	ECP3-150EA	0.25	—	0.25	—	0.25	—	UI
f_{MAX_DDR}	DDR Clock Frequency	ECP3-150EA	95	200	95	200	95	166	MHz
f_{MAX_DDR2}	DDR2 clock frequency	ECP3-150EA	133	266	133	200	133	166	MHz
t_{DVADQ}	Data Valid After DQS (DDR Read)	ECP3-70E/95E	—	0.225	—	0.225	—	0.225	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	ECP3-70E/95E	0.64	—	0.64	—	0.64	—	UI
t_{DQVBS}	Data Valid Before DQS	ECP3-70E/95E	0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Data Valid After DQS	ECP3-70E/95E	0.25	—	0.25	—	0.25	—	UI
f_{MAX_DDR}	DDR Clock Frequency	ECP3-70E/95E	95	200	95	200	95	133	MHz

Figure 3-7. DDR/DDR2/DDR3 SDRAM

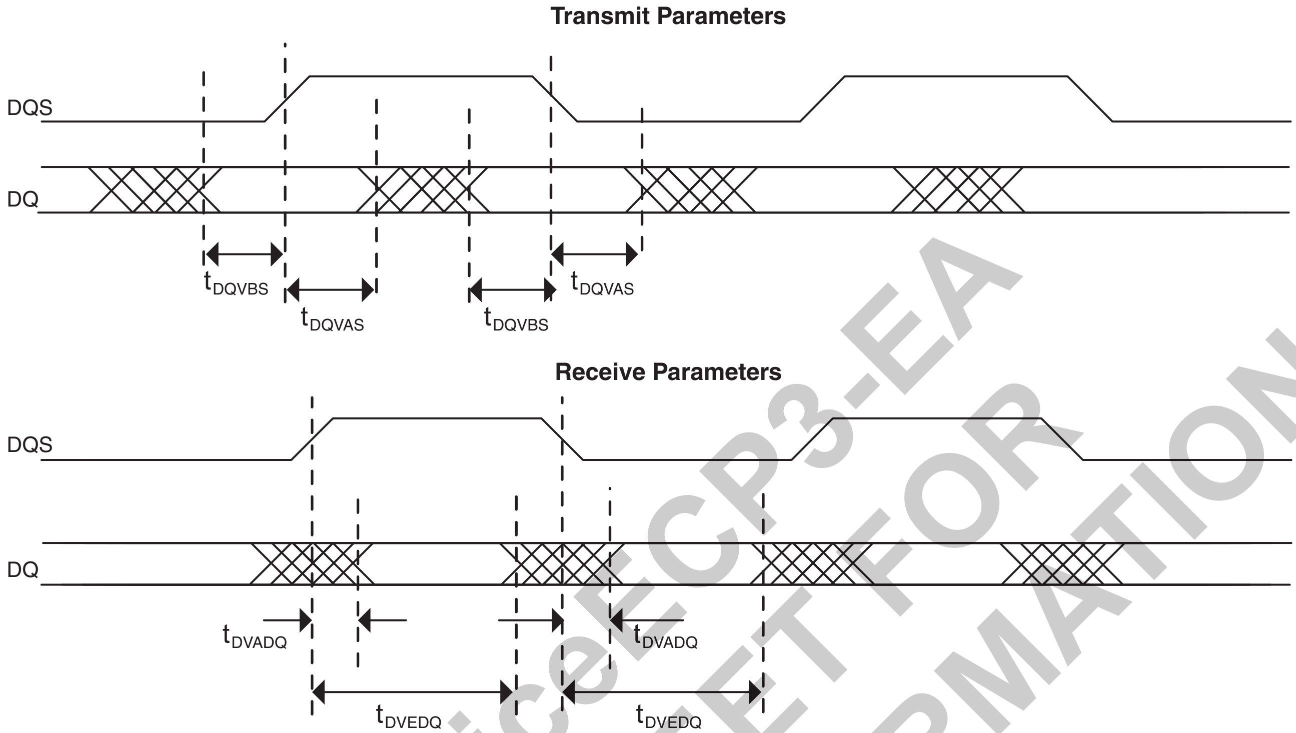


Figure 3-8. Generic DDR/DDR2 Parameters (With Clock Center on Data Window)

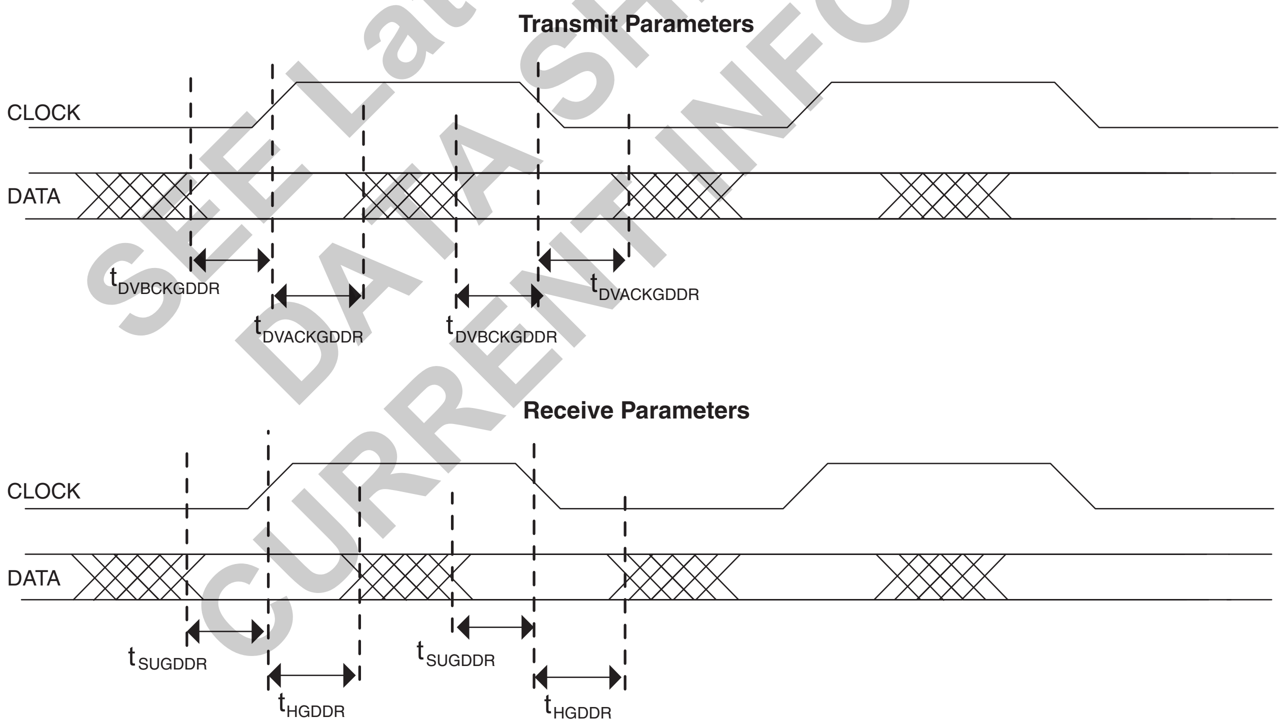
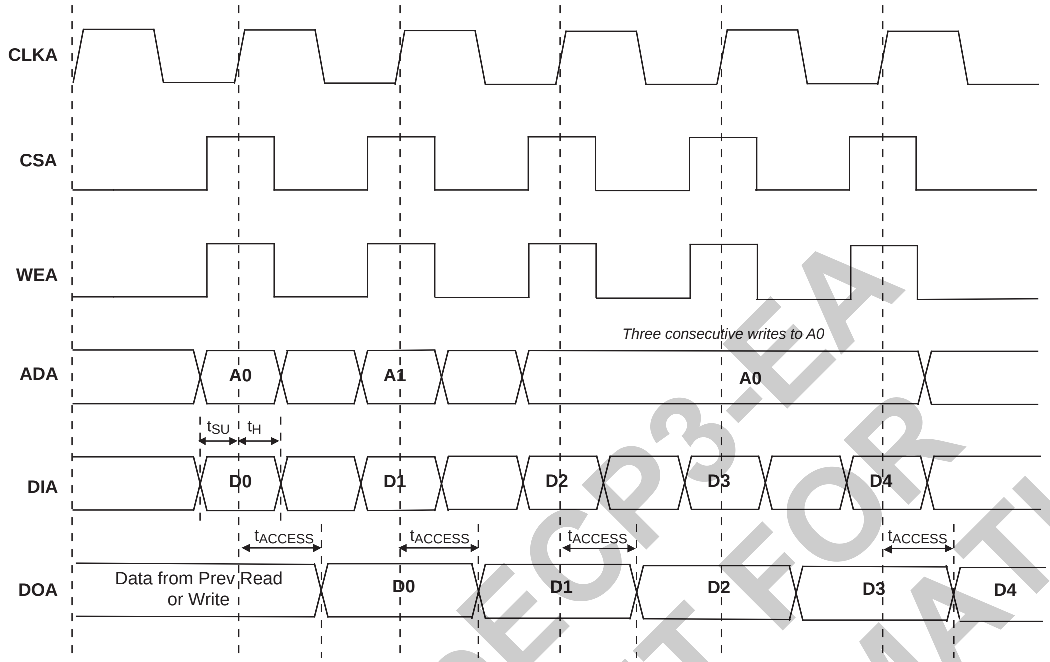


Figure 3-11. Write Through (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

LatticeECP3 Family Timing Adders[1, 2, 3, 4, 5] (Continued)

Over Recommended Commercial Operating Conditions

Buffer Type	Description	-8	-7	-6	Units
RSDS25	RSDS, VCCIO = 2.5V	0.05	0.10	0.16	ns
PPLVDS	Point-to-Point LVDS, Emulated, VCCIO = 2.5V	-0.10	-0.05	0.01	ns
LVPECL33	LVPECL, Emulated, VCCIO = 3.0V	-0.02	-0.04	-0.06	ns
HSTL18_I	HSTL_18 class I 8mA drive, VCCIO = 1.8V	-0.19	-0.16	-0.12	ns
HSTL18_II	HSTL_18 class II, VCCIO = 1.8V	-0.30	-0.28	-0.25	ns
HSTL18D_I	Differential HSTL 18 class I 8mA drive	-0.19	-0.16	-0.12	ns
HSTL18D_II	Differential HSTL 18 class II	-0.30	-0.28	-0.25	ns
HSTL15_I	HSTL_15 class I 4mA drive, VCCIO = 1.5V	-0.22	-0.19	-0.16	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	-0.22	-0.19	-0.16	ns
SSTL33_I	SSTL_3 class I, VCCIO = 3.0V	0.08	0.13	0.19	ns
SSTL33_II	SSTL_3 class II, VCCIO = 3.0V	-0.20	-0.17	-0.14	ns
SSTL33D_I	Differential SSTL_3 class I	0.08	0.13	0.18	ns
SSTL33D_II	Differential SSTL_3 class II	-0.20	-0.17	-0.14	ns
SSTL25_I	SSTL_2 class I 8mA drive, VCCIO = 2.5V	-0.06	-0.02	0.02	ns
SSTL25_II	SSTL_2 class II 16mA drive, VCCIO = 2.5V	-0.19	-0.15	-0.12	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.06	-0.02	0.02	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.19	-0.15	-0.12	ns
SSTL18_I	SSTL_1.8 class I, VCCIO = 1.8V	-0.14	-0.10	-0.07	ns
SSTL18_II	SSTL_1.8 class II 8mA drive, VCCIO = 1.8V	-0.20	-0.17	-0.14	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.14	-0.10	-0.07	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.20	-0.17	-0.14	ns
SSTL15	SSTL_1.5, VCCIO = 1.5V	0.07	0.08	0.08	ns
SSTL15D	Differential SSTL_15	0.07	0.08	0.08	ns
LVTTL33_4mA	LVTTL 4mA drive, VCCIO = 3.0V	0.21	0.23	0.25	ns
LVTTL33_8mA	LVTTL 8mA drive, VCCIO = 3.0V	0.09	0.09	0.10	ns
LVTTL33_12mA	LVTTL 12mA drive, VCCIO = 3.0V	0.02	0.03	0.03	ns
LVTTL33_16mA	LVTTL 16mA drive, VCCIO = 3.0V	0.12	0.13	0.13	ns
LVTTL33_20mA	LVTTL 20mA drive, VCCIO = 3.0V	0.08	0.08	0.09	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, fast slew rate	0.21	0.23	0.25	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, fast slew rate	0.09	0.09	0.10	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, fast slew rate	0.02	0.03	0.03	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, fast slew rate	0.12	0.13	0.13	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, fast slew rate	0.08	0.08	0.09	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, fast slew rate	0.12	0.12	0.12	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, fast slew rate	0.05	0.05	0.05	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, fast slew rate	0.08	0.08	0.08	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, fast slew rate	0.04	0.04	0.04	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, fast slew rate	0.08	0.09	0.09	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, fast slew rate	0.02	0.01	0.01	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, fast slew rate	-0.03	-0.03	-0.03	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, fast slew rate	0.03	0.03	0.03	ns

SERDES High-Speed Data Transmitter[1]

Table 3-6. Serial Output Timing and Levels

Symbol	Description	Frequency	Min.	Typ.	Max.	Units
$V_{TX-DIFF-P-P-1.44}$	Differential swing (1.44V setting)[1, 2]	0.25 to 3.125 Gbps	1150	1440	1730	mV, p-p
$V_{TX-DIFF-P-P-1.35}$	Differential swing (1.35V setting)[1, 2]	0.25 to 3.125 Gbps	1080	1350	1620	mV, p-p
$V_{TX-DIFF-P-P-1.26}$	Differential swing (1.26V setting)[1, 2]	0.25 to 3.125 Gbps	1000	1260	1510	mV, p-p
$V_{TX-DIFF-P-P-1.13}$	Differential swing (1.13V setting)[1, 2]	0.25 to 3.125 Gbps	840	1130	1420	mV, p-p
$V_{TX-DIFF-P-P-1.04}$	Differential swing (1.04V setting)[1, 2]	0.25 to 3.125 Gbps	780	1040	1300	mV, p-p
$V_{TX-DIFF-P-P-0.92}$	Differential swing (0.92V setting)[1, 2]	0.25 to 3.125 Gbps	690	920	1150	mV, p-p
$V_{TX-DIFF-P-P-0.87}$	Differential swing (0.87V setting)[1, 2]	0.25 to 3.125 Gbps	650	870	1090	mV, p-p
$V_{TX-DIFF-P-P-0.78}$	Differential swing (0.78V setting)[1, 2]	0.25 to 3.125 Gbps	585	780	975	mV, p-p
$V_{TX-DIFF-P-P-0.64}$	Differential swing (0.64V setting)[1, 2]	0.25 to 3.125 Gbps	480	640	800	mV, p-p
V_{OCM}	Output common mode voltage	—	V_{CCOB} -0.75	V_{CCOB} -0.60	V_{CCOB} -0.45	V
T_{TX-R}	Rise time (20% to 80%)	—	145	185	265	ps
T_{TX-F}	Fall time (80% to 20%)	—	145	185	265	ps
$Z_{TX-OI-SE}$	Output Impedance 50/75/HiZ Ohms (single ended)	—	-20%	50/75/ Hi Z	+20%	Ohms
R_{LTX-RL}	Return loss (with package)	—	10			dB
$T_{TX-INTRASKEW}$	Lane-to-lane TX skew within a SERDES quad block (intra-quad)	—	—	—	200	ps
$T_{TX-INTERSKEW}$[3]	Lane-to-lane skew between SERDES quad blocks (inter-quad)	—	—	—	1UI +200	ps

1. All measurements are with 50 ohm impedance.
2. See TN1176, LatticeECP3 SERDES/PCS Usage Guide for actual binary settings and the min-max range.
3. Inter-quad skew is between all SERDES channels on the device and requires the use of a low skew internal reference clock.

Table 3-7. Channel Output Jitter

Description	Frequency	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	—	—	0.17	UI, p-p
Random	3.125 Gbps	—	—	0.25	UI, p-p
Total	3.125 Gbps	—	—	0.35	UI, p-p
Deterministic	2.5Gbps	—	—	0.17	UI, p-p
Random	2.5Gbps	—	—	0.20	UI, p-p
Total	2.5Gbps	—	—	0.35	UI, p-p
Deterministic	1.25 Gbps	—	—	0.10	UI, p-p
Random	1.25 Gbps	—	—	0.22	UI, p-p
Total	1.25 Gbps	—	—	0.24	UI, p-p
Deterministic	622 Mbps	—	—	0.10	UI, p-p
Random	622 Mbps	—	—	0.20	UI, p-p
Total	622 Mbps	—	—	0.24	UI, p-p
Deterministic	250 Mbps	—	—	0.10	UI, p-p
Random	250 Mbps	—	—	0.18	UI, p-p
Total	250 Mbps	—	—	0.24	UI, p-p

Note: Values are measured with PRBS 2^7-1, all channels operating, FPGA logic active, I/Os around SERDES pins quiet, reference clock @ 10X mode.

SERDES/PCS Block Latency

Table 3-8 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3-12 shows the location of each block.

Table 3-8. SERDES/PCS Latency Breakdown

Item	Description	Min.	Avg.	Max.	Fixed	Bypass	Units
Transmit Data Latency[1]							
T1	FPGA Bridge - Gearing disabled with different clocks	1	3	5	—	1	word clk
	FPGA Bridge - Gearing disabled with same clocks	—	—	—	3	1	word clk
	FPGA Bridge - Gearing enabled	1	3	5	—	—	word clk
T2	8b10b Encoder	—	—	—	2	1	word clk
T3	SERDES Bridge transmit	—	—	—	2	1	word clk
T4	Serializer: 8-bit mode	—	—	—	15 + Δ1	—	UI + ps
	Serializer: 10-bit mode	—	—	—	18 + Δ1	—	UI + ps
T5	Pre-emphasis ON	—	—	—	1 + Δ2	—	UI + ps
	Pre-emphasis OFF	—	—	—	0 + Δ3	—	UI + ps
Receive Data Latency[2]							
R1	Equalization ON	—	—	—	Δ1	—	UI + ps
	Equalization OFF	—	—	—	Δ2	—	UI + ps
R2	Deserializer: 8-bit mode	—	—	—	10 + Δ3	—	UI + ps
	Deserializer: 10-bit mode	—	—	—	12 + Δ3	—	UI + ps
R3	SERDES Bridge receive	—	—	—	2	—	word clk
R4	Word alignment	3.1	—	4	—	—	word clk
R5	8b10b decoder	—	—	—	1	—	word clk
R6	Clock Tolerance Compensation	7	15	23	1	1	word clk
R7	FPGA Bridge - Gearing disabled with different clocks	1	3	5	—	1	word clk
	FPGA Bridge - Gearing disabled with same clocks	—	—	—	3	1	word clk
	FPGA Bridge - Gearing enabled	1	3	5	—	—	word clk

1. Δ1 = -245ps, Δ2 = +88ps, Δ3 = +112ps.
2. Δ1 = +118ps, Δ2 = +132ps, Δ3 = +700ps.

Figure 3-12. Transmitter and Receiver Latency Block Diagram

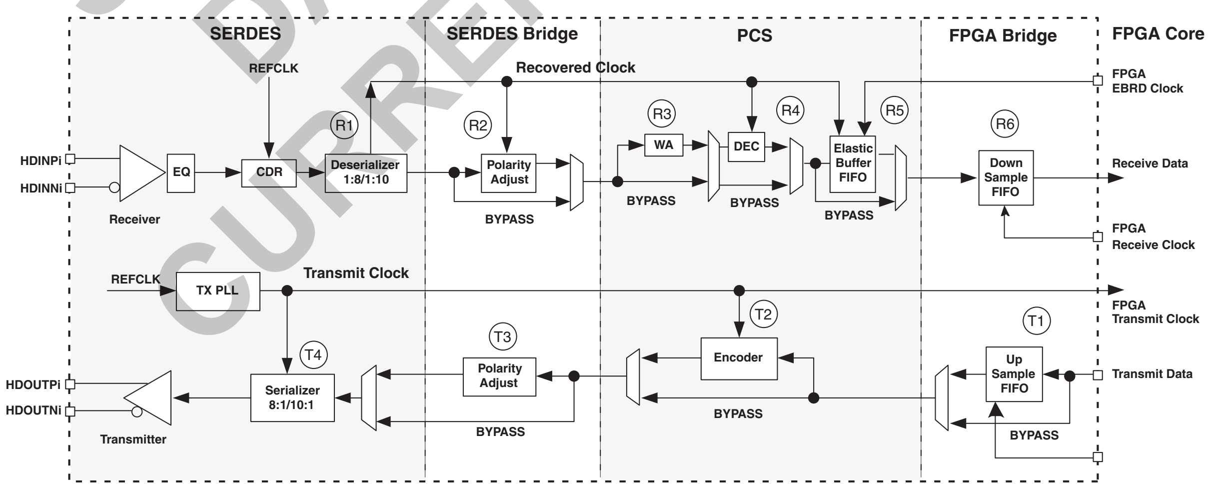


Table 3-11. Periodic Receiver Jitter Tolerance Specification

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Periodic	2.97 Gbps	600 mV differential eye	—	—	0.24	UI, p-p
Periodic	2.5 Gbps	600 mV differential eye	—	—	0.22	UI, p-p
Periodic	1.485 Gbps	600 mV differential eye	—	—	0.24	UI, p-p
Periodic	622 Mbps	600 mV differential eye	—	—	0.15	UI, p-p
Periodic	155 Mbps	600 mV differential eye	—	—	0.5	UI, p-p

Note: Values are measured with PRBS 2^7-1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.

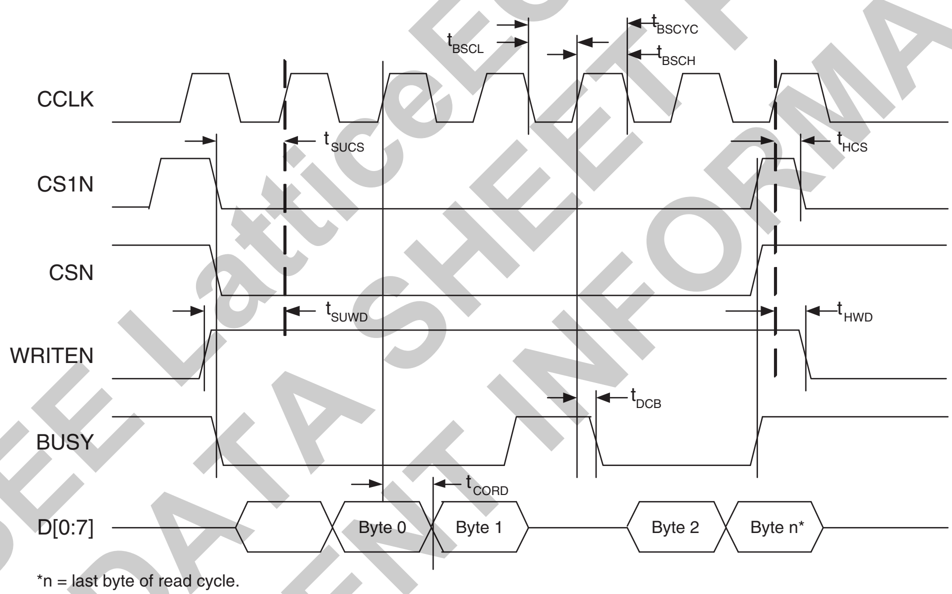
LatticeECP3 sysCONFIG Port Timing Specifications (Continued)

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
t_{CHHH}	HOLDN Low Hold Time (Relative to CCLK)	5	—	ns
Master and Slave SPI (Continued)				
t_{CHHL}	HOLDN High Hold Time (Relative to CCLK)	5	—	ns
t_{HHCH}	HOLDN High Setup Time (Relative to CCLK)	5	—	ns
t_{HLQZ}	HOLDN to Output High-Z	—	9	ns
t_{HHQX}	HOLDN to Output Low-Z	—	9	ns

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value - 15%	Selected value + 15%	MHz
Duty Cycle	40	60	%

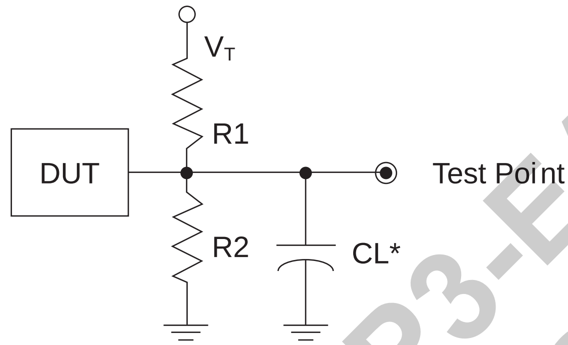
Figure 3-16. sysCONFIG Parallel Port Read Cycle



Switching Test Conditions

Figure 3-26 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-23.

Figure 3-26. Output Test Load, LVTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-23. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	R_2	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L -> H, H -> L)	∞	∞	0pF	LVCMOS 3.3 = 1.5V	—
				LVCMOS 2.5 = $V_{CCIO}/2$	—
				LVCMOS 1.8 = $V_{CCIO}/2$	—
				LVCMOS 1.5 = $V_{CCIO}/2$	—
				LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> H)	∞	1MΩ	0pF	$V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> L)	1MΩ	∞	0pF	$V_{CCIO}/2$	V_{CCIO}
LVCMOS 2.5 I/O (H -> Z)	∞	100	0pF	V_{OH} - 0.10	—
LVCMOS 2.5 I/O (L -> Z)	100	∞	0pF	V_{OL} + 0.10	V_{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

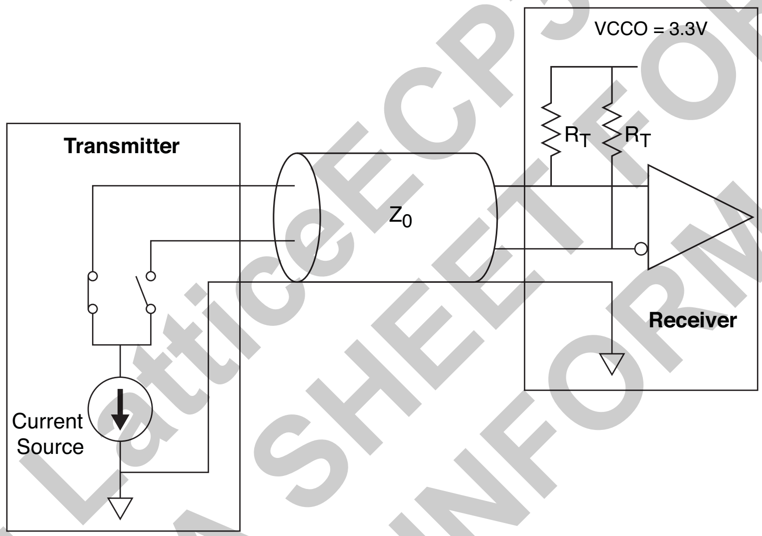
sysI/O Differential Electrical Characteristics

Transition Reduced LVDS (TRLVDS DC Specification)

Over Recommended Operating Conditions

Symbol	Description	Min.	Nom.	Max.	Units
V_{CCO}	Driver supply voltage (+/- 5%)	3.14	3.3	3.47	V
V_{ID}	Input differential voltage	150		1200	mV
V_{ICM}	Input common mode voltage	3		3.265	V
V_{CCO}	Termination supply voltage	3.14	3.3	3.47	V
R_T	Termination resistance (off-chip)	45	50	55	Ohms

Note: LatticeECP3 only supports the TRLVDS receiver.



Mini LVDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Typ.	Max.	Units
Z_O	Single-ended PCB trace impedance	30	50	75	ohms
R_T	Differential termination resistance	50	100	150	ohms
V_{OD}	Output voltage, differential, $\|V_{OP} - V_{OM}\|$	300	—	600	mV
V_{OS}	Output voltage, common mode, $\|V_{OP} + V_{OM}\|/2$	1	1.2	1.4	V
ΔV_{OD}	Change in V_{OD}, between H and L	—	—	50	mV
ΔV_{ID}	Change in V_{OS}, between H and L	—	—	50	mV
V_{THD}	Input voltage, differential, $\|V_{INP} - V_{INM}\|$	200	—	600	mV
V_{CM}	Input voltage, common mode, $\|V_{INP} + V_{INM}\|/2$	$0.3+(V_{THD}/2)$	—	$2.1-(V_{THD}/2)$	
T_R, T_F	Output rise and fall times, 20% to 80%	—	—	550	ps
T_{ODUTY}	Output clock duty cycle	40	—	60	%

Note: Data is for 6mA differential current drive. Other differential driver current options are available.

Pin Information Summary (Cont.)

Pin Information Summary		ECP3-70E			ECP3-70EA		
Pin Type		484 fpBGA	672 fpBGA	1156 fpBGA	484 fpBGA	672 fpBGA	1156 fpBGA
Emulated Differential I/O per Bank	Bank 0	21	30	43	21	30	43
	Bank 1	18	24	39	18	24	39
	Bank 2	10	15	16	8	12	13
	Bank 3	23	27	39	20	23	33
	Bank 6	26	30	39	22	25	33
	Bank 7	14	20	22	11	16	18
	Bank 8	12	12	12	12	12	12
High-Speed Differential I/O per Bank	Bank 0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0
	Bank 2	4	6	6	6	9	9
	Bank 3	6	8	10	9	12	16
	Bank 6	7	9	10	11	14	16
	Bank 7	6	8	9	9	12	13
	Bank 8	0	0	0	0	0	0
Total Single-Ended/ Total Differential I/O per Bank	Bank 0	42/21	60/30	86/43	42/21	60/30	86/43
	Bank 1	36/18	48/24	78/39	36/18	48/24	78/39
	Bank 2	28/14	42/21	44/22	28/14	42/21	44/22
	Bank 3	58/29	71/35	98/49	58/29	71/35	98/49
	Bank 6	67/33	79/38	98/49	67/33	78/39	98/49
	Bank 7	40/20	56/28	62/31	40/20	56/28	62/31
	Bank 8	24/12	24/12	24/12	24/12	24/12	24/12
DDR Groups Bonded per Bank	Bank 0	3	5	7	3	5	7
	Bank 1	3	4	7	3	4	7
	Bank 2	2	3	3	2	3	3
	Bank 3	3	4	5	3	4	5
	Bank 6	4	4	5	4	4	5
	Bank 7	3	4	4	3	4	4
	Configuration Bank 8	0	0	0	0	0	0
SERDES Quads		1	2	3	1	2	3

LatticeECP3 Family Data Sheet
Ordering Information

March 2010 | Preliminary Data Sheet DS1021

LatticeECP3 Part Number Description

LFE3 – XXX XX – X XXXXXX X

Device Family
ECP3 (LatticeECP3 FPGA + SERDES)

Logic Capacity
17 = 17K LUTs
35 = 33K LUTs
70 = 67K LUTs
95 = 92K LUTs
150 = 149K LUTs

Supply Voltage
E or EA = 1.2V

Speed
6 = Slowest
7
8 = Fastest

Grade
C = Commercial
I = Industrial

Package
FTN256 = 256-ball Lead-Free ftBGA
FN484 = 484-ball Lead-Free fpBGA
FN672 = 672-ball Lead-Free fpBGA
FN1156 = 1156-ball Lead-Free fpBGA

Ordering Information

LatticeECP3 devices have top-side markings, for commercial and industrial grades, as shown below:

Commercial	Industrial
Lattice ECP3 LFE3-95E 7FN672C Datecode	Lattice ECP3 LFE3-95E 7FN672I Datecode

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-70E-6FN484C[1]	1.2V	-6	Lead-Free fpBGA	484	COM	67
LFE3-70E-7FN484C[1]	1.2V	-7	Lead-Free fpBGA	484	COM	67
LFE3-70E-8FN484C[1]	1.2V	-8	Lead-Free fpBGA	484	COM	67
LFE3-70E-6FN672C[1]	1.2V	-6	Lead-Free fpBGA	672	COM	67
LFE3-70E-7FN672C[1]	1.2V	-7	Lead-Free fpBGA	672	COM	67
LFE3-70E-8FN672C[1]	1.2V	-8	Lead-Free fpBGA	672	COM	67
LFE3-70E-6FN1156C[1]	1.2V	-6	Lead-Free fpBGA	1156	COM	67
LFE3-70E-7FN1156C[1]	1.2V	-7	Lead-Free fpBGA	1156	COM	67
LFE3-70E-8FN1156C[1]	1.2V	-8	Lead-Free fpBGA	1156	COM	67

1.This device has associated errata. View www.latticesemi.com/documents/ds1021.zip for a description of the errata.

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-95EA-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	92
LFE3-95EA-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	92
LFE3-95EA-8FN484C	1.2V	-8	Lead-Free fpBGA	484	COM	92
LFE3-95EA-6FN672C	1.2V	-6	Lead-Free fpBGA	672	COM	92
LFE3-95EA-7FN672C	1.2V	-7	Lead-Free fpBGA	672	COM	92
LFE3-95EA-8FN672C	1.2V	-8	Lead-Free fpBGA	672	COM	92
LFE3-95EA-6FN1156C	1.2V	-6	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-7FN1156C	1.2V	-7	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-8FN1156C	1.2V	-8	Lead-Free fpBGA	1156	COM	92

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-95E-6FN484C[1]	1.2V	-6	Lead-Free fpBGA	484	COM	92
LFE3-95E-7FN484C[1]	1.2V	-7	Lead-Free fpBGA	484	COM	92
LFE3-95E-8FN484C[1]	1.2V	-8	Lead-Free fpBGA	484	COM	92
LFE3-95E-6FN672C[1]	1.2V	-6	Lead-Free fpBGA	672	COM	92
LFE3-95E-7FN672C[1]	1.2V	-7	Lead-Free fpBGA	672	COM	92
LFE3-95E-8FN672C[1]	1.2V	-8	Lead-Free fpBGA	672	COM	92
LFE3-95E-6FN1156C[1]	1.2V	-6	Lead-Free fpBGA	1156	COM	92
LFE3-95E-7FN1156C[1]	1.2V	-7	Lead-Free fpBGA	1156	COM	92
LFE3-95E-8FN1156C[1]	1.2V	-8	Lead-Free fpBGA	1156	COM	92

1.This device has associated errata. View www.latticesemi.com/documents/ds1021.zip for a description of the errata.

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672C	1.2V	-6	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7FN672C	1.2V	-7	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8FN672C	1.2V	-8	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6FN1156C	1.2V	-6	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7FN1156C	1.2V	-7	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8FN1156C	1.2V	-8	Lead-Free fpBGA	1156	COM	149

LatticeECP3 Family Data Sheet Revision History

March 2010 — Preliminary Data Sheet DS1021

Date	Version	Section	Change Summary
February 2009	01.0	—	Initial release.
May 2009	01.1	All	Removed references to Parallel burst mode Flash.
		Introduction	Features - Changed 250 Mbps to 230 Mbps in Embedded SERDES bulleted section and added a footnote to indicate 230 Mbps applies to 8b10b and 10b12b applications.
			Updated data for ECP3-17 in LatticeECP3 Family Selection Guide table.
			Changed embedded memory from 552 to 700 Kbits in LatticeECP3 Family Selection Guide table.
		Architecture	Updated description for CLKFB in General Purpose PLL Diagram.
			Corrected Primary Clock Sources text section.
			Corrected Secondary Clock/Control Sources text section.
			Corrected Secondary Clock Regions table.
			Corrected note below Detailed sysDSP Slice Diagram.
			Corrected Clock, Clock Enable, and Reset Resources text section.
			Corrected ECP3-17 EBR number in Embedded SRAM in the LatticeECP3 Family table.
			Added On-Chip Termination Options for Input Modes table.
			Updated Available SERDES Quads per LatticeECP3 Devices table.
			Updated Simplified Channel Block Diagram for SERDES/PCS Block diagram.
			Updated Device Configuration text section.
			Corrected software default value of MCLK to be 2.5 MHz.
		DC and Switching Characteristics	Updated VCCOB Min/Max data in Recommended Operating Conditions table.
			Corrected footnote 2 in sysIO Recommended Operating Conditions table.
			Added added footnote 7 for t_{SKEW_PRIB} to External Switching Characteristics table.
			Added 2-to-1 Gearing text section and table.
			Updated External Reference Clock Specification (refclkp/refclkn) table.
			LatticeECP3 sysCONFIG Port Timing Specifications - updated t_{DINIT} information.
			Added sysCONFIG Port Timing waveform.
			Serial Input Data Specifications table, delete Typ data for $V_{RX-DIFF-S}$.
			Added footnote 4 to sysCLOCK PLL Timing table for t_{PFD}.
			Added SERDES/PCS Block Latency Breakdown table.
			External Reference Clock Specifications table, added footnote 4, add symbol name vREF-IN-DIFF.
			Added SERDES External Reference Clock Waveforms.
			Updated Serial Output Timing and Levels table.
			Pin-to-pin performance table, changed "typically 3% slower" to "typically slower".