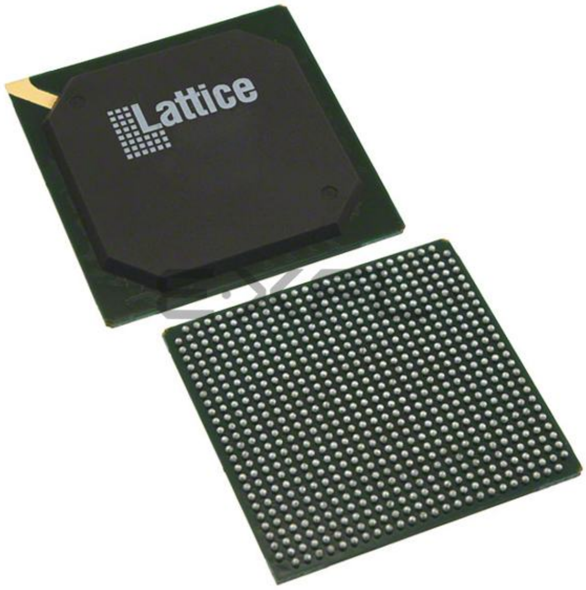

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	11500
Number of Logic Elements/Cells	92000
Total RAM Bits	4526080
Number of I/O	380
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95e-7fn672c

Introduction

The LatticeECP3™ (EConomy Plus Third generation) family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES and high speed source synchronous interfaces in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 65nm technology making the devices suitable for high-volume, high-speed, low-cost applications.

The LatticeECP3 device family expands look-up-table (LUT) capacity to 149K logic elements and supports up to 486 user I/Os. The LatticeECP3 device family also offers up to 320 18x18 multipliers and a wide range of parallel I/O standards.

The LatticeECP3 FPGA fabric is optimized with high performance and low cost in mind. The LatticeECP3 devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the LatticeECP3 device family supports a broad range of interface standards, including DDR3, XGMII and 7:1 LVDS.

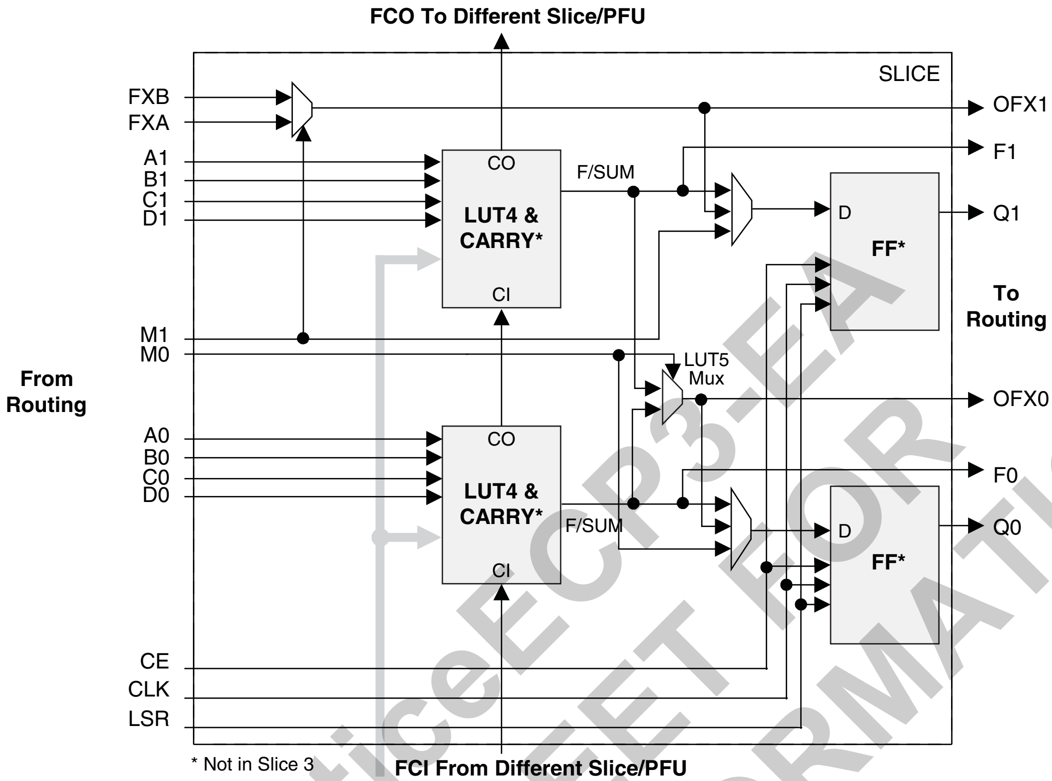
The LatticeECP3 device family also features high speed SERDES with dedicated PCS functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, SMPTE, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit Pre-emphasis and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The LatticeECP3 devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

The ispLEVER® design tool suite from Lattice allows large complex designs to be efficiently implemented using the LatticeECP3 FPGA family. Synthesis library support for LatticeECP3 is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP3 device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) ispLeverCORE™ modules for the LatticeECP3 family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Figure 2-3. Slice Diagram



For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:
- WCK is CLK
- WRE is from LSR
- DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
- WAD [A:D] is a 4-bit address from slice 2 LUT input

Table 2-2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FC	Fast Carry-in[1]
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output[1]

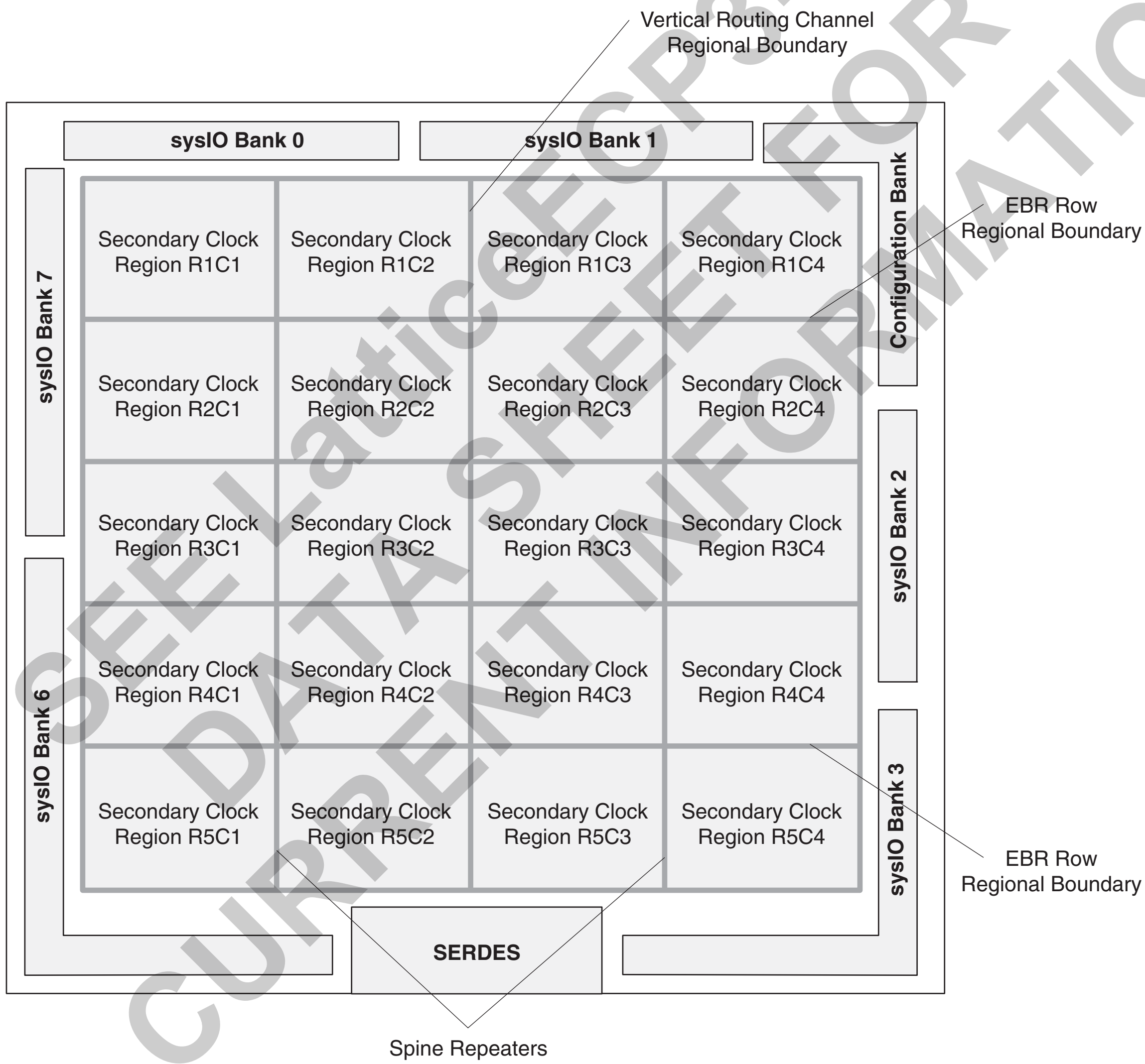
1. See Figure 2-3 for connection details.
2. Requires two PFUs.

secondary clock resources per region (SC0 to SC7). The same secondary clock routing can be used for control signals.

Table 2-6. Secondary Clock Regions

Device	Number of Secondary Clock Regions
ECP3-17	16
ECP3-35	16
ECP3-70	20
ECP3-95	20
ECP3-150	36

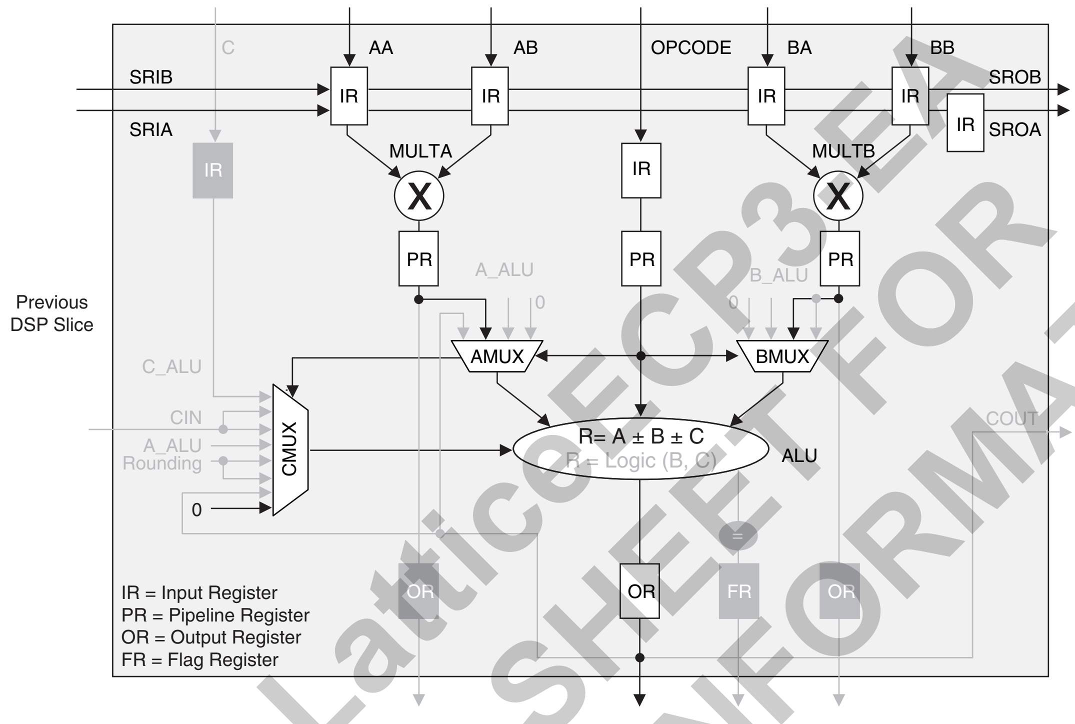
Figure 2-15. LatticeECP3-70 and LatticeECP3-95 Secondary Clock Regions



MULTADDSUB DSP Element

In this case, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB. The user can enable the input, output and pipeline registers. Figure 2-29 shows the MULTADDSUB sysDSP element.

Figure 2-29. MULTADDSUB

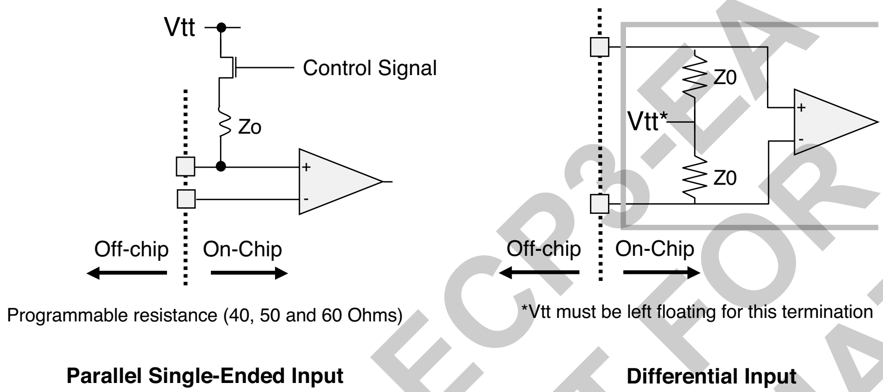


On-Chip Programmable Termination

The LatticeECP3 supports a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single Ended Termination for SSTL15 inputs with programmable resistor values of 40, 50, or 60 ohms. This is particularly useful for low power JEDEC compliant DDR3 memory controller implementations. External termination to Vtt should be used for DDR2 memory controller implementation.
- Common mode termination of 80, 100, 120 ohms for differential inputs

Figure 2-39. On-Chip Termination



See Table 2-12 for termination options for input modes.

Table 2-12. On-Chip Termination Options for Input Modes

IO_TYPE	TERMINATE to VTT[1, 2]	DIFFRENTIAL TERMINATION RESISTOR[1]
LVDS25	þ	80, 100, 120
BLVDS25	þ	80, 100, 120
MLVDS	þ	80, 100, 120
HSTL18_I	40, 50, 60	þ
HSTL18_II	40, 50, 60	þ
HSTL18D_I	40, 50, 60	þ
HSTL18D_II	40, 50, 60	þ
HSTL15_I	40, 50, 60	þ
HSTL15D_I	40, 50, 60	þ
SSTL25_I	40, 50, 60	þ
SSTL25_II	40, 50, 60	þ
SSTL25D_I	40, 50, 60	þ
SSTL25D_II	40, 50, 60	þ
SSTL18_I	40, 50, 60	þ
SSTL18_II	40, 50, 60	þ
SSTL18D_I	40, 50, 60	þ
SSTL18D_II	40, 50, 60	þ
SSTL15	40, 50, 60	þ
SSTL15D	40, 50, 60	þ

1. TERMINATE to VTT and DIFFRENTIAL TERMINATION RESISTOR when turn on can only have one setting per bank. Only left and right banks have this feature.
   Use of TERMINATE to VTT and DIFFRENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank.
   On-chip termination tolerance +/- 20%
2. External termination to VTT should be used when implementing DDR2 memory controller.

access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards.

For more information, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

Device Configuration

All LatticeECP3 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support dual-byte, byte and serial configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. The sysCONFIG port includes seven I/Os used as dedicated pins with the remaining pins used as dual-use pins. See TN1169, LatticeECP3 sysCONFIG Usage Guide for more information about using the dual-use pins as general purpose I/Os.

There are various ways to configure a LatticeECP3 device:

1. JTAG
2. Standard Serial Peripheral Interface (SPI and SPIm modes) - interface to boot PROM memory
3. System microprocessor to drive a x8 CPU port (PCM mode)
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Generic byte wide flash with a MachXO™ device, providing control and addressing

On power-up, the FPGA SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port.

LatticeECP3 devices also support the Slave SPI Interface. In this mode, the FPGA behaves like a SPI Flash device (slave mode) with the SPI port of the FPGA to perform read-write operations.

Enhanced Configuration Options

LatticeECP3 devices have enhanced configuration features such as: decryption support, TransFR™ I/O and dual-boot image support.

1. **TransFR (Transparent Field Reconfiguration)**
   TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. See TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

2. **Dual-Boot Image Support**
   Dual-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LatticeECP3 can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the LatticeECP3 device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

Soft Error Detect (SED) Support

LatticeECP3 devices have dedicated logic to perform Cycle Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, the LatticeECP3 device

Hot Socketing Specifications[1, 3, 4]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDK_HS[2]	Input or I/O Leakage Current	$0 \le V_{IN} \le V_{IH}$ (Max.)	—	—	+/-1	mA
IDK[5]	Input or I/O Leakage Current	$0 \le V_{IN} < V_{CCIO}$	—	—	+/-1	mA
		$V_{CCIO} \le V_{IN} \le V_{CCIO}$ + 0.5V	—	18	—	mA

1. V_{CC}, V_{CCAUX} and V_{CCIO} should rise/fall monotonically.
2. Applicable to general purpose I/O pins in top I/O banks only.
3. I_{DK} is additive to I_{PU}, I_{PW} or I_{BH}.
4. LVCMOS and LVTTL only.
5. Applicable to general purpose I/O pins in left and right I/O banks only.

Hot Socketing Requirements[1, 2]

Description	Min.	Typ.	Max.	Units
Input current per SERDES I/O pin when device is powered down and inputs driven.	—	—	8	mA

1. Assumes the device is powered down, all supplies grounded, both P and N inputs driven by CML driver with maximum allowed VCCOB (1.575V), 8b10b data, internal AC coupling.
2. Each P and N input must have less than the specified maximum input current. For a 16-channel device, the total input current would be 8mA*16 channels *2 input pins per channel = 256mA

ESD Performance

Pin Group	ESD Stress	Min.	Units
All pins	HBM	1000	V
All pins except high-speed serial and XRES[1]	CDM	500	V
High-speed serial inputs	CDM	400	V

1. The XRES pin on the TW device passes CDM testing at 250V.

sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL} Min. (V)	V_{IL} Max. (V)	V_{IH} Min. (V)	V_{IH} Max. (V)	V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
LVCMOS33	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS25	-0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS18	-0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS15	-0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} - 0.4	8, 4	-8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS12	-0.3	0.35 V_{CC}	0.65 V_{CC}	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVTTL33	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
PCI33	-0.3	0.3 V_{CCIO}	0.5 V_{CCIO}	3.6	0.1 V_{CCIO}	0.9 V_{CCIO}	1.5	-0.5
SSTL18_I	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.4	V_{CCIO} - 0.4	6.7	-6.7
SSTL18_II (DDR2 Memory)	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.28	V_{CCIO} - 0.28	8	-8
							11	-11
SSTL2_I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	7.6	-7.6
							12	-12
SSTL2_II (DDR2 Memory)	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCIO} - 0.43	15.2	-15.2
							20	-20
SSTL3_I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCIO} - 1.1	8	-8
SSTL3_II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCIO} - 0.9	16	-16
SSTL15 (DDR3 Memory)	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.3	V_{CCIO} - 0.3	7.5	-7.5
						V_{CCIO} * 0.8	9	-9
HSTL15_I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	4	-4
							8	-8
HSTL18_I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	8	-8
							12	-12
HSTL18_II	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	16	-16

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA, where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

Typical Building Block Function Performance

Pin-to-Pin Performance (LVCMOS25 12mA Drive)[1, 2]

Function	-8 Timing	Units
Basic Functions		
16-bit Decoder	4.7	ns
32-bit Decoder	4.7	ns
64-bit Decoder	5.7	ns
4:1 MUX	4.1	ns
8:1 MUX	4.3	ns
16:1 MUX	4.7	ns
32:1 MUX	4.8	ns

1. These functions were generated using the ispLEVER design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the ispLEVER software.

Register-to-Register Performance[1, 2]

Function	-8 Timing	Units
Basic Functions		
16-bit Decoder	500	MHz
32-bit Decoder	500	MHz
64-bit Decoder	475	MHz
4:1 MUX	500	MHz
8:1 MUX	500	MHz
16:1 MUX	500	MHz
32:1 MUX	445	MHz
8-bit adder	500	MHz
16-bit adder	500	MHz
64-bit adder	305	MHz
16-bit counter	500	MHz
32-bit counter	460	MHz
64-bit counter	320	MHz
64-bit accumulator	315	MHz
Embedded Memory Functions		
512x36 Single Port RAM, EBR Output Registers	340	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	340	MHz
1024x18 True-Dual Port RAM (Read-Before-Write, EBR Output Registers; EA devices only)	130	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	245	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (One PFU)	500	MHz
32x4 Pseudo-Dual Port RAM	500	MHz
64x8 Pseudo-Dual Port RAM	380	MHz
DSP Function		
18x18 Multiplier (All Registers)	400	MHz
9x9 Multiplier (All Registers)	400	MHz
36x36 Multiply (All Registers)	245	MHz

Register-to-Register Performance[1, 2]

Function	-8 Timing	Units
18x18 Multiply/Accumulate (Input & Output Registers)	200	MHz
18x18 Multiply-Add/Sub (All Registers)	400	MHz
DSP IP Functions		
16-Tap Fully-Parallel FIR Filter		MHz
1024-pt, Radix 4, Decimation in Frequency FFT		MHz
8X8 Matrix Multiplication		MHz

1. These timing numbers were generated using ispLEVER tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the ispLEVER software.

Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the ispLEVER design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The ispLEVER design tool can provide logic timing numbers at a particular temperature and voltage.

LatticeECP3 External Switching Characteristics (Continued)[1, 2]

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX_DDR2}	DDR2 Clock Frequency	ECP3-70E/95E	133	266	133	200	133	166	MHz
DDR3 (Using PLL for SCLK) I/O Pin Parameters									
t_{DVADQ}	Data Valid After DQS (DDR Read)	ECP3-150EA	—	0.225	—	0.225	—	0.225	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	ECP3-150EA	0.64	—	0.64	—	0.64	—	UI
t_{DQVBS}	Data Valid Before DQS	ECP3-150EA	0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Data Valid After DQS	ECP3-150EA	0.25	—	0.25	—	0.25	—	UI
f_{MAX_DDR3}	DDR3 clock frequency	ECP3-150EA	266	400	266	333	266	300	MHz

1. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the ispLEVER software.
2. General I/O timing numbers based on LVCMOS 2.5, 12mA, 0pf load.
3. Generic DDR timing numbers based on LVDS I/O.
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18.
5. DDR3 timing numbers based on SSTL15.
6. Uses LVDS I/O standard.
7. The current version of software does not support per bank skew numbers; this will be supported in a future release.
8. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.

Table 3-11. Periodic Receiver Jitter Tolerance Specification

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Periodic	2.97 Gbps	600 mV differential eye	—	—	0.24	UI, p-p
Periodic	2.5 Gbps	600 mV differential eye	—	—	0.22	UI, p-p
Periodic	1.485 Gbps	600 mV differential eye	—	—	0.24	UI, p-p
Periodic	622 Mbps	600 mV differential eye	—	—	0.15	UI, p-p
Periodic	155 Mbps	600 mV differential eye	—	—	0.5	UI, p-p

Note: Values are measured with PRBS 2^7-1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.

XAUI/Serial Rapid I/O Type 3 Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-13. Transmit

Over Recommended Operating Conditions

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
T_{RF}	Differential rise/fall time	20%-80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential impedance		80	100	120	Ohms
J_{TX_DDJ} [2, 3, 4]	Output data deterministic jitter		—	—	0.17	UI
J_{TX_TJ} [1, 2, 3, 4]	Total output data jitter		—	—	0.35	UI

1. Total jitter includes both deterministic jitter and random jitter.
2. Jitter values are measured with each CML output AC coupled into a 50-ohm impedance (100-ohm differential impedance).
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Values are measured at 2.5 Gbps.

Table 3-14. Receive and Jitter Tolerance

Over Recommended Operating Conditions

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
RL_{RX_DIFF}	Differential return loss	From 100 MHz to 3.125 GHz	10	—	—	dB
RL_{RX_CM}	Common mode return loss	From 100 MHz to 3.125 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential termination resistance		80	100	120	Ohms
J_{RX_DJ} [1, 2, 3]	Deterministic jitter tolerance (peak-to-peak)		—	—	0.37	UI
J_{RX_RJ} [1, 2, 3]	Random jitter tolerance (peak-to-peak)		—	—	0.18	UI
J_{RX_SJ} [1, 2, 3]	Sinusoidal jitter tolerance (peak-to-peak)		—	—	0.10	UI
J_{RX_TJ} [1, 2, 3]	Total jitter tolerance (peak-to-peak)		—	—	0.65	UI
T_{RX_EYE}	Receiver eye opening		0.35	—	—	UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-14.
2. Jitter values are measured with each high-speed input AC coupled into a 50-ohm impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance parameters are characterized when Full Rx Equalization is enabled.
5. Values are measured at 2.5 Gbps.

Serial Rapid I/O Type 2 Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-15. Transmit

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
T_{RF}[1]	Differential rise/fall time	20%-80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential impedance		80	100	120	Ohms
J_{TX_DDJ}[3, 4, 5]	Output data deterministic jitter		—	—	0.17	UI
J_{TX_TJ}[2, 3, 4, 5]	Total output data jitter		—	—	0.35	UI

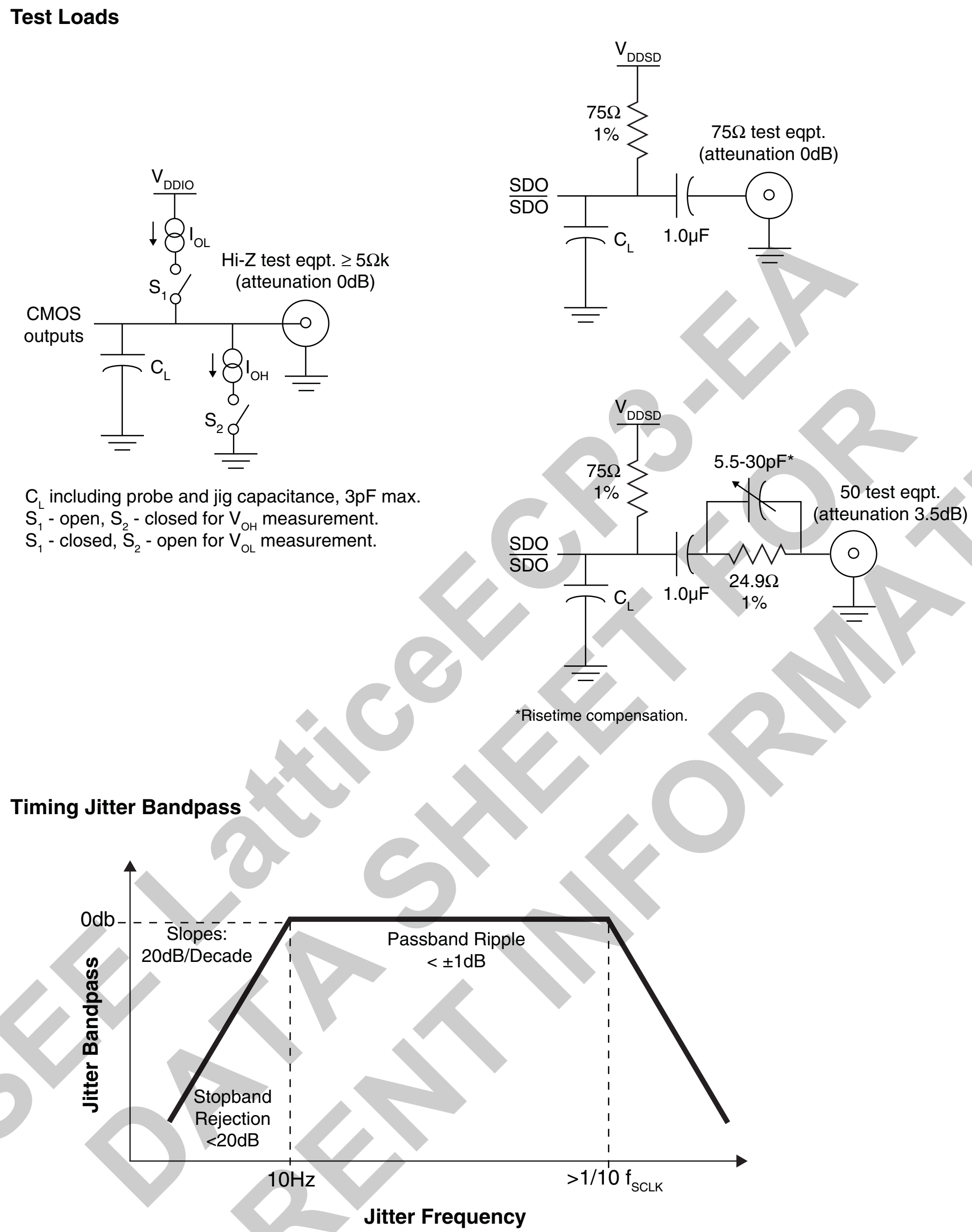
1. Rise and Fall times measured with board trace, connector and approximately 2.5pf load.
2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
3. Jitter values are measured with each CML output AC coupled into a 50-ohm impedance (100-ohm differential impedance).
4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
5. Values are measured at 2.5 Gbps.

Table 3-16. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
RL_{RX_DIFF}	Differential return loss	From 100 MHz to 2.5 GHz	10	—	—	dB
RL_{RX_CM}	Common mode return loss	From 100 MHz to 2.5 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential termination resistance		80	100	120	Ohms
J_{RX_DJ}[2, 3, 4, 5]	Deterministic jitter tolerance (peak-to-peak)		—	—	0.37	UI
J_{RX_RJ}[2, 3, 4, 5]	Random jitter tolerance (peak-to-peak)		—	—	0.18	UI
J_{RX_SJ}[2, 3, 4, 5]	Sinusoidal jitter tolerance (peak-to-peak)		—	—	0.10	UI
J_{RX_TJ}[1, 2, 3, 4, 5]	Total jitter tolerance (peak-to-peak)		—	—	0.65	UI
T_{RX_EYE}	Receiver eye opening		0.35	—	—	UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-14.
2. Jitter values are measured with each high-speed input AC coupled into a 50-ohm impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.
5. Values are measured at 2.5 Gbps.

Figure 3-15. Test Loads



LatticeECP3 sysCONFIG Port Timing Specifications (Continued)

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
t_{CHHH}	HOLDN Low Hold Time (Relative to CCLK)	5	—	ns
Master and Slave SPI (Continued)				
t_{CHHL}	HOLDN High Hold Time (Relative to CCLK)	5	—	ns
t_{HHCH}	HOLDN High Setup Time (Relative to CCLK)	5	—	ns
t_{HLQZ}	HOLDN to Output High-Z	—	9	ns
t_{HHQX}	HOLDN to Output Low-Z	—	9	ns

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value - 15%	Selected value + 15%	MHz
Duty Cycle	40	60	%

Figure 3-16. sysCONFIG Parallel Port Read Cycle

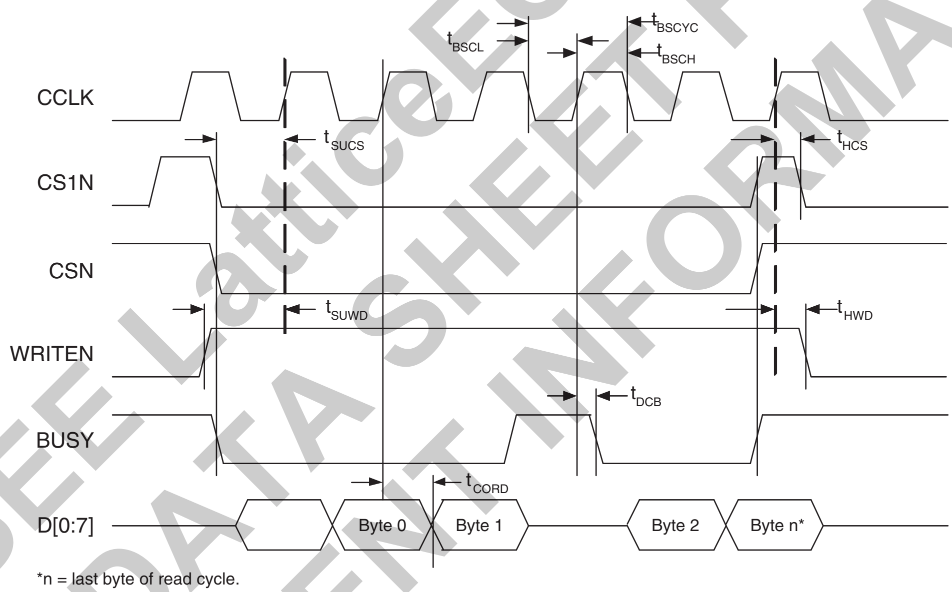
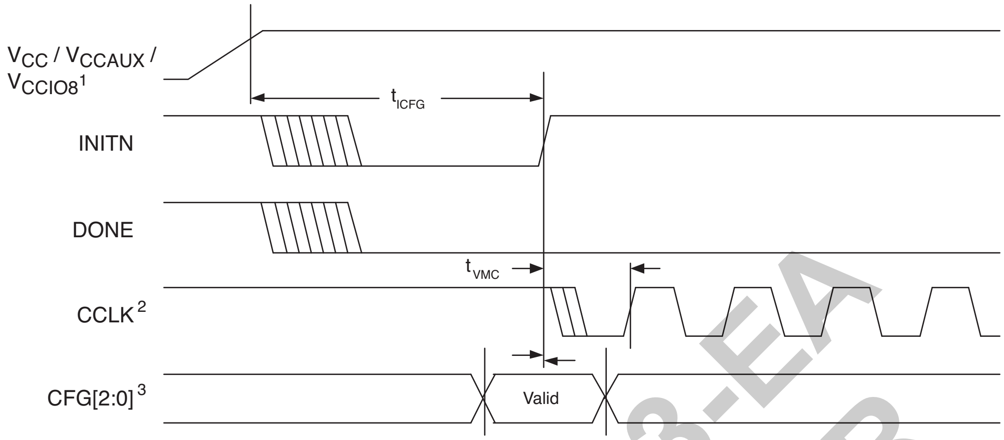
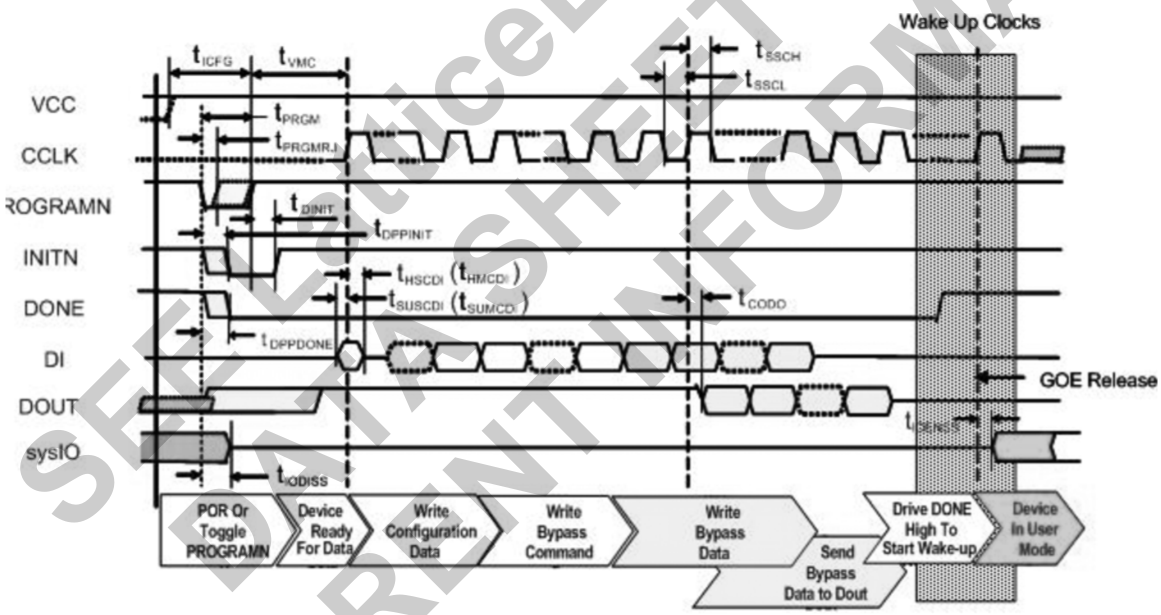


Figure 3-20. Power-On-Reset (POR) Timing



1. Time taken from V_{CC}, V_{CCAUX} or V_{CCIO8}, whichever is the last to cross the POR trip point.
2. Device is in a Master Mode (SPI, SPIm).
3. The CFG pins are normally static (hard wired).

Figure 3-21. sysCONFIG Port Timing



Pin Information Summary

Pin Information Summary		ECP3-17EA		ECP3-35EA			ECP3-70E/EA		
Pin Type		256 ftBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA	1156 fpBGA
General Purpose Inputs/Outputs per Bank	Bank 0	26	36	26	42	48	42	60	86
	Bank 1	14	24	14	36	36	36	48	78
	Bank 2	6	12	6	24	24	24	34	36
	Bank 3	18	44	16	54	59	54	59	86
	Bank 6	20	44	18	63	61	63	67	86
	Bank 7	19	32	19	36	42	36	48	54
	Bank 8	24	24	24	24	24	24	24	24
General Purpose Inputs per Bank	Bank 0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0
	Bank 2	2	2	2	4	4	4	8	8
	Bank 3	0	0	2	4	4	4	12	12
	Bank 6	0	0	2	4	4	4	12	12
	Bank 7	4	4	4	4	4	4	8	8
	Bank 8	0	0	0	0	0	0	0	0
General Purpose Outputs per Bank	Bank 0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0
	Bank 2	0	0	0	0	0	0	0	0
	Bank 3	0	0	0	0	0	0	0	0
	Bank 6	0	0	0	0	0	0	0	0
	Bank 7	0	0	0	0	0	0	0	0
	Bank 8	0	0	0	0	0	0	0	0
Total Single-Ended User I/O		133	222	133	295	310	295	380	490
VCC		6	16	6	16	32	16	32	32
VCCAUX		4	8	4	8	12	8	12	16
VTT		4	4	4	4	4	4	4	8
VCCA		4	4	4	4	8	4	8	16
VCCPLL		2	4	2	4	4	4	4	4
VCCIO	Bank 0	2	2	2	2	4	2	4	4
	Bank 1	2	2	2	2	4	2	4	4
	Bank 2	2	2	2	2	4	2	4	4
	Bank 3	2	2	2	2	4	2	4	4
	Bank 6	2	2	2	2	4	2	4	4
	Bank 7	2	2	2	2	4	2	4	4
	Bank 8	2	2	2	2	2	2	2	2
VCCJ		1	1	1	1	1	1	1	1
TAP		4	4	4	4	4	4	4	4
GND, GNDIO		50	98	50	98	139	98	139	233
NC		0	73	0	0	96	0	0	238
Reserved[1]		0	2	0	2	2	2	2	2
SERDES		26	26	26	26	26	26	52	78
Miscellaneous Pins		8	8	8	8	8	8	8	8
Total Bonded Pins		256	484	256	484	672	484	672	1156

Pin Information Summary (Cont.)

Pin Information Summary		ECP3-95E			ECP3-95EA			ECP3-150EA	
Pin Type		484 fpBGA	672 fpBGA	1156 fpBGA	484 fpBGA	672 fpBGA	1156 fpBGA	672 fpBGA	1156 fpBGA
Emulated Differential I/O per Bank	Bank 0	21	30	43	21	30	43	30	47
	Bank 1	18	24	39	18	24	39	24	43
	Bank 2	10	15	16	8	12	13	12	18
	Bank 3	23	27	39	20	23	33	23	37
	Bank 6	26	30	39	22	25	33	25	37
	Bank 7	14	20	22	11	16	18	16	24
	Bank 8	12	12	12	12	12	12	12	12
Highspeed Differential I/O per Bank	Bank 0	0	0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0	0	0
	Bank 2	4	6	6	6	9	9	9	15
	Bank 3	6	8	10	9	12	16	12	21
	Bank 6	7	9	10	11	14	16	14	21
	Bank 7	6	8	9	9	12	13	12	18
	Bank 8	0	0	0	0	0	0	0	0
Total Single Ended/ Total Differential I/O per Bank	Bank 0	42/21	60/30	86/43	42/21	60/30	86/43	60/30	94/47
	Bank 1	36/18	48/24	78/39	36/18	48/24	78/39	48/24	86/43
	Bank 2	28/14	42/21	44/22	28/14	42/21	44/22	42/21	66/33
	Bank 3	58/29	71/35	98/49	58/29	71/35	98/49	71/35	116/58
	Bank 6	67/33	78/39	98/49	67/33	78/39	98/49	78/39	116/58
	Bank 7	40/20	56/28	62/31	40/20	56/28	62/31	56/28	84/42
	Bank 8	24/12	24/12	24/12	24/12	24/12	24/12	24/12	24/12
DDR Groups Bonded per Bank	Bank 0	3	5	7	3	5	7	5	7
	Bank 1	3	4	7	3	4	7	4	7
	Bank 2	2	3	3	2	3	3	3	4
	Bank 3	3	4	5	3	4	5	4	7
	Bank 6	4	4	5	4	4	5	4	7
	Bank 7	3	4	4	3	4	4	4	6
	Configuration Bank8	0	0	0	0	0	0	0	0
SERDES Quads		1	2	3	1	2	3	2	4

1.These pins must remain floating on the board.

Lattice Semiconductor Corporation

LatticeECP3 Family Data Sheet Supplemental Information

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For Further Information

A variety of technical notes for the LatticeECP3 family are available on the Lattice website at www.latticesemi.com.

- TN1169, LatticeECP3 sysCONFIG Usage Guide
- TN1176, LatticeECP3 SERDES/PCS Usage Guide
- TN1177, LatticeECP3 sysIO Usage Guide
- TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide
- TN1179, LatticeECP3 Memory Usage Guide
- TN1180, LatticeECP3 High-Speed I/O Interface
- TN1181, Power Consumption and Management for LatticeECP3 Devices
- TN1182, LatticeECP3 sysDSP Usage Guide
- TN1184, LatticeECP3 Soft Error Detection (SED) Usage Guide
- TN1189, LatticeECP3 Hardware Checklist

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com