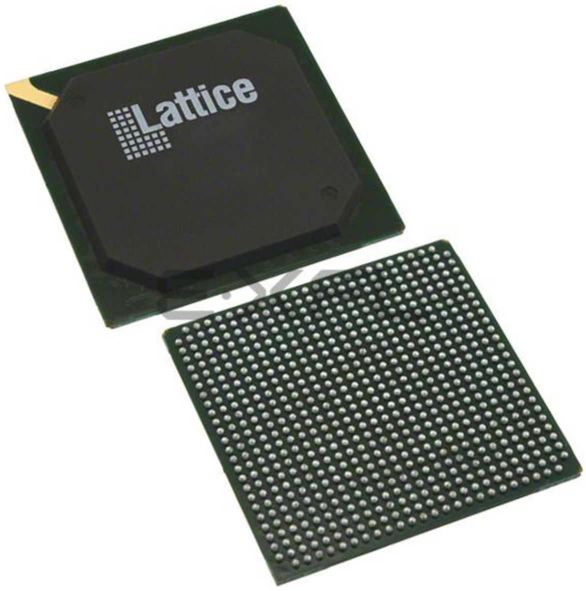

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

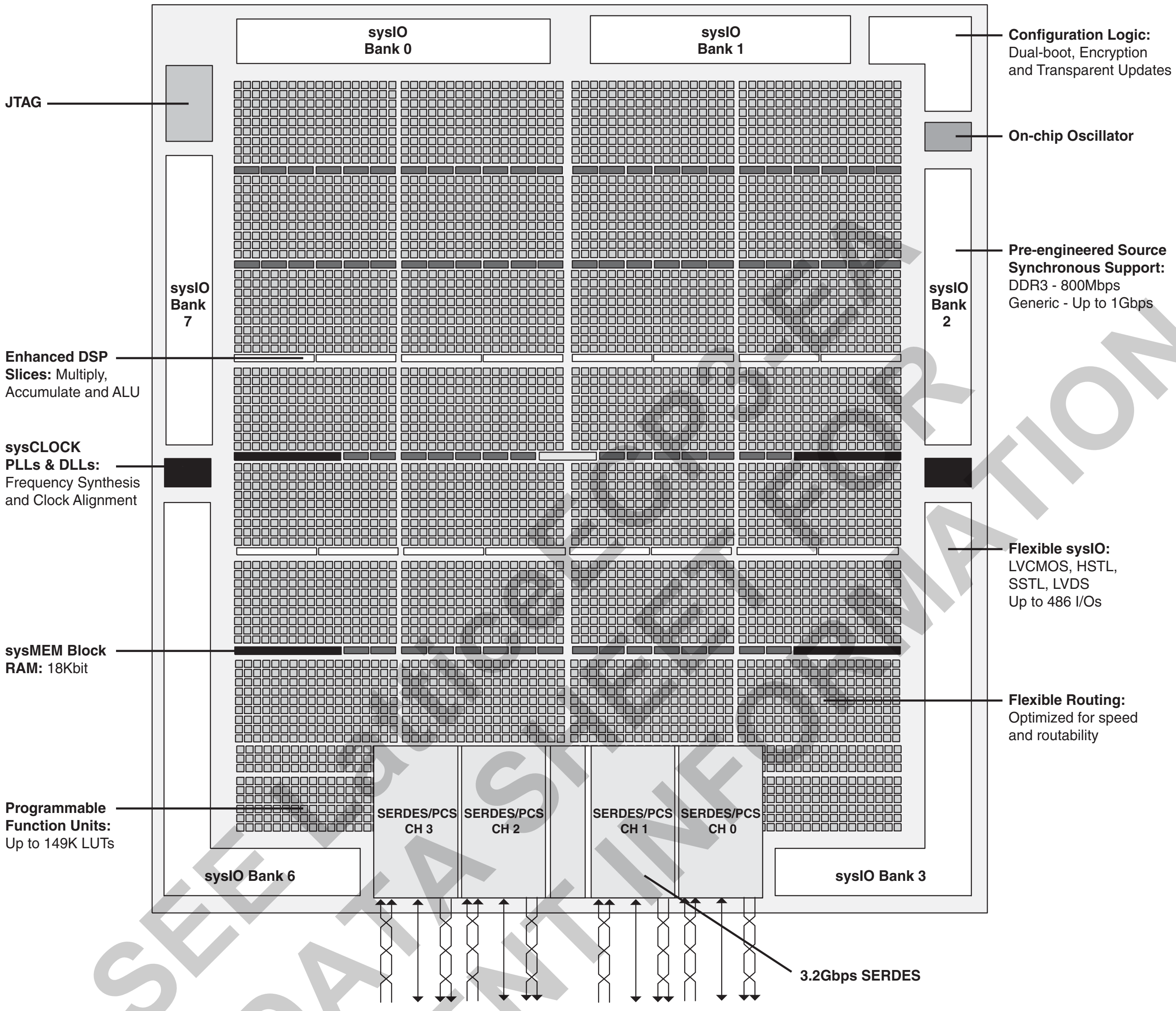
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	11500
Number of Logic Elements/Cells	92000
Total RAM Bits	4526080
Number of I/O	380
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95e-7fn672i

Figure 2-1. Simplified Block Diagram, LatticeECP3-35 Device (Top Level)

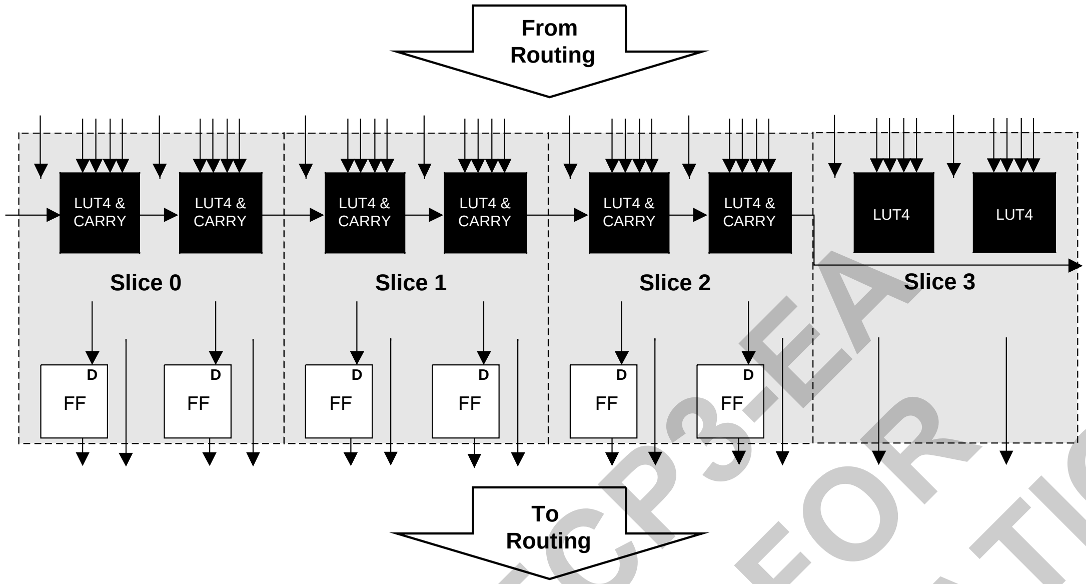


PFU Blocks

The core of the LatticeECP3 device consists of PFU blocks, which are provided in two forms, the PFU and PFF. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices numbered 0-3 as shown in Figure 2-2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

Figure 2-2. PFU Diagram



Slice

Slice 0 through Slice 2 contain two LUT4s feeding two registers, whereas Slice 3 contains two LUT4s only. For PFUs, Slice 0 through Slice 2 can be configured as distributed memory, a capability not available in the PFF. Table 2-1 shows the capability of the slices in both PFF and PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2-1. Resources and Modes Available per Slice

Slice	PFU BLock		PFF Block	
	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s	Logic, ROM	2 LUT4s	Logic, ROM

Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

Slices 0, 1 and 2 have 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to the adjacent PFU). Slice 3 has 10 input signals from routing and four signals to routing. Table 2-2 lists the signals associated with Slice 0 to Slice 2.

Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

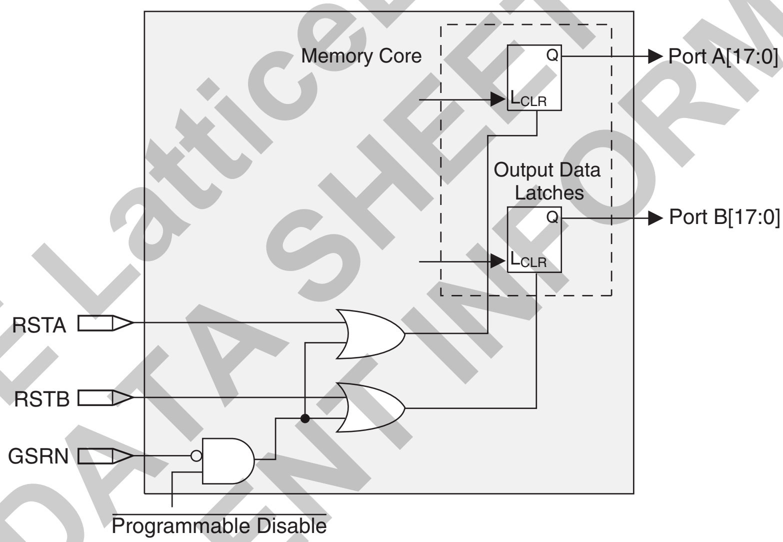
EBR memory supports the following forms of write behavior for single port or dual port operation:

1. **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write (EA devices only)** – When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2-22.

Figure 2-22. Memory Core Reset



For further information on the sysMEM EBR block, please see the list of technical documentation at the end of this data sheet.

sysDSP™ Slice

The LatticeECP3 family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

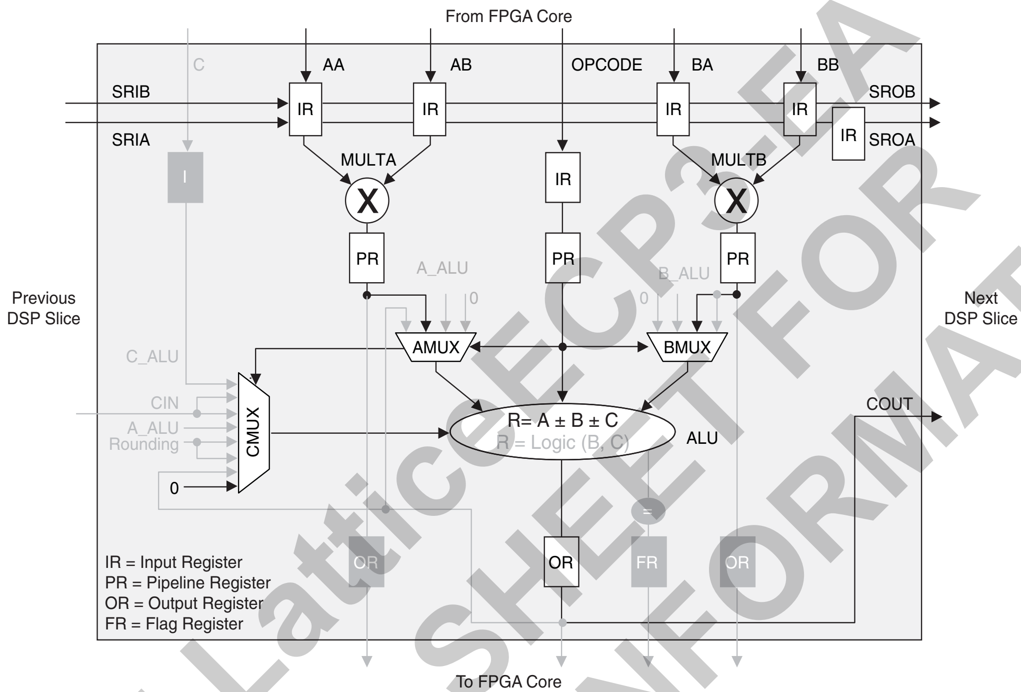
sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP3, on the other hand, has many DSP slices that support different data widths.

MULTADDSUBSUM DSP Element

In this case, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB of Slice 0. Additionally, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB of Slice 1. The results of both addition/subtractions are added by the second ALU following the slice cascade path. The user can enable the input, output and pipeline registers. Figure 2-30 and Figure 2-31 show the MULTADDSUBSUM sysDSP element.

Figure 2-30. MULTADDSUBSUM Slice 0

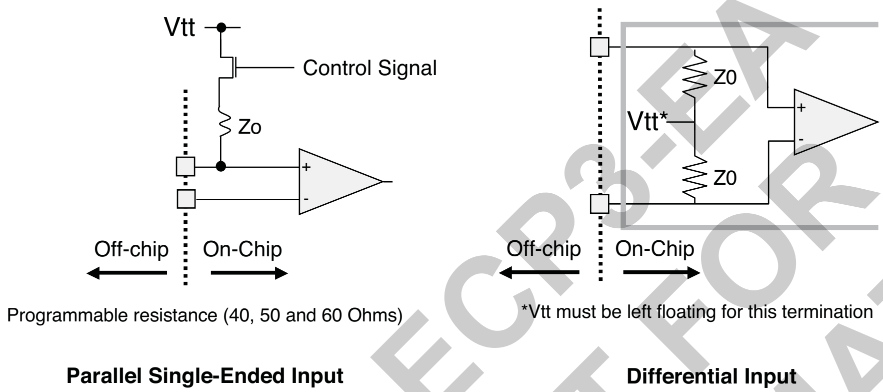


On-Chip Programmable Termination

The LatticeECP3 supports a variety of programmable on-chip terminations options, including:

- Dynamically switchable Single Ended Termination for SSTL15 inputs with programmable resistor values of 40, 50, or 60 ohms. This is particularly useful for low power JEDEC compliant DDR3 memory controller implementations. External termination to Vtt should be used for DDR2 memory controller implementation.
- Common mode termination of 80, 100, 120 ohms for differential inputs

Figure 2-39. On-Chip Termination



See Table 2-12 for termination options for input modes.

Table 2-12. On-Chip Termination Options for Input Modes

IO_TYPE	TERMINATE to VTT[1, 2]	DIFFRENTIAL TERMINATION RESISTOR[1]
LVDS25	þ	80, 100, 120
BLVDS25	þ	80, 100, 120
MLVDS	þ	80, 100, 120
HSTL18_I	40, 50, 60	þ
HSTL18_II	40, 50, 60	þ
HSTL18D_I	40, 50, 60	þ
HSTL18D_II	40, 50, 60	þ
HSTL15_I	40, 50, 60	þ
HSTL15D_I	40, 50, 60	þ
SSTL25_I	40, 50, 60	þ
SSTL25_II	40, 50, 60	þ
SSTL25D_I	40, 50, 60	þ
SSTL25D_II	40, 50, 60	þ
SSTL18_I	40, 50, 60	þ
SSTL18_II	40, 50, 60	þ
SSTL18D_I	40, 50, 60	þ
SSTL18D_II	40, 50, 60	þ
SSTL15	40, 50, 60	þ
SSTL15D	40, 50, 60	þ

1. TERMINATE to VTT and DIFFRENTIAL TERMINATION RESISTOR when turn on can only have one setting per bank. Only left and right banks have this feature.
   Use of TERMINATE to VTT and DIFFRENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank.
   On-chip termination tolerance +/- 20%
2. External termination to VTT should be used when implementing DDR2 memory controller.

can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode (normal operation) the device can be programmed to generate an error signal.

For further information on SED support, please see TN1184, LatticeECP3 Soft Error Detection (SED) Usage Guide.

External Resistor

LatticeECP3 devices require a single external, 10K ohm ±1% value between the XRES pin and ground. Device configuration will not be completed if this resistor is missing. There is no boundary scan register on the external resistor pad.

On-Chip Oscillator

Every LatticeECP3 device has an internal CMOS oscillator which is used to derive a Master Clock (MCLK) for configuration. The oscillator and the MCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCLK is nominally 2.5MHz. Table 2-16 lists all the available MCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 3.1MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.5MHz.

This internal CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

Table 2-16. Selectable Master Clock (MCLK) Frequencies During Configuration (Nominal)

MCLK (MHz)	MCLK (MHz)	MCLK (MHz)
2.5[1]	10	41
3.1	13	45
4.3	15	51
5.4	20	55
6.9	26	60
8.1	30	130
9.2	34	—

1. Software default MCLK frequency. Hardware default is 3.1MHz.

Density Shifting

The LatticeECP3 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. An example is that some user I/Os may become No Connects in smaller devices in the same packge.

Hot Socketing Specifications[1, 3, 4]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDK_HS[2]	Input or I/O Leakage Current	$0 \leq V_{IN} \leq V_{IH}$ (Max.)	—	—	+/-1	mA
IDK[5]	Input or I/O Leakage Current	$0 \leq V_{IN} < V_{CCIO}$	—	—	+/-1	mA
		$V_{CCIO} \leq V_{IN} \leq V_{CCIO} + 0.5V$	—	18	—	mA

1. V_{CC}, V_{CCAUX} and V_{CCIO} should rise/fall monotonically.
2. Applicable to general purpose I/O pins in top I/O banks only.
3. I_{DK} is additive to I_{PU}, I_{PW} or I_{BH}.
4. LVCMOS and LVTTL only.
5. Applicable to general purpose I/O pins in left and right I/O banks only.

Hot Socketing Requirements[1, 2]

Description	Min.	Typ.	Max.	Units
Input current per SERDES I/O pin when device is powered down and inputs driven.	—	—	8	mA

1. Assumes the device is powered down, all supplies grounded, both P and N inputs driven by CML driver with maximum allowed VCCOB (1.575V), 8b10b data, internal AC coupling.
2. Each P and N input must have less than the specified maximum input current. For a 16-channel device, the total input current would be 8mA*16 channels *2 input pins per channel = 256mA

ESD Performance

Pin Group	ESD Stress	Min.	Units
All pins	HBM	1000	V
All pins except high-speed serial and XRES[1]	CDM	500	V
High-speed serial inputs	CDM	400	V

1. The XRES pin on the TW device passes CDM testing at 250V.

SERDES Power Supply Requirements[1, 2, 3]

Over Recommended Operating Conditions

Symbol	Description	Typ.	Max.	Units
Standby (Power Down)				
I_{CCA-SB}	V_{CCA} current (per channel)	3	5	mA
$I_{CCIB-SB}$	Input buffer current (per channel)	—	—	mA
$I_{CCOB-SB}$	Output buffer current (per channel)	—	—	mA
Operating (Data Rate = 3.2 Gbps)				
I_{CCA-OP}	V_{CCA} current (per channel)	68	77	mA
$I_{CCIB-OP}$	Input buffer current (per channel)	5	7	mA
$I_{CCOB-OP}$	Output buffer current (per channel)	19	25	mA
Operating (Data Rate = 2.5 Gbps)				
I_{CCA-OP}	V_{CCA} current (per channel)	66	76	mA
$I_{CCIB-OP}$	Input buffer current (per channel)	4	5	mA
$I_{CCOB-OP}$	Output buffer current (per channel)	15	18	mA
Operating (Data Rate = 1.25 Gbps)				
I_{CCA-OP}	V_{CCA} current (per channel)	62	72	mA
$I_{CCIB-OP}$	Input buffer current (per channel)	4	5	mA
$I_{CCOB-OP}$	Output buffer current (per channel)	15	18	mA
Operating (Data Rate = 250 Mbps)				
I_{CCA-OP}	V_{CCA} current (per channel)	55	65	mA
$I_{CCIB-OP}$	Input buffer current (per channel)	4	5	mA
$I_{CCOB-OP}$	Output buffer current (per channel)	14	17	mA

1. Equalization enabled, pre-emphasis disabled.
2. One quarter of the total quad power (includes contribution from common circuits, all channels in the quad operating, pre-emphasis disabled, equalization enabled).
3. Pre-emphasis adds 20mA to ICCA-OP data.

sysI/O Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS33[2]	3.135	3.3	3.465	—	—	—
LVCMOS25[2]	2.375	2.5	2.625	—	—	—
LVCMOS18	1.71	1.8	1.89	—	—	—
LVCMOS15	1.425	1.5	1.575	—	—	—
LVCMOS12[2]	1.14	1.2	1.26	—	—	—
LVTTL33[2]	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
SSTL15[3]	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, II[2]	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I, II[2]	2.375	2.5	2.625	1.15	1.25	1.35
SSTL33_I, II[2]	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15_I[2]	1.425	1.5	1.575	0.68	0.75	0.9
HSTL18_I, II[2]	1.71	1.8	1.89	0.816	0.9	1.08
LVDS25[2]	2.375	2.5	2.625	—	—	—
MLVDS25[1]	2.375	2.5	2.625	—	—	—
LVPECL33[1, 2]	3.135	3.3	3.465	—	—	—
Mini LVDS	—	—	—	—	—	—
BLVDS25[1, 2]	2.375	2.5	2.625	—	—	—
RSDS25[1, 2]	2.375	2.5	2.625	—	—	—
RSDS25E[1, 2]	2.375	2.5	2.625	—	—	—
TRLVDS	3.14	3.3	3.47	—	—	—
PPLVDS	3.14/2.25	3.3/2.5	3.47/2.75	—	—	—
SSTL15D	1.43	1.5	1.57	—	—	—
SSTL18D_I[2], II[2]	1.71	1.8	1.89	—	—	—
SSTL25D_ I[2], II[2]	2.375	2.5	2.625	—	—	—
SSTL33D_ I[2], II[2]	3.135	3.3	3.465	—	—	—
HSTL15D_ I[2]	1.425	1.5	1.575	—	—	—
HSTL18D_ I[2], II[2]	1.71	1.8	1.89	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.
2. For input voltage compatibility, refer to the "Mixed Voltage Support" section of TN1177, LatticeECP3 sysIO Usage Guide.

LatticeECP3 External Switching Characteristics (Continued)[1, 2]

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Output with Clock and Data (> 10 Bits Wide) Aligned at Pin (GDDRX2_TX.ECLK.Aligned)									
Left and Right Sides									
$t_{DIBGDDR}$	Data Setup Before CLK	ECP3-150EA	—		—		—		ps
$t_{DIAGDDR}$	Data Hold After CLK	ECP3-150EA	—		—		—		ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	—		—		—		MHz
Generic DDRX2 Outputs with Clock and Data Edges Aligned, Without PLL 90-degree shifted clock output[5] (GDDRX2_TX.Aligned)									
$t_{DIBGDDR}$	Data Invalid Before Clock	ECP3-70E/95E	—	200	—	225	—	250	ps
$t_{DIAGDDR}$	Data Invalid After Clock	ECP3-70E/95E	—	200	—	225	—	250	ps
f_{MAX_GDDR}	DDR/DDRX2 Clock Frequency[8]	ECP3-70E/95E	—	500	—	420	—	375	MHz
Generic DDRX2 Output with Clock and Data (> 10 Bits Wide) Centered at Pin Using DQSDLL (GDDRX2_TX.DQS-DLL.Centered)									
Left and Right Sides									
$t_{DVBGDDR}$	Data Valid Before CLK	ECP3-150EA		—		—		—	ns
$t_{DVAGDDR}$	Data Valid After CLK	ECP3-150EA		—		—		—	ns
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	—		—		—		ns
Generic DDRX2 Output with Clock and Data (> 10 Bits Wide) Centered at Pin Using PLL (GDDRX2_TX.PLL.Centered)									
Left and Right Sides									
$t_{DVBGDDR}$	Data Valid Before CLK	ECP3-150EA		—		—		—	ns
$t_{DVAGDDR}$	Data Valid After CLK	ECP3-150EA		—		—		—	ns
f_{MAX_GDDR}	DDRX2 Clock Frequency	ECP3-150EA	—		—		—		ns
Generic DDRX2 Outputs with Clock Edge in the Center of Data Window, with PLL 90-degree Shifted Clock Output[6] (GDDRX2_TX.PLL.Centered)									
$t_{DVBGDDR}$	Data Valid Before CLK	ECP3-70E/95E	300	—	370	—	417	—	ps
$t_{DVAGDDR}$	Data Valid After CLK	ECP3-70E/95E	300	—	370	—	417	—	ps
f_{MAX_GDDR}	DDR/DDRX2 Clock Frequency[8]	ECP3-70E/95E	—	500	—	420	—	375	MHz

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Memory Interface									
DDR/DDR2 SDRAM I/O Pin Parameters (Input Data are Strobe Edge Aligned, Output Strobe Edge is Data Centered)[4]									
t_{DVADQ}	Data Valid After DQS (DDR Read)	ECP3-150EA	—	0.225	—	0.225	—	0.225	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	ECP3-150EA	0.64	—	0.64	—	0.64	—	UI
t_{DQVBS}	Data Valid Before DQS	ECP3-150EA	0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Data Valid After DQS	ECP3-150EA	0.25	—	0.25	—	0.25	—	UI
f_{MAX_DDR}	DDR Clock Frequency	ECP3-150EA	95	200	95	200	95	166	MHz
f_{MAX_DDR2}	DDR2 clock frequency	ECP3-150EA	133	266	133	200	133	166	MHz
t_{DVADQ}	Data Valid After DQS (DDR Read)	ECP3-70E/95E	—	0.225	—	0.225	—	0.225	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	ECP3-70E/95E	0.64	—	0.64	—	0.64	—	UI
t_{DQVBS}	Data Valid Before DQS	ECP3-70E/95E	0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Data Valid After DQS	ECP3-70E/95E	0.25	—	0.25	—	0.25	—	UI
f_{MAX_DDR}	DDR Clock Frequency	ECP3-70E/95E	95	200	95	200	95	133	MHz

LatticeECP3 External Switching Characteristics (Continued)[1, 2]

Over Recommended Commercial Operating Conditions

Parameter	Description	Device	-8		-7		-6		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX_DDR2}	DDR2 Clock Frequency	ECP3-70E/95E	133	266	133	200	133	166	MHz
DDR3 (Using PLL for SCLK) I/O Pin Parameters									
t_{DVADQ}	Data Valid After DQS (DDR Read)	ECP3-150EA	—	0.225	—	0.225	—	0.225	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	ECP3-150EA	0.64	—	0.64	—	0.64	—	UI
t_{DQVBS}	Data Valid Before DQS	ECP3-150EA	0.25	—	0.25	—	0.25	—	UI
t_{DQVAS}	Data Valid After DQS	ECP3-150EA	0.25	—	0.25	—	0.25	—	UI
f_{MAX_DDR3}	DDR3 clock frequency	ECP3-150EA	266	400	266	333	266	300	MHz

1. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the ispLEVER software.
2. General I/O timing numbers based on LVCMOS 2.5, 12mA, 0pf load.
3. Generic DDR timing numbers based on LVDS I/O.
4. DDR timing numbers based on SSTL25. DDR2 timing numbers based on SSTL18.
5. DDR3 timing numbers based on SSTL15.
6. Uses LVDS I/O standard.
7. The current version of software does not support per bank skew numbers; this will be supported in a future release.
8. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.

SERDES High-Speed Data Transmitter[1]

Table 3-6. Serial Output Timing and Levels

Symbol	Description	Frequency	Min.	Typ.	Max.	Units
$V_{TX-DIFF-P-P-1.44}$	Differential swing (1.44V setting)[1, 2]	0.25 to 3.125 Gbps	1150	1440	1730	mV, p-p
$V_{TX-DIFF-P-P-1.35}$	Differential swing (1.35V setting)[1, 2]	0.25 to 3.125 Gbps	1080	1350	1620	mV, p-p
$V_{TX-DIFF-P-P-1.26}$	Differential swing (1.26V setting)[1, 2]	0.25 to 3.125 Gbps	1000	1260	1510	mV, p-p
$V_{TX-DIFF-P-P-1.13}$	Differential swing (1.13V setting)[1, 2]	0.25 to 3.125 Gbps	840	1130	1420	mV, p-p
$V_{TX-DIFF-P-P-1.04}$	Differential swing (1.04V setting)[1, 2]	0.25 to 3.125 Gbps	780	1040	1300	mV, p-p
$V_{TX-DIFF-P-P-0.92}$	Differential swing (0.92V setting)[1, 2]	0.25 to 3.125 Gbps	690	920	1150	mV, p-p
$V_{TX-DIFF-P-P-0.87}$	Differential swing (0.87V setting)[1, 2]	0.25 to 3.125 Gbps	650	870	1090	mV, p-p
$V_{TX-DIFF-P-P-0.78}$	Differential swing (0.78V setting)[1, 2]	0.25 to 3.125 Gbps	585	780	975	mV, p-p
$V_{TX-DIFF-P-P-0.64}$	Differential swing (0.64V setting)[1, 2]	0.25 to 3.125 Gbps	480	640	800	mV, p-p
V_{OCM}	Output common mode voltage	—	V_{CCOB} -0.75	V_{CCOB} -0.60	V_{CCOB} -0.45	V
T_{TX-R}	Rise time (20% to 80%)	—	145	185	265	ps
T_{TX-F}	Fall time (80% to 20%)	—	145	185	265	ps
$Z_{TX-OI-SE}$	Output Impedance 50/75/HiZ Ohms (single ended)	—	-20%	50/75/ Hi Z	+20%	Ohms
R_{LTX-RL}	Return loss (with package)	—	10			dB
$T_{TX-INTRASKEW}$	Lane-to-lane TX skew within a SERDES quad block (intra-quad)	—	—	—	200	ps
$T_{TX-INTERSKEW}$[3]	Lane-to-lane skew between SERDES quad blocks (inter-quad)	—	—	—	1UI +200	ps

1. All measurements are with 50 ohm impedance.
2. See TN1176, LatticeECP3 SERDES/PCS Usage Guide for actual binary settings and the min-max range.
3. Inter-quad skew is between all SERDES channels on the device and requires the use of a low skew internal reference clock.

Table 3-7. Channel Output Jitter

Description	Frequency	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	—	—	0.17	UI, p-p
Random	3.125 Gbps	—	—	0.25	UI, p-p
Total	3.125 Gbps	—	—	0.35	UI, p-p
Deterministic	2.5Gbps	—	—	0.17	UI, p-p
Random	2.5Gbps	—	—	0.20	UI, p-p
Total	2.5Gbps	—	—	0.35	UI, p-p
Deterministic	1.25 Gbps	—	—	0.10	UI, p-p
Random	1.25 Gbps	—	—	0.22	UI, p-p
Total	1.25 Gbps	—	—	0.24	UI, p-p
Deterministic	622 Mbps	—	—	0.10	UI, p-p
Random	622 Mbps	—	—	0.20	UI, p-p
Total	622 Mbps	—	—	0.24	UI, p-p
Deterministic	250 Mbps	—	—	0.10	UI, p-p
Random	250 Mbps	—	—	0.18	UI, p-p
Total	250 Mbps	—	—	0.24	UI, p-p

Note: Values are measured with PRBS 2^7-1, all channels operating, FPGA logic active, I/Os around SERDES pins quiet, reference clock @ 10X mode.

SERDES External Reference Clock

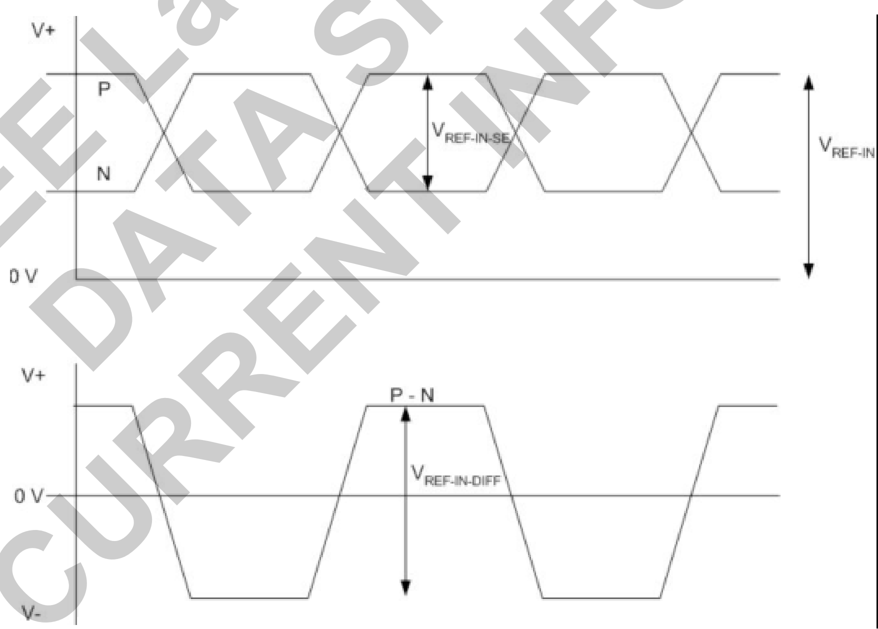
The external reference clock selection and its interface are a critical part of system applications for this product. Table 3-12 specifies reference clock requirements, over the full range of operating conditions.

Table 3-12. External Reference Clock Specification (refclkp/refclkn)

Symbol	Description	Min.	Typ.	Max.	Units
F_{REF}	Frequency range	15	—	320	MHz
$F_{REF-PPM}$	Frequency tolerance[4]	-1000	—	1000	ppm
$V_{REF-IN-SE}$	Input swing, single-ended clock[1]	200	—	V_{CCA}	mV, p-p
$V_{REF-IN-DIFF}$	Input swing, differential clock	200	—	$2*V_{CCA}$	mV, p-p differential
V_{REF-IN}	Input levels	0	—	V_{CCA} + 0.3	V
$V_{REF-CM-AC}$	Input common mode range (AC coupled)[2]	0.125	—	V_{CCA}	V
D_{REF}	Duty cycle[3]	40	—	60	%
T_{REF-R}	Rise time (20% to 80%)	200	500	1000	ps
T_{REF-F}	Fall time (80% to 20%)	200	500	1000	ps
$Z_{REF-IN-TERM-DIFF}$	Differential input termination	-20%	100/2K	+20%	Ohms
$C_{REF-IN-CAP}$	Input capacitance	—	—	7	pF

1. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.
2. When AC coupled, the input common mode range is determined by:
   (Min input level) + (Peak-to-peak input swing)/2 ≤ (Input common mode voltage) ≤ (Max input level) - (Peak-to-peak input swing)/2
3. Measured at 50% amplitude.
4. Depending on the application, the PLL_LOL_SET and CDR_LOL_SET control registers may be adjusted for other tolerance values as described in TN1176, LatticeECP3 SERDES/PCS Usage Guide.

Figure 3-13. SERDES External Reference Clock Waveforms



Gigabit Ethernet/Serial Rapid I/O Type 1/SGMII Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-17. Transmit

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
T_{RF}	Differential rise/fall time	20%-80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential impedance		80	100	120	Ohms
J_{TX_DDJ} [3, 4, 5]	Output data deterministic jitter		—	—	0.10	UI
J_{TX_TJ} [2, 3, 4, 5]	Total output data jitter		—	—	0.24	UI

1. Rise and fall times measured with board trace, connector and approximately 2.5pf load.
2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
3. Jitter values are measured with each CML output AC coupled into a 50-ohm impedance (100-ohm differential impedance).
4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
5. Values are measured at 1.25 Gbps.

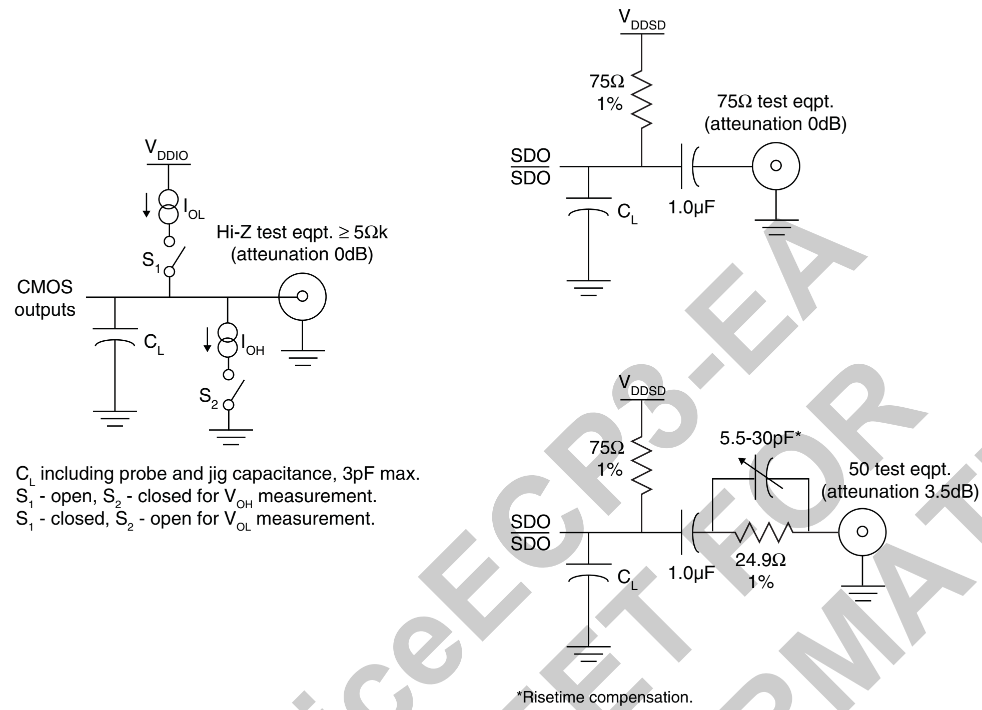
Table 3-18. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
RL_{RX_DIFF}	Differential return loss	From 100 MHz to 1.25 GHz	10	—	—	dB
RL_{RX_CM}	Common mode return loss	From 100 MHz to 1.25 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential termination resistance		80	100	120	Ohms
J_{RX_DJ} [1, 2, 3, 4, 5]	Deterministic jitter tolerance (peak-to-peak)		—	—	0.34	UI
J_{RX_RJ} [1, 2, 3, 4, 5]	Random jitter tolerance (peak-to-peak)		—	—	0.26	UI
J_{RX_SJ} [1, 2, 3, 4, 5]	Sinusoidal jitter tolerance (peak-to-peak)		—	—	0.11	UI
J_{RX_TJ} [1, 2, 3, 4, 5]	Total jitter tolerance (peak-to-peak)		—	—	0.71	UI
T_{RX_EYE}	Receiver eye opening		0.29	—	—	UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-14.
2. Jitter values are measured with each high-speed input AC coupled into a 50-ohm impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.
5. Values are measured at 1.25 Gbps.

Figure 3-15. Test Loads

Test Loads



Timing Jitter Bandpass

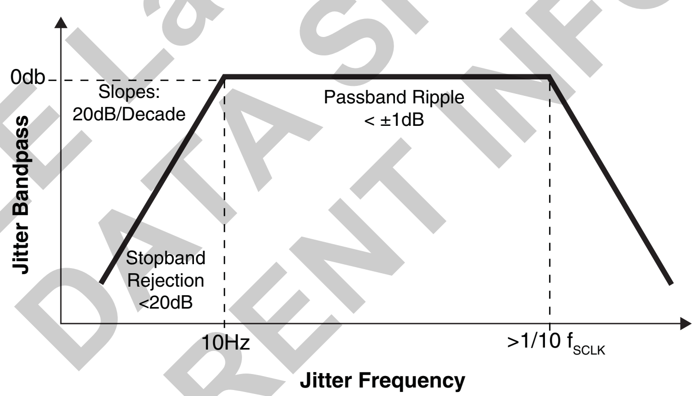
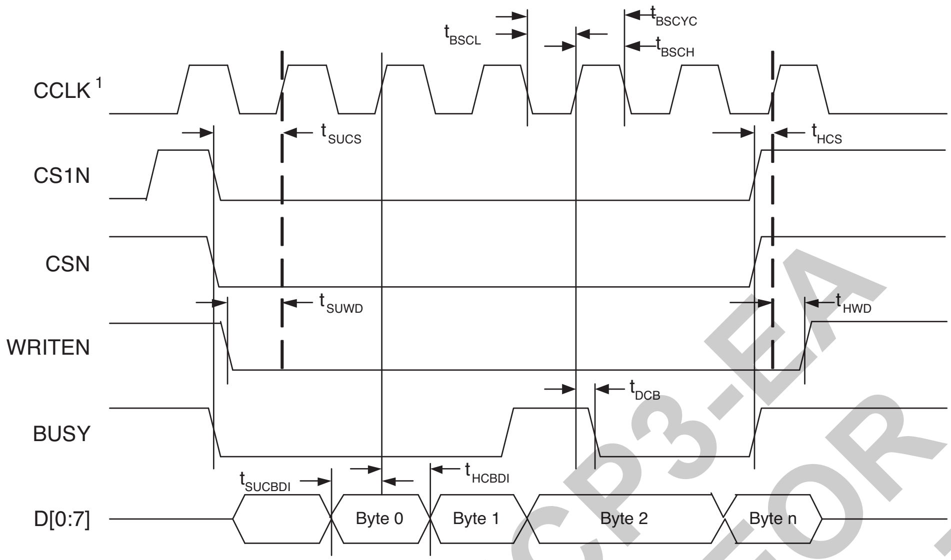


Figure 3-17. sysCONFIG Parallel Port Write Cycle



1. In Master Parallel Mode the FPGA provides CCLK (MCLK). In Slave Parallel Mode the external device provides CCLK.

Figure 3-18. sysCONFIG Master Serial Port Timing

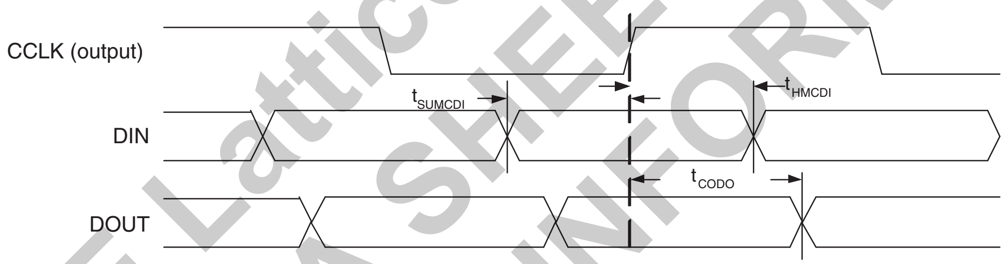


Figure 3-19. sysCONFIG Slave Serial Port Timing

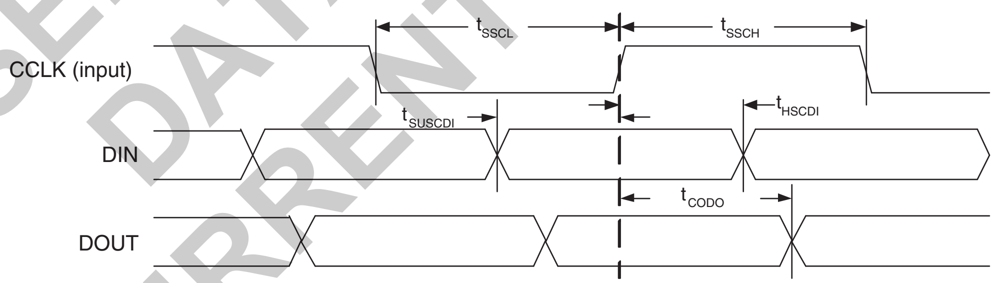
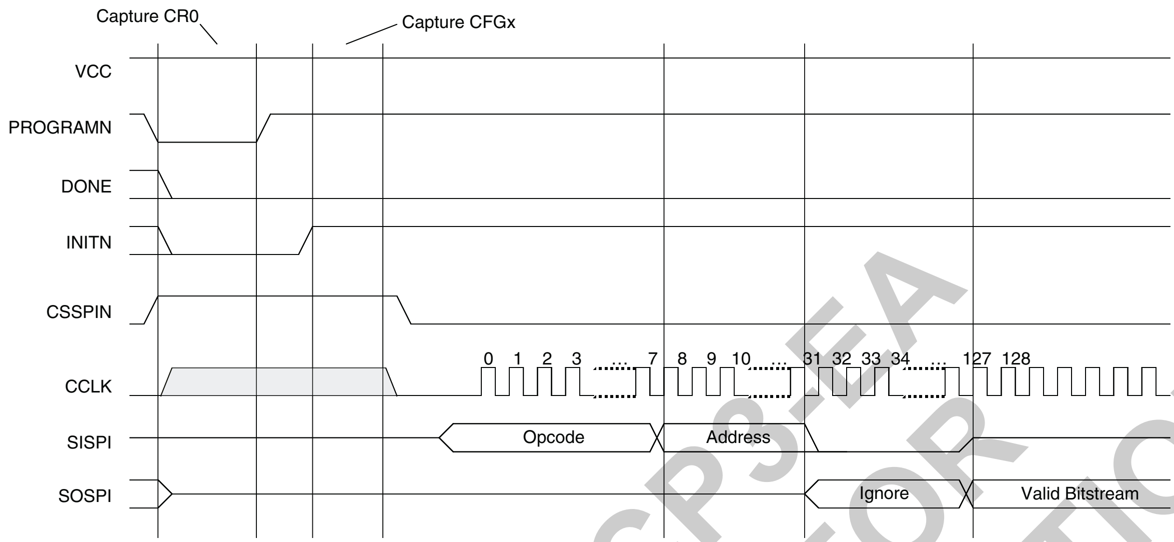


Figure 3-24. Master SPI Configuration Waveforms



Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672I	1.2V	-6	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672I	1.2V	-7	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672I	1.2V	-8	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156I	1.2V	-6	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156I	1.2V	-7	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156I	1.2V	-8	Lead-Free fpBGA	1156	IND	149

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672ITW*	1.2V	-6	Lead-Free fpBGA	672	IND	149
LFE3-150EA-7FN672ITW*	1.2V	-7	Lead-Free fpBGA	672	IND	149
LFE3-150EA-8FN672ITW*	1.2V	-8	Lead-Free fpBGA	672	IND	149
LFE3-150EA-6FN1156ITW*	1.2V	-6	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-7FN1156ITW*	1.2V	-7	Lead-Free fpBGA	1156	IND	149
LFE3-150EA-8FN1156ITW*	1.2V	-8	Lead-Free fpBGA	1156	IND	149

*Note: Specifications for the LFE3-150EA-*sp*FN*pkg*CTW and LFE3-150EA-*sp*FN*pkg*ITW devices, (where *sp* is the speed and *pkg* is the package), are the same as the LFE3-150EA-*sp*FN*pkg*C and LFE3-150EA-*sp*FN*pkg*I devices respectively, except as specified below.

- The CTC (Clock Tolerance Circuit) inside the SERDES hard PCS in the TW device is not functional but it can be bypassed and implemented in soft IP.
- The SERDES XRES pin on the TW device passes CDM testing at 250V.

For Further Information

A variety of technical notes for the LatticeECP3 family are available on the Lattice website at www.latticesemi.com.

- TN1169, LatticeECP3 sysCONFIG Usage Guide
- TN1176, LatticeECP3 SERDES/PCS Usage Guide
- TN1177, LatticeECP3 sysIO Usage Guide
- TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide
- TN1179, LatticeECP3 Memory Usage Guide
- TN1180, LatticeECP3 High-Speed I/O Interface
- TN1181, Power Consumption and Management for LatticeECP3 Devices
- TN1182, LatticeECP3 sysDSP Usage Guide
- TN1184, LatticeECP3 Soft Error Detection (SED) Usage Guide
- TN1189, LatticeECP3 Hardware Checklist

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com

Date	Version	Section	Change Summary
May 2009 (cont.)	01.1 (cont.)	DC and Switching Characteristics (cont.)	Updated timing information
			Updated SERDES minimum frequency.
			Added data to the following tables: External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, Maximum I/O Buffer Speed, DLL Timing, High Speed Data Transmitter, Channel Output Jitter, Typical Building Block Function Performance, Register-to-Register Performance, and Power Supply Requirements.
			Updated Serial Input Data Specifications table.
			Updated Transmit table, Serial Rapid I/O Type 2 Electrical and Timing Characteristics section.
		Pinout Information	Updated Signal Description tables.
			Updated Pin Information Summary tables and added footnote 1.
July 2009	01.2	Multiple	Changed references of “multi-boot” to “dual-boot” throughout the data sheet.
		Architecture	Updated On-Chip Programmable Termination bullets.
			Updated On-Chip Termination Options for Input Modes table.
			Updated On-Chip Termination figure.
		DC and Switching Characterisitcs	Changed min/max data for FREF_PPM and added footnote 4 in SERDES External Reference Clock Specification table.
			Updated SERDES minimum frequency.
		Pinout Information	Corrected MCLK to be I/O and CCLK to be I in Signal Descriptions table
August 2009	01.3	DC and Switching Characterisitcs	Corrected truncated numbers for V_{CCIB} and V_{CCOB} in Recommended Operating Conditions table.
September 2009	01.4	Architecture	Corrected link in sysMEM Memory Block section.
			Updated information for On-Chip Programmable Termination and modified corresponding figure.
			Added footnote 2 to On-Chip Programmable Termination Options for Input Modes table.
			Corrected Per Quadrant Primary Clock Selection figure.
		DC and Switching Characterisitcs	Modified -8 Timing data for 1024x18 True-Dual Port RAM (Read-Before-Write, EBR Output Registers)
			Added ESD Performance table.
			LatticeECP3 External Switching Characteristics table - updated data for $t_{DIBGDDR}$, t_{W_PRI}, t_{W_EDGE} and $t_{SKEW\_EDGE\_DQS}$.
			LatticeECP3 Internal Switching Characteristics table - updated data for t_{COO_PIO} and added footnote #4.
			sysCLOCK PLL Timing table - updated data for f_{OUT}.
			External Reference Clock Specification (refclkp/refclkn) table - updated data for $V_{REF-IN-SE}$ and $V_{REF-IN-DIFF}$
			LatticeECP3 sysCONFIG Port Timing Specifications table - updated data for t_{MWC}.
			Added TRLVDS DC Specification table and diagram.
			Updated Mini LVDS table.
November 2009	01.5	Introduction	Updated Embedded SERDES features.
			Added SONET/SDH to Embedded SERDES protocols.
		Architecture	Updated Figure 2-4, General Purpose PLL Diagram.
			Updated SONET/SDH to SERDES and PCS protocols.