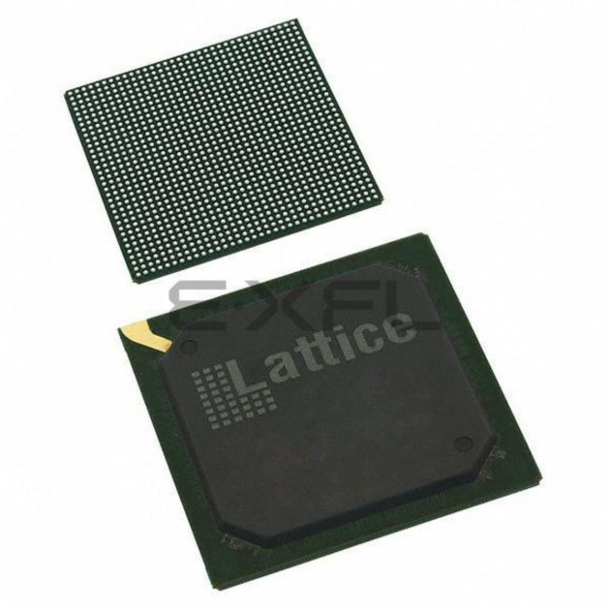

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	11500
Number of Logic Elements/Cells	92000
Total RAM Bits	4526080
Number of I/O	490
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe3-95e-8fn1156c

Introduction

The LatticeECP3™ (EConomy Plus Third generation) family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES and high speed source synchronous interfaces in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 65nm technology making the devices suitable for high-volume, high-speed, low-cost applications.

The LatticeECP3 device family expands look-up-table (LUT) capacity to 149K logic elements and supports up to 486 user I/Os. The LatticeECP3 device family also offers up to 320 18x18 multipliers and a wide range of parallel I/O standards.

The LatticeECP3 FPGA fabric is optimized with high performance and low cost in mind. The LatticeECP3 devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the LatticeECP3 device family supports a broad range of interface standards, including DDR3, XGMII and 7:1 LVDS.

The LatticeECP3 device family also features high speed SERDES with dedicated PCS functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, SMPTE, Ethernet (XAUI, GbE, and SGMII) and CPRI. Transmit Pre-emphasis and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The LatticeECP3 devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

The ispLEVER® design tool suite from Lattice allows large complex designs to be efficiently implemented using the LatticeECP3 FPGA family. Synthesis library support for LatticeECP3 is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP3 device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) ispLeverCORE™ modules for the LatticeECP3 family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

LatticeECP3 Family Data Sheet Architecture

March 2010 — Preliminary Data Sheet DS1021

Architecture Overview

Each LatticeECP3 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sysDSP™ Digital Signal Processing slices, as shown in Figure 2-1. In addition, the LatticeECP3 family contains SERDES Quads on the bottom of the device.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LatticeECP3 devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18Kbit fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, LatticeECP3 devices contain up to two rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The LatticeECP3 devices feature up to 16 embedded 3.2Gbps SERDES (Serializer / Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of four SERDES channels, along with its Physical Coding Sub-layer (PCS) block, creates a quad. The functionality of the SERDES/PCS quads can be controlled by memory cells set during device configuration or by registers that are addressable during device operation. The registers in every quad can be programmed via the SERDES Client Interface (SCI). These quads (up to four) are located at the bottom of the devices.

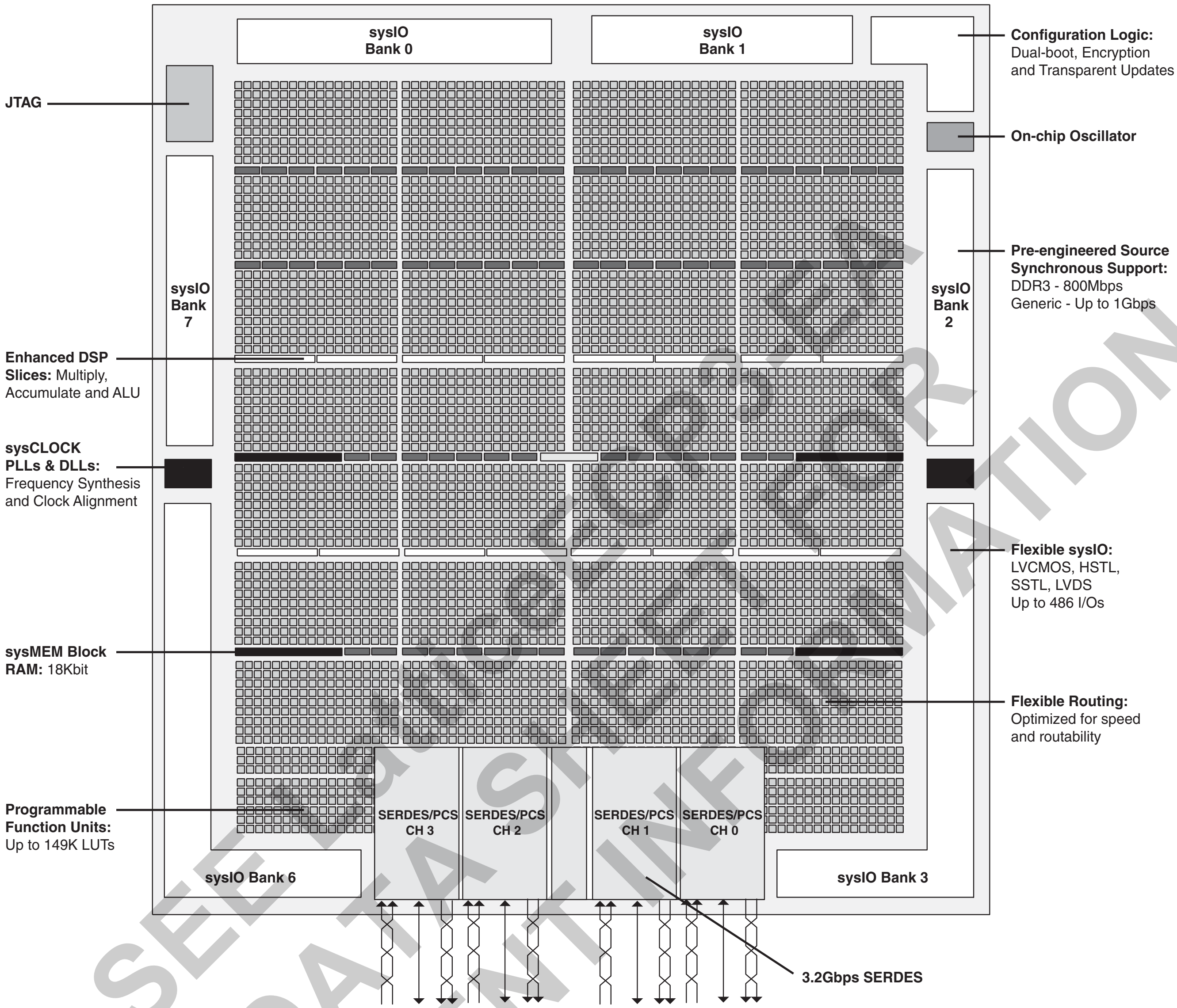
Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the LatticeECP3 devices are arranged in seven banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. 50% of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3.

Other blocks provided include PLLs, DLLs and configuration functions. The LatticeECP3 architecture provides two Delay Locked Loops (DLLs) and up to ten Phase Locked Loops (PLLs). In addition, each LatticeECP3 family member provides two DLLs per device. The PLL and DLL blocks are located at the end of the EBR/DSP rows.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual-boot support is located toward the center of this EBR row. Every device in the LatticeECP3 family supports a sysCONFIG™ port located in the corner between banks one and two, which allows for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The LatticeECP3 devices use 1.2V as their core voltage.

Figure 2-1. Simplified Block Diagram, LatticeECP3-35 Device (Top Level)



Note: There is no Bank 4 or Bank 5 in LatticeECP3 devices.

PFU Blocks

The core of the LatticeECP3 device consists of PFU blocks, which are provided in two forms, the PFU and PFF. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

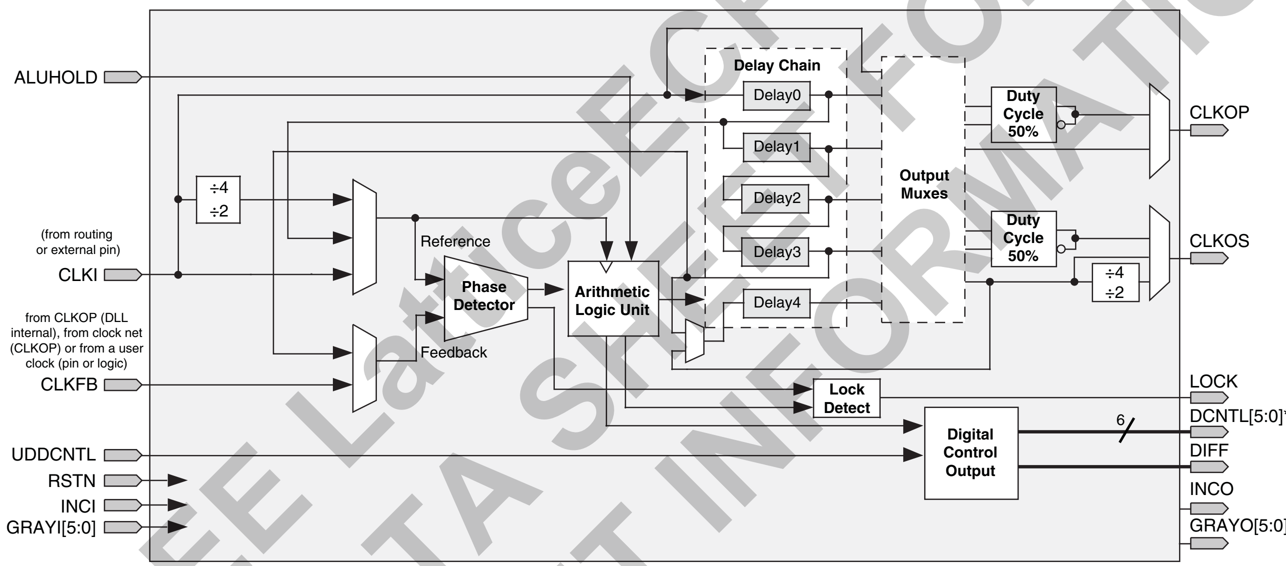
Each PFU block consists of four interconnected slices numbered 0-3 as shown in Figure 2-2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

chain in order to better match the reference and feedback signals. This digital code from the ALU is also transmitted via the Digital Control bus (DCNTL) bus to its associated Slave Delay lines (two per DLL). The ALUHOLD input allows the user to suspend the ALU output at its current value. The UDDCNTL signal allows the user to latch the current value on the DCNTL bus.

The DLL has two clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine delay shift and divider blocks to allow this output to be further modified, if required. The fine delay shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. Both the CLKOS and CLKOP outputs are available with optional duty cycle correction. Divide by two and divide by four frequencies are available at CLKOS. The LOCK output signal is asserted when the DLL is locked. Figure 2-5 shows the DLL block diagram and Table 2-5 provides a description of the DLL inputs and outputs.

The user can configure the DLL for many common functions such as time reference delay mode and clock injection removal mode. Lattice provides primitives in its design tools for these functions.

Figure 2-5. Delay Locked Loop Diagram (DLL)



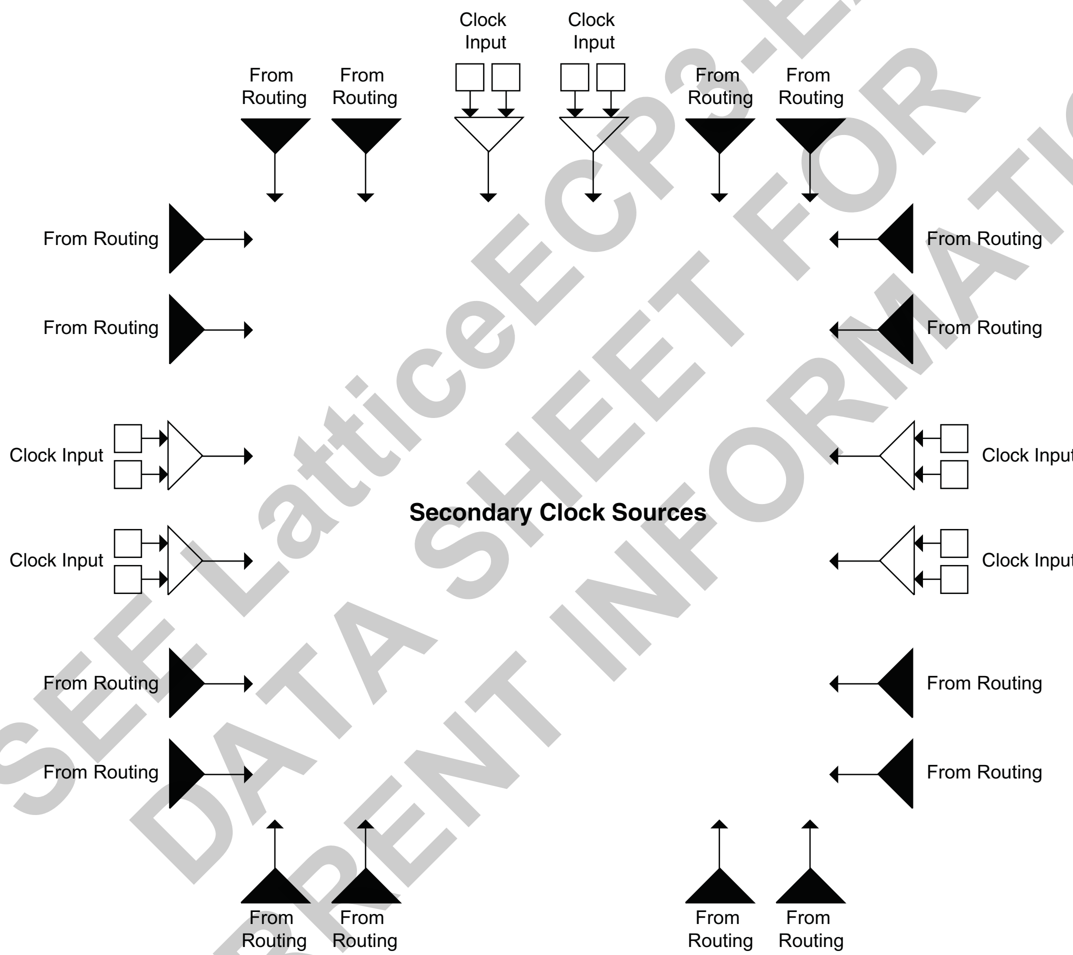
* This signal is not user accessible. This can only be used to feed the slave delay line.

Secondary Clock/Control Sources

LatticeECP3 devices derive eight secondary clock sources (SC0 through SC7) from six dedicated clock input pads and the rest from routing. Figure 2-14 shows the secondary clock sources. All eight secondary clock sources are defined as inputs to a per-region mux SC0-SC7. SC0-SC3 are primary for control signals (CE and/or LSR), and SC4-SC7 are for clock and high fanout data.

In an actual implementation, there is some overlap to maximize routability. In addition to SC0-SC3, SC7 is also an input to the control signals (LSR or CE). SC0-SC2 are also inputs to clocks along with SC4-SC7. High fanout logic signals (LUT inputs) will utilize the X2 and X0 switches where SC0-SC7 are inputs to X2 switches, and SC4-SC7 are inputs to X0 switches. Note that through X0 switches, SC4-SC7 can also access control signals CE/LSR.

Figure 2-14. Secondary Clock Sources



Note: Clock inputs can be configured in differential or single-ended mode.

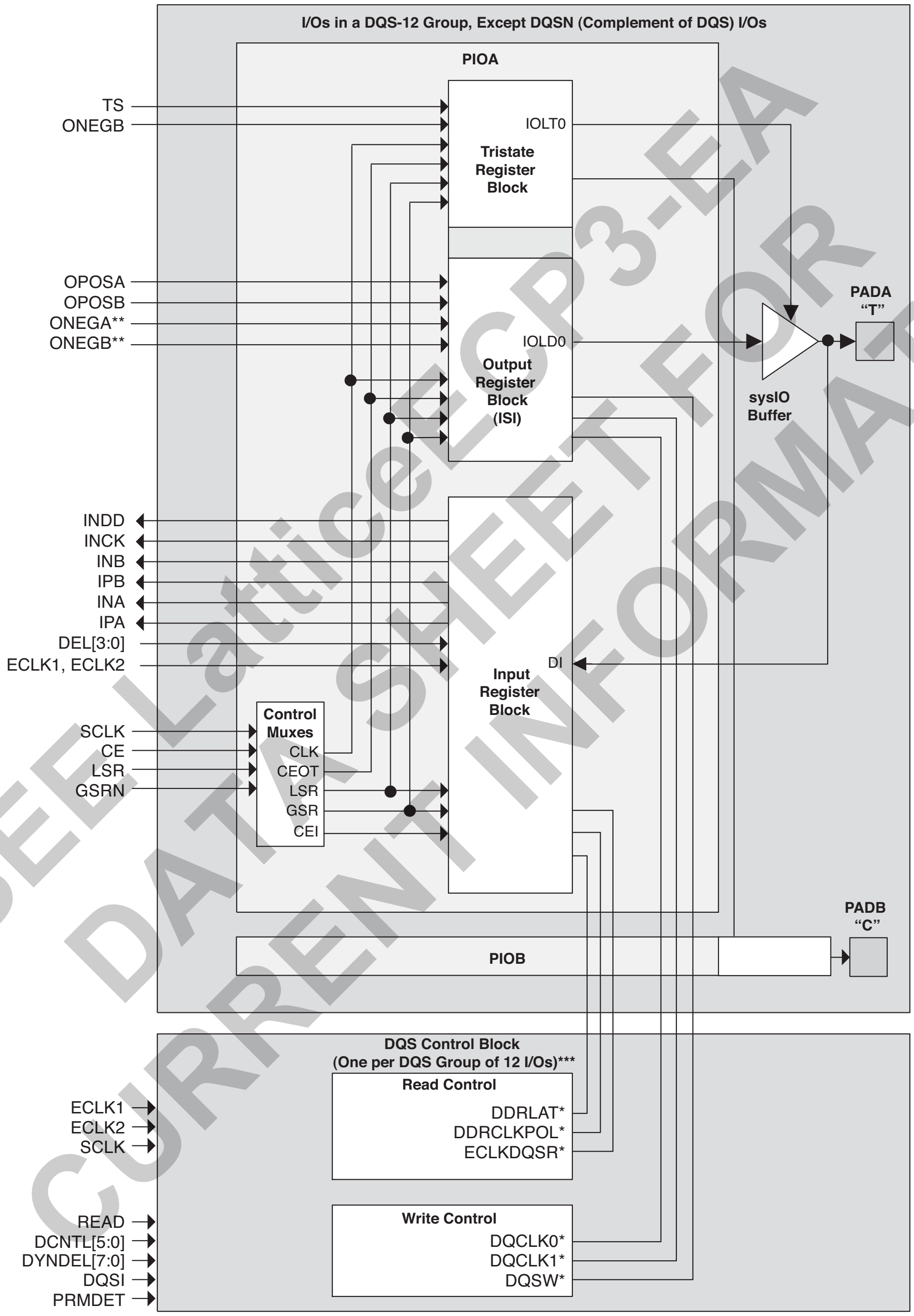
Secondary Clock/Control Routing

Global secondary clock is a secondary clock that is distributed to all regions. The purpose of the secondary clock routing is to distribute the secondary clock sources to the secondary clock regions. Secondary clocks in the LatticeECP3 devices are region-based resources. Certain EBR rows and special vertical routing channels bind the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP slice in the DSP row or the center of the DSP row. Figure 2-15 shows this special vertical routing channel and the 20 secondary clock regions for the LatticeECP3 family of devices. All devices in the LatticeECP3 family have eight

Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O buffers as shown in Figure 2-32. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysI/O buffer and receives input from the buffer. Table 2-11 provides the PIO signal list.

Figure 2-32. PIC Diagram



* Signals are available on left/right/top edges only.
** Signals are available on the left and right sides only
*** Selected PIO.

Please see TN1177, LatticeECP3 sysIO Usage Guide for on-chip termination usage and value ranges.

Equalization Filter

Equalization filtering is available for single-ended inputs on both true and complementary I/Os, and for differential inputs on the true I/Os on the left, right, and top sides. Equalization is required to compensate for the difficulty of sampling alternating logic transitions with a relatively slow slew rate. It is considered the most useful for the Input DDRX2 modes, used in DDR3 memory, LVDS, or TRLVDS signaling. Equalization filter acts as a tunable filter with settings to determine the level of correction. In the LatticeECP3 devices, there are four settings available: 0 (none), 1, 2 and 3. The default setting is 0. The equalization logic resides in the sysI/O buffers, the two bits of setting is set uniquely in each input IOLOGIC block. Therefore, each sysI/O can have a unique equalization setting within a DQS-12 group.

Hot Socketing

LatticeECP3 devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. Please refer to the Hot Socketing Specifications in the DC and Switching Characteristics in this data sheet.

SERDES and PCS (Physical Coding Sublayer)

LatticeECP3 devices feature up to 16 channels of embedded SERDES/PCS arranged in quads at the bottom of the devices supporting up to 3.2Gbps data rate. Figure 2-40 shows the position of the quad blocks for the LatticeECP3-150 devices. Table 2-14 shows the location of available SERDES Quads for all devices.

The LatticeECP3 SERDES/PCS supports a range of popular serial protocols, including:

- PCI Express 1.1
- Ethernet (XAUI, GbE - 1000 Base CS/SX/LX and SGMII)
- Serial RapidIO
- SMPTE SDI (3G, HD, SD)
- CPRI
- SONET/SDH (STS-3, STS-12, STS-48)

Each quad contains four dedicated SERDES for high speed, full duplex serial data transfer. Each quad also has a PCS block that interfaces to the SERDES channels and contains protocol specific digital logic to support the standards listed above. The PCS block also contains interface logic to the FPGA fabric. All PCS logic for dedicated protocol support can also be bypassed to allow raw 8-bit or 10-bit interfaces to the FPGA fabric.

Even though the SERDES/PCS blocks are arranged in quads, multiple baud rates can be supported within a quad with the use of dedicated, per channel ÷1, ÷2 and ÷11 rate dividers. Additionally, multiple quads can be arranged together to form larger data pipes.

For information on how to use the SERDES/PCS blocks to support specific protocols, as well on how to combine multiple protocols and baud rates within a device, please refer to TN1176, LatticeECP3 SERDES/PCS Usage Guide.

Lattice Semiconductor Corporation

LatticeECP3 Family Data Sheet DC and Switching Characteristics

March 2010 Preliminary Data Sheet DS1021

Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC} . . . . -0.5 to 1.32V

Supply Voltage V_{CCAUX} . . . . -0.5 to 3.75V

Supply Voltage V_{CCJ} . . . . -0.5 to 3.75V

Output Supply Voltage V_{CCIO} . . . . -0.5 to 3.75V

Input or I/O Tristate Voltage Applied[4]. . . . . . -0.5 to 3.75V

Storage Temperature (Ambient) . . . . -65 to 150°C

Junction Temperature (Tj) . . . . +125°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to (V_{IHMAX} + 2) volts is permitted for a duration of <20ns.

Recommended Operating Conditions[1]

Symbol	Parameter	Min.	Max.	Units
V_{CC}[2]	Core Supply Voltage	1.14	1.26	V
V_{CCAUX}[2, 4]	Auxiliary Supply Voltage, Terminating Resistor Switching Power Supply (SERDES)	3.135	3.465	V
V_{CCPLL}	PLL Supply Voltage	3.135	3.465	V
V_{CCIO}[2, 3]	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ}[2]	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
V_{REF1} and V_{REF2}	Input Reference Voltage	0.5	1.7	V
V_{TT}[5]	Termination Voltage	0.5	1.3125	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature, Industrial Operation	-40	100	°C
SERDES External Power Supply[6]				
V_{CCIB}	Input Buffer Power Supply (1.2V)	1.14	1.26	V
	Input Buffer Power Supply (1.5V)	1.425	1.575	V
V_{CCOB}	Output Buffer Power Supply (1.2V)	1.14	1.26	V
	Output Buffer Power Supply (1.5V)	1.425	1.575	V
V_{CCA}	Transmit, Receive, PLL and Reference Clock Buffer Power Supply	1.14	1.26	V

1. For correct operation, all supplies except V_{REF} and V_{TT} must be held in their valid operation range. This is true independent of feature usage.
2. If V_{CCIO} or V_{CCJ} is set to 1.2V, they must be connected to the same power supply as V_{CC}. If V_{CCIO} or V_{CCJ} is set to 3.3V, they must be connected to the same power supply as V_{CCAUX}.
3. See recommended voltages by I/O standard in subsequent table.
4. V_{CCAUX} ramp rate must not exceed 30mV/µs during power-up when transitioning between 0V and 3.3V.
5. If not used, V_{TT} should be left floating.
6. See TN1176, LatticeECP3 SERDES/PCS Usage Guide for information on board considerations for SERDES power supplies.

LatticeECP3 Internal Switching Characteristics[1, 2]

Over Recommended Commercial Operating Conditions

Parameter	Description	-8		-7		-6		Units.
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t_{LUT4_PFU}	LUT4 delay (A to D inputs to F output)	—	0.147	—	0.163	—	0.179	ns
t_{LUT6_PFU}	LUT6 delay (A to D inputs to OFX output)	—	0.273	—	0.307	—	0.342	ns
t_{LSR_PFU}	Set/Reset to output of PFU (Asynchronus)	—	0.593	—	0.674	—	0.756	ns
t_{LSRREC_PFU}	Asynchronous Set/Reset recovery time for PFU Logic	—	0.298	—	0.345	—	0.391	ns
t_{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.134	—	0.144	—	0.153	—	ns
t_{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	-0.097	—	-0.103	—	-0.109	—	ns
t_{SUD_PFU}	Clock to D input setup time	0.061	—	0.068	—	0.075	—	ns
t_{HD_PFU}	Clock to D input hold time	0.019	—	0.013	—	0.015	—	ns
t_{CK2Q_PFU}	Clock to Q delay, (D-type Register Configuration)	—	0.243	—	0.273	—	0.303	ns
PFU Dual Port Memory Mode Timing								
t_{CORAM_PFU}	Clock to Output (F Port)	—	0.710	—	0.803	—	0.897	ns
t_{SUDATA_PFU}	Data Setup Time	-0.137	—	-0.155	—	-0.174	—	ns
t_{HDATA_PFU}	Data Hold Time	0.188	—	0.217	—	0.246	—	ns
t_{SUADDR_PFU}	Address Setup Time	-0.227	—	-0.257	—	-0.286	—	ns
t_{HADDR_PFU}	Address Hold Time	0.240	—	0.275	—	0.310	—	ns
t_{SUWREN_PFU}	Write/Read Enable Setup Time	-0.055	—	-0.055	—	-0.063	—	ns
t_{HWREN_PFU}	Write/Read Enable Hold Time	0.059	—	0.059	—	0.071	—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t_{IN_PIO}	Input Buffer Delay (LVCMOS25)	—	0.423	—	0.466	—	0.508	ns
t_{OUT_PIO}	Output Buffer Delay (LVCMOS25)	—	1.115	—	1.155	—	1.196	ns
IOLOGIC Input/Output Timing								
t_{SUI_PIO}	Input Register Setup Time (Data Before Clock)	0.956	—	1.124	—	1.293	—	ns
t_{HI_PIO}	Input Register Hold Time (Data after Clock)	0.313	—	0.395	—	0.378	—	ns
t_{COO_PIO}	Output Register Clock to Output Delay[4]	—	1.455	—	1.564	—	1.674	ns
t_{SUCE_PIO}	Input Register Clock Enable Setup Time	0.220	—	0.185	—	0.150	—	ns
t_{HCE_PIO}	Input Register Clock Enable Hold Time	-0.085	—	-0.072	—	-0.058	—	ns
t_{SULSR_PIO}	Set/Reset Setup Time	0.117	—	0.103	—	0.088	—	ns
t_{HLSR_PIO}	Set/Reset Hold Time	-0.107	—	-0.094	—	-0.081	—	ns
EBR Timing								
t_{CO_EBR}	Clock (Read) to output from Address or Data	—	2.78	—	2.89	—	2.99	ns
t_{COO_EBR}	Clock (Write) to output from EBR output Register	—	0.31	—	0.32	—	0.33	ns
t_{SUDATA_EBR}	Setup Data to EBR Memory	-0.218	—	-0.227	—	-0.237	—	ns
t_{HDATA_EBR}	Hold Data to EBR Memory	0.249	—	0.257	—	0.265	—	ns
t_{SUADDR_EBR}	Setup Address to EBR Memroy	-0.071	—	-0.070	—	-0.068	—	ns
t_{HADDR_EBR}	Hold Address to EBR Memory	0.118	—	0.098	—	0.077	—	ns
t_{SUWREN_EBR}	Setup Write/Read Enable to PFU Memory	-0.107	—	-0.106	—	-0.106	—	ns

LatticeECP3 Internal Switching Characteristics[1, 2] (Continued)

Over Recommended Commercial Operating Conditions

Parameter	Description	-8		-7		-6		Units.
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{HWREN_EBR}	Hold Write/Read Enable to PFU Memory	0.141	—	0.145	—	0.149	—	ns
t_{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.087		0.096		0.104		ns
t_{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.066		-0.080		-0.094		ns
t_{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register	-0.071		-0.070		-0.068		ns
t_{HBE_EBR}	Byte Enable Hold Time to EBR Output Register	0.118		0.098		0.077		ns
DSP Block Timing[3]								
t_{SUI_DSP}	Input Register Setup Time	0.32	—	0.36	—	0.39	—	ns
t_{HI_DSP}	Input Register Hold Time	-0.17	—	-0.19	—	-0.21	—	ns
t_{SUP_DSP}	Pipeline Register Setup Time	2.23	—	2.30	—	2.37	—	ns
t_{HP_DSP}	Pipeline Register Hold Time	-1.02	—	-1.09	—	-1.15	—	ns
t_{SUO_DSP}	Output Register Setup Time	3.09	—	3.22	—	3.34	—	ns
t_{HO_DSP}	Output Register Hold Time	-1.67	—	-1.76	—	-1.84	—	ns
t_{COI_DSP}	Input Register Clock to Output Time	—	3.68	—	4.03	—	4.38	ns
t_{COP_DSP}	Pipeline Register Clock to Output Time	—	1.30	—	1.47	—	1.64	ns
t_{COO_DSP}	Output Register Clock to Output Time	—	0.58	—	0.60	—	0.62	ns
t_{SUOPT_DSP}	Opcode Register Setup Time	0.31	—	0.35	—	0.39	—	ns
t_{HOPT_DSP}	Opcode Register Hold Time	-0.20	—	-0.24	—	-0.27	—	ns
t_{SUDATA_DSP}	Cascade_data through ALU to Output Register Setup Time	1.55	—	1.67	—	1.78	—	ns
t_{HPDATA_DSP}	Cascade_data through ALU to Output Register Hold Time	-0.44	—	-0.53	—	-0.61	—	ns

1. Internal parameters are characterized but not tested on every device.
2. Commercial timing numbers are shown. Industrial timing numbers are typically slower and can be extracted from the ispLEVER software.
3. DSP slice is configured in Multiply Add/Sub 18x18 mode.
4. The output register is in Flip-flop mode.

LatticeECP3 Maximum I/O Buffer Speed (Continued)[1, 2, 3, 4, 5, 6]

Over Recommended Operating Conditions

Buffer	Description	Max.	Units
PCI33	PCI, V_{CCIO} = 3.3V	66	MHz

1. These maximum speeds are characterized but not tested on every device.
2. Maximum I/O speed for differential output standards emulated with resistors depends on the layout.
3. LVCMOS timing is measured with the load specified in the Switching Test Conditions table of this document.
4. All speeds are measured at fast slew.
5. Actual system operation may vary depending on user logic implementation.
6. Maximum data rate equals 2 times the clock rate when utilizing DDR.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Clock	Min.	Typ.	Max.	Units
f_{IN}	Input clock frequency (CLKI, CLKFB)		Edge clock	2	—	500	MHz
			Primary clock	2	—	420	MHz
f_{OUT}	Output clock frequency (CLKOP, CLKOS)		Edge clock	4	—	500	MHz
			Primary clock	4	—	420	MHz
f_{OUT1}	K-Divider output frequency	CLKOK		0.03125	—	250	MHz
f_{OUT2}	K2-Divider output frequency	CLKOK2		0.667	—	166	MHz
f_{VCO}	PLL VCO frequency			500	—	1000	MHz
f_{PFD}[3]	Phase detector input frequency		Edge clock	2	—	500	MHz
			Primary clock	2	—	420	MHz
AC Characteristics							
t_{PA}	Programmable delay unit			65	130	260	ps
t_{DT}	Output clock duty cycle (CLKOS, at 50% setting)		Edge clock	45	50	55	%
		$f_{OUT} \leq 250$ MHz	Primary clock	45	50	55	%
		$f_{OUT} > 250$MHz	Primary clock	30	50	70	%
t_{CPA}	Coarse phase shift error (CLKOS, at all settings)			-5	0	+5	% of period
t_{OPW}	Output clock pulse width high or low (CLKOS)			1.8	—	—	ns
t_{OPJIT}[1]	Output clock period jitter	$f_{OUT} \geq 420$MHz		—	—	200	p-p
		420MHz > $f_{OUT} \geq 100$MHz		—	—	250	p-p
		$f_{OUT} < 100$MHz		—	—	0.025	UIPP
t_{SK}	Input clock to output clock skew when N/M = integer			—	—	500	p-p
t_{LOCK}[2]	Lock time	2 to 25 MHz		—	—	200	us
		25 to 500 MHz		—	—	50	us
t_{UNLOCK}	Reset to PLL unlock time to ensure fast reset			—	—	50	ns
t_{HI}	Input clock high time	90% to 90%		0.5	—	—	ns
t_{LO}	Input clock low time	10% to 10%		0.5	—	—	ns
t_{IPJIT}	Input clock period jitter			—	—	400	p-p
t_{RST}	Reset signal pulse width high, RESETM, RESETK			10	—	—	ns
	Reset signal pulse width high, CNTRST			500	—	—	ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for $f_{PFD} > 4$MHz. For $f_{PFD} < 4$MHz, the jitter numbers may not be met in certain conditions. Please contact the factory for $f_{PFD} < 4$MHz.

SERDES High Speed Data Receiver

Table 3-9. Serial Input Data Specifications

Symbol	Description		Min.	Typ.	Max.	Units
$RX\text{-}CID_S$	Stream of nontransitions[1] (CID = Consecutive Identical Digits) @ 10^{-12} BER	3.125G	—	—	136	Bits
		2.5G	—	—	144	
		1.485G	—	—	160	
		622M	—	—	204	
		270M	—	—	228	
		155M	—	—	296	
$V_{RX-DIFF-S}$	Differential input sensitivity		150	—	1760	mV, p-p
V_{RX-IN}	Input levels		0	—	V_{CCA} +0.5[4]	V
$V_{RX-CM-DC}$	Input common mode range (DC coupled)		0.6	—	V_{CCA}	V
$V_{RX-CM-AC}$	Input common mode range (AC coupled)[3]		0.1	—	V_{CCA} +0.2	V
$T_{RX-RELOCK}$	SCDR re-lock time[2]		—	1000	—	Bits
$Z_{RX-TERM}$	Input termination 50/75 Ohm/High Z		-20%	50/75/HiZ	+20%	Ohms
RL_{RX-RL}	Return loss (without package)		10	—	—	dB

1. This is the number of bits allowed without a transition on the incoming data stream when using DC coupling.
2. This is the typical number of bit times to re-lock to a new phase or frequency within +/- 300 ppm, assuming 8b10b encoded data.
3. AC coupling is used to interface to LVPECL and LVDS. LVDS interfaces are found in laser drivers and Fibre Channel equipment. LVDS interfaces are generally found in 622 Mbps SERDES devices.
4. Up to 1.76V.

Input Data Jitter Tolerance

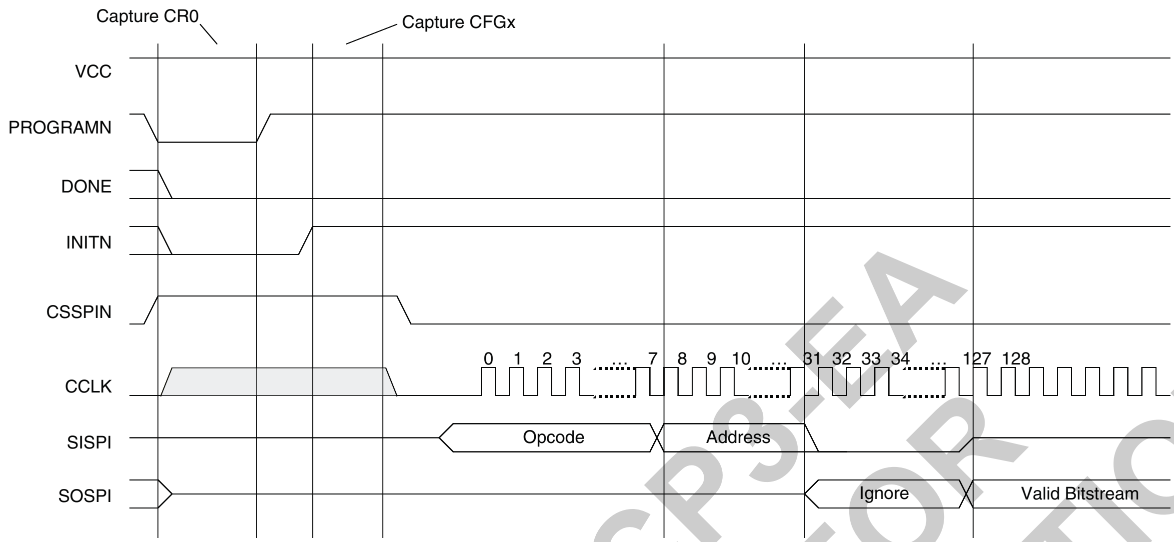
A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

Table 3-10. Receiver Total Jitter Tolerance Specification

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	2.5 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	1.25 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	622 Mbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p

Note: Values are measured with CJPAT, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.

Figure 3-24. Master SPI Configuration Waveforms



Signal Descriptions (Cont.)

Signal Name	I/O	Description
[LOC]DQS[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQS, num = ball function number.
[LOC]DQ[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQ, associated DQS number.
Test and Programming (Dedicated Pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ	—	Power supply pin for JTAG Test Access Port.
Configuration Pads (Used During sysCONFIG)		
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. It is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. It is a dedicated pin.
CCLK	I	Input Configuration Clock for configuring an FPGA in Slave SPI, Serial, and CPU modes. It is a dedicated pin.
MCLK	I/O	Output Configuration Clock for configuring an FPGA in SPI, SPIm, and Master configuration modes.
BUSY/SISPI	O	Parallel configuration mode busy indicator. SPI/SPIm mode data output.
CSN/SN/OEN	I/O	Parallel configuration mode active-low chip select. Slave SPI chip select. Parallel burst Flash output enable.
CS1N/HOLDN/RDY	I	Parallel configuration mode active-low chip select. Slave SPI hold input.
WRITEN	I	Write enable for parallel configuration modes.
DOUT/CSON/CSSPI1N	O	Serial data output. Chip select output. SPI/SPIm mode chip select.
D[0]/SPIFASTN	I/O	sysCONFIG Port Data I/O for Parallel mode. Open drain during configuration.
		sysCONFIG Port Data I/O for SPI or SPIm. When using the SPI or SPIm mode, this pin should either be tied high or low, must not be left floating. Open drain during configuration.
D1	I/O	Parallel configuration I/O. Open drain during configuration.
D2	I/O	Parallel configuration I/O. Open drain during configuration.
D3/SI	I/O	Parallel configuration I/O. Slave SPI data input. Open drain during configuration.
D4/SO	I/O	Parallel configuration I/O. Slave SPI data output. Open drain during configuration.
D5	I/O	Parallel configuration I/O. Open drain during configuration.
D6/SPID1	I/O	Parallel configuration I/O. SPI/SPIm data input. Open drain during configuration.

Pin Information Summary (Cont.)

Pin Information Summary		ECP3-17EA		ECP3-35EA		
Pin Type		256 ftBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA
Emulated Differential I/O per Bank	Bank 0	13	18	13	21	24
	Bank 1	7	12	7	18	18
	Bank 2	2	4	1	8	8
	Bank 3	4	13	5	20	19
	Bank 6	5	13	6	22	20
	Bank 7	6	10	6	11	13
	Bank 8	12	12	12	12	12
Highspeed Differential I/O per Bank	Bank 0	0	0	0	0	0
	Bank 1	0	0	0	0	0
	Bank 2	2	3	3	6	6
	Bank 3	5	9	4	9	12
	Bank 6	5	9	4	11	12
	Bank 7	5	8	5	9	10
	Bank 8	0	0	0	0	0
Total Single Ended/ Total Differential I/O per Bank	Bank 0	26/13	36/18	26/13	42/21	48/24
	Bank 1	14/7	24/12	14/7	36/18	36/18
	Bank 2	8/4	14/7	8/4	28/14	28/14
	Bank 3	18/9	44/22	18/9	58/29	63/31
	Bank 6	20/10	44/22	20/10	67/33	65/32
	Bank 7	23/11	36/18	23/11	40/20	46/23
	Bank 8	24/12	24/12	24/12	24/12	24/12
DDR Groups Bonded per Bank	Bank 0	2	3	2	3	4
	Bank 1	1	2	1	3	3
	Bank 2	0	1	0	2	2
	Bank 3	1	3	1	3	4
	Bank 6	1	3	1	4	4
	Bank 7	1	2	1	3	3
	Configuration Bank 8	0	0	0	0	0
SERDES Quads		1	1	1	1	1

1. These pins must remain floating on the board.

LatticeECP3 Devices, Lead-Free Packaging

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Commercial

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-17EA-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	17
LFE3-17EA-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	17
LFE3-17EA-8FTN256C	1.2V	-8	Lead-Free ftBGA	256	COM	17
LFE3-17EA-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	17
LFE3-17EA-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	17
LFE3-17EA-8FN484C	1.2V	-8	Lead-Free fpBGA	484	COM	17

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-35EA-6FTN256C	1.2V	-6	Lead-Free ftBGA	256	COM	33
LFE3-35EA-7FTN256C	1.2V	-7	Lead-Free ftBGA	256	COM	33
LFE3-35EA-8FTN256C	1.2V	-8	Lead-Free ftBGA	256	COM	33
LFE3-35EA-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	33
LFE3-35EA-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	33
LFE3-35EA-8FN484C	1.2V	-8	Lead-Free fpBGA	484	COM	33
LFE3-35EA-6FN672C	1.2V	-6	Lead-Free fpBGA	672	COM	33
LFE3-35EA-7FN672C	1.2V	-7	Lead-Free fpBGA	672	COM	33
LFE3-35EA-8FN672C	1.2V	-8	Lead-Free fpBGA	672	COM	33

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-70EA-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	67
LFE3-70EA-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	67
LFE3-70EA-8FN484C	1.2V	-8	Lead-Free fpBGA	484	COM	67
LFE3-70EA-6FN672C	1.2V	-6	Lead-Free fpBGA	672	COM	67
LFE3-70EA-7FN672C	1.2V	-7	Lead-Free fpBGA	672	COM	67
LFE3-70EA-8FN672C	1.2V	-8	Lead-Free fpBGA	672	COM	67
LFE3-70EA-6FN1156C	1.2V	-6	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-7FN1156C	1.2V	-7	Lead-Free fpBGA	1156	COM	67
LFE3-70EA-8FN1156C	1.2V	-8	Lead-Free fpBGA	1156	COM	67

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-70E-6FN484C[1]	1.2V	-6	Lead-Free fpBGA	484	COM	67
LFE3-70E-7FN484C[1]	1.2V	-7	Lead-Free fpBGA	484	COM	67
LFE3-70E-8FN484C[1]	1.2V	-8	Lead-Free fpBGA	484	COM	67
LFE3-70E-6FN672C[1]	1.2V	-6	Lead-Free fpBGA	672	COM	67
LFE3-70E-7FN672C[1]	1.2V	-7	Lead-Free fpBGA	672	COM	67
LFE3-70E-8FN672C[1]	1.2V	-8	Lead-Free fpBGA	672	COM	67
LFE3-70E-6FN1156C[1]	1.2V	-6	Lead-Free fpBGA	1156	COM	67
LFE3-70E-7FN1156C[1]	1.2V	-7	Lead-Free fpBGA	1156	COM	67
LFE3-70E-8FN1156C[1]	1.2V	-8	Lead-Free fpBGA	1156	COM	67

1.This device has associated errata. View www.latticesemi.com/documents/ds1021.zip for a description of the errata.

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-95EA-6FN484C	1.2V	-6	Lead-Free fpBGA	484	COM	92
LFE3-95EA-7FN484C	1.2V	-7	Lead-Free fpBGA	484	COM	92
LFE3-95EA-8FN484C	1.2V	-8	Lead-Free fpBGA	484	COM	92
LFE3-95EA-6FN672C	1.2V	-6	Lead-Free fpBGA	672	COM	92
LFE3-95EA-7FN672C	1.2V	-7	Lead-Free fpBGA	672	COM	92
LFE3-95EA-8FN672C	1.2V	-8	Lead-Free fpBGA	672	COM	92
LFE3-95EA-6FN1156C	1.2V	-6	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-7FN1156C	1.2V	-7	Lead-Free fpBGA	1156	COM	92
LFE3-95EA-8FN1156C	1.2V	-8	Lead-Free fpBGA	1156	COM	92

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-95E-6FN484C[1]	1.2V	-6	Lead-Free fpBGA	484	COM	92
LFE3-95E-7FN484C[1]	1.2V	-7	Lead-Free fpBGA	484	COM	92
LFE3-95E-8FN484C[1]	1.2V	-8	Lead-Free fpBGA	484	COM	92
LFE3-95E-6FN672C[1]	1.2V	-6	Lead-Free fpBGA	672	COM	92
LFE3-95E-7FN672C[1]	1.2V	-7	Lead-Free fpBGA	672	COM	92
LFE3-95E-8FN672C[1]	1.2V	-8	Lead-Free fpBGA	672	COM	92
LFE3-95E-6FN1156C[1]	1.2V	-6	Lead-Free fpBGA	1156	COM	92
LFE3-95E-7FN1156C[1]	1.2V	-7	Lead-Free fpBGA	1156	COM	92
LFE3-95E-8FN1156C[1]	1.2V	-8	Lead-Free fpBGA	1156	COM	92

1.This device has associated errata. View www.latticesemi.com/documents/ds1021.zip for a description of the errata.

Part Number	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE3-150EA-6FN672C	1.2V	-6	Lead-Free fpBGA	672	COM	149
LFE3-150EA-7FN672C	1.2V	-7	Lead-Free fpBGA	672	COM	149
LFE3-150EA-8FN672C	1.2V	-8	Lead-Free fpBGA	672	COM	149
LFE3-150EA-6FN1156C	1.2V	-6	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-7FN1156C	1.2V	-7	Lead-Free fpBGA	1156	COM	149
LFE3-150EA-8FN1156C	1.2V	-8	Lead-Free fpBGA	1156	COM	149

Date	Version	Section	Change Summary
May 2009 (cont.)	01.1 (cont.)	DC and Switching Characteristics (cont.)	Updated timing information
			Updated SERDES minimum frequency.
			Added data to the following tables: External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, Maximum I/O Buffer Speed, DLL Timing, High Speed Data Transmitter, Channel Output Jitter, Typical Building Block Function Performance, Register-to-Register Performance, and Power Supply Requirements.
			Updated Serial Input Data Specifications table.
			Updated Transmit table, Serial Rapid I/O Type 2 Electrical and Timing Characteristics section.
		Pinout Information	Updated Signal Description tables.
			Updated Pin Information Summary tables and added footnote 1.
July 2009	01.2	Multiple	Changed references of “multi-boot” to “dual-boot” throughout the data sheet.
		Architecture	Updated On-Chip Programmable Termination bullets.
			Updated On-Chip Termination Options for Input Modes table.
			Updated On-Chip Termination figure.
		DC and Switching Characterisitcs	Changed min/max data for FREF_PPM and added footnote 4 in SERDES External Reference Clock Specification table.
			Updated SERDES minimum frequency.
		Pinout Information	Corrected MCLK to be I/O and CCLK to be I in Signal Descriptions table
August 2009	01.3	DC and Switching Characterisitcs	Corrected truncated numbers for V_{CCIB} and V_{CCOB} in Recommended Operating Conditions table.
September 2009	01.4	Architecture	Corrected link in sysMEM Memory Block section.
			Updated information for On-Chip Programmable Termination and modified corresponding figure.
			Added footnote 2 to On-Chip Programmable Termination Options for Input Modes table.
			Corrected Per Quadrant Primary Clock Selection figure.
		DC and Switching Characterisitcs	Modified -8 Timing data for 1024x18 True-Dual Port RAM (Read-Before-Write, EBR Output Registers)
			Added ESD Performance table.
			LatticeECP3 External Switching Characteristics table - updated data for $t_{DIBGDDR}$, t_{W_PRI}, t_{W_EDGE} and $t_{SKEW\_EDGE\_DQS}$.
			LatticeECP3 Internal Switching Characteristics table - updated data for t_{COO_PIO} and added footnote #4.
			sysCLOCK PLL Timing table - updated data for f_{OUT}.
			External Reference Clock Specification (refclkp/refclkn) table - updated data for $V_{REF-IN-SE}$ and $V_{REF-IN-DIFF}$
			LatticeECP3 sysCONFIG Port Timing Specifications table - updated data for t_{MWC}.
			Added TRLVDS DC Specification table and diagram.
			Updated Mini LVDS table.
November 2009	01.5	Introduction	Updated Embedded SERDES features.
			Added SONET/SDH to Embedded SERDES protocols.
		Architecture	Updated Figure 2-4, General Purpose PLL Diagram.
			Updated SONET/SDH to SERDES and PCS protocols.

Date	Version	Section	Change Summary
November 2009 (cont.)	01.5 (cont.)	Architecture (cont.)	Updated Table 2-13, SERDES Standard Support to include SONET/ SDH and updated footnote 2.
		DC and Switching Characterisitcs	Added footnote to ESD Performance table.
			Updated SERDES Power Supply Requirements table and footnotes.
			Updated Maximum I/O Buffer Speed table.
			Updated Pin-to-Pin Peformance table.
			Updated sysCLOCK PLL Timing table.
			Updated DLL timing table.
			Updated High-Speed Data Transmitter tables.
			Updated High-Speed Data Receiver table.
			Updated footnote for Receiver Total Jitter Tolerance Specification table.
			Updated Periodic Receiver Jitter Tolerance Specification table.
			Updated SERDES External Reference Clock Specification table.
			Updated PCI Express Electrical and Timing AC and DC Characteristics.
			Deleted Reference Clock table for PCI Express Electrical and Timing AC and DC Characteristics.
			Updated SMPTE AC/DC Characteristics Transmit table.
			Updated Mini LVDS table.
			Updated RSDS table.
			Added Supply Current (Standby) table for EA devices.
			Updated Internal Switching Characteristics table.
			Updated Register-to-Register Performance table.
			Added HDMI Electrical and Timing Characteristics data.
			Updated Family Timing Adders table.
			Updated sysCONFIG Port Timing Specifications table.
			Updated Recommended Operating Conditions table.
			Updated Hot Socket Specifications table.
			Updated Single-Ended DC table.
			Updated TRLVDS table and figure.
			Updated Serial Data Input Specifications table.
			Updated HDMI Transmit and Receive table.
		Ordering Information	Added LFE3-150EA “TW” devices and footnotes to the Commercial and Industrial tables.
March 2010	01.6	Architecture	Added Read-Before-Write information.
		DC and Switching Characteristics	Added footnote #6 to Maximum I/O Buffer Speed table.
			Corrected minimum operating conditions for input and output differential voltages in the Point-to-Point LVDS table.
		Pinout Information	Added pin information for the LatticeECP3-70EA and LatticeECP3-95EA devices.
		Ordering Information	Added ordering part numbers for the LatticeECP3-70EA and LatticeECP3-95EA devices.
			Removed dual mark information.