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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8/300L
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	71
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38344hv

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2.4 Addressing Modes

2.4.1 Addressing Modes

The H8/300L CPU supports the eight addressing modes listed in table 2.1. Each instruction uses a subset of these addressing modes.

Table 2.1 Addressing Modes

No.	Address Modes	Symbol
1	Register direct	Rn
2	Register indirect	@Rn
3	Register indirect with displacement	@(d:16, Rn)
4	Register indirect with post-increment	@Rn+
	Register indirect with pre-decrement	@–Rn
5	Absolute address	@aa:8 or @aa:16
6	Immediate	#xx:8 or #xx:16
7	Program-counter relative	@(d:8, PC)
8	Memory indirect	@@aa:8

1. Register Direct—Rn: The register field of the instruction specifies an 8- or 16-bit general register containing the operand.

   Only the MOV.W, ADD.W, SUB.W, CMP.W, ADDS, SUBS, MULXU (8 bits × 8 bits), and DIVXU (16 bits ÷ 8 bits) instructions have 16-bit operands.

2. Register Indirect—@Rn: The register field of the instruction specifies a 16-bit general register containing the address of the operand in memory.

3. Register Indirect with Displacement—@(d:16, Rn): The instruction has a second word (bytes 3 and 4) containing a displacement which is added to the contents of the specified general register to obtain the operand address in memory.

   This mode is used only in MOV instructions. For the MOV.W instruction, the resulting address must be even.

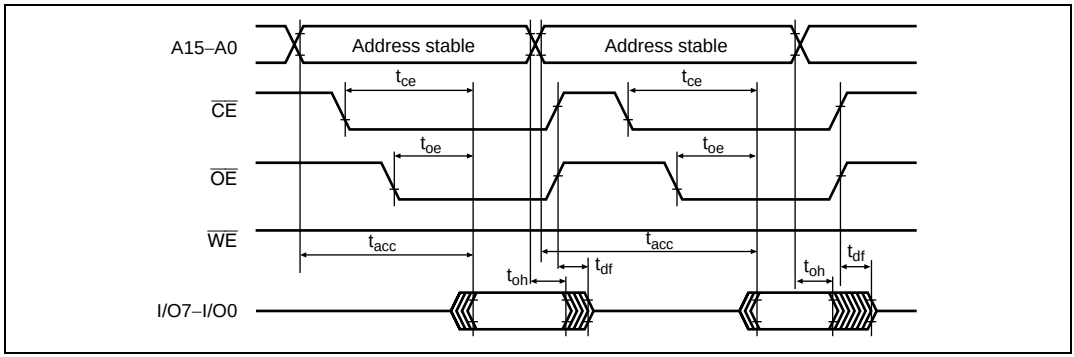


Figure 6.16 $\overline{CE}$ and $\overline{OE}$ Clock System Read Timing Waveforms

6.10.4 Auto-Program Mode

1. When reprogramming previously programmed addresses, perform auto-erasing before auto-programming.
2. Perform auto-programming once only on the same address block. It is not possible to program an address block that has already been programmed.
3. In auto-program mode, 128 bytes are programmed simultaneously. This should be carried out by executing 128 consecutive byte transfers. A 128-byte data transfer is necessary even when programming fewer than 128 bytes. In this case, H'FF data must be written to the extra addresses.
4. The lower 7 bits of the transfer address must be low. If a value other than an effective address is input, processing will switch to a memory write operation but a write error will be flagged.
5. Memory address transfer is performed in the second cycle (figure 6.17). Do not perform transfer after the third cycle.
6. Do not perform a command write during a programming operation.
7. Perform one auto-program operation for a 128-byte block for each address. Two or more additional programming operations cannot be performed on a previously programmed address block.
8. Confirm normal end of auto-programming by checking I/O6. Alternatively, status read mode can also be used for this purpose (I/O7 status polling uses the auto-program operation end decision pin).
9. Status polling I/O6 and I/O7 pin information is retained until the next command write. As long as the next command write has not been performed, reading is possible by enabling $\overline{CE}$ and $\overline{OE}$.
10. Table 6.18 shows the AC characteristics.

Section 7 RAM

7.1 Overview

The H8/3842R, H8/3843R, H8/38342, H8/38343, H8/38442, and H8/38443 have 1 Kbytes of high-speed static RAM, and H8/3844R, H8/3844S, H8/38344, H8/38444, H8/3845R, H8/3845S, H8/38345, H8/38445, H8/3846R, H8/3846S, H8/38346, H8/38446, H8/3847R, H8/3847S, H8/38347, and H8/38447 have 2 Kbytes of high-speed static RAM on-chip. The RAM is connected to the CPU by a 16-bit data bus, allowing high-speed 2-state access for both byte data and word data.

7.1.1 Block Diagram

Figure 7.1 shows a block diagram of the on-chip RAM.

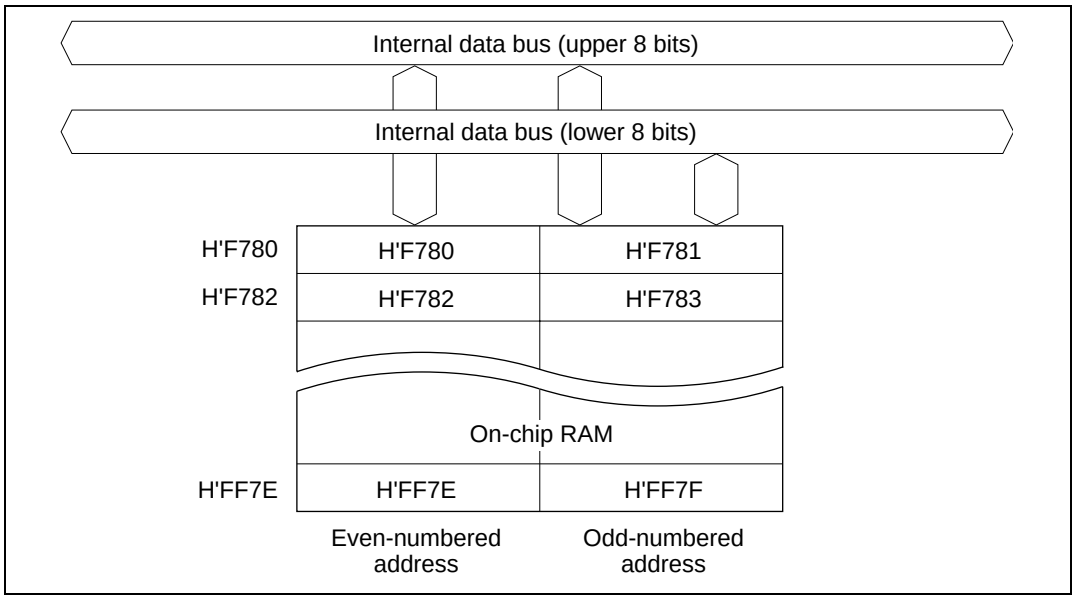


Figure 7.1 RAM Block Diagram (H8/3844R, H8/3844S, H8/38344 and H8/38444)

8.5.3 Pin Functions

Table 8.12 shows the port 4 pin functions.

Table 8.12 Port 4 Pin Functions

Pin	Pin Functions and Selection Method
$P4_3/\overline{IRQ_0}$	The pin function depends on bit IRQ0 in PMR3.

IRQ0	0	1
Pin function	$P4_3$ input pin	$\overline{IRQ_0}$ input pin

$P4_2/TXD_{32}$ — The pin function depends on bit TE in SCR3-2, bit SPC32 in SPCR, and bit $PCR4_2$ in PCR4.

SPC32	0		1
TE	0		1
$PCR4_2$	0	1	*
Pin function	$P4_2$ input pin	$P4_2$ output pin	TXD_{32} output pin

$P4_1/RXD_{32}$ — The pin function depends on bit RE in SCR3-2 and bit $PCR4_1$ in PCR4.

RE	0		1
$PCR4_1$	0	1	*
Pin function	$P4_1$ input pin	$P4_1$ output pin	RXD_{32} input pin

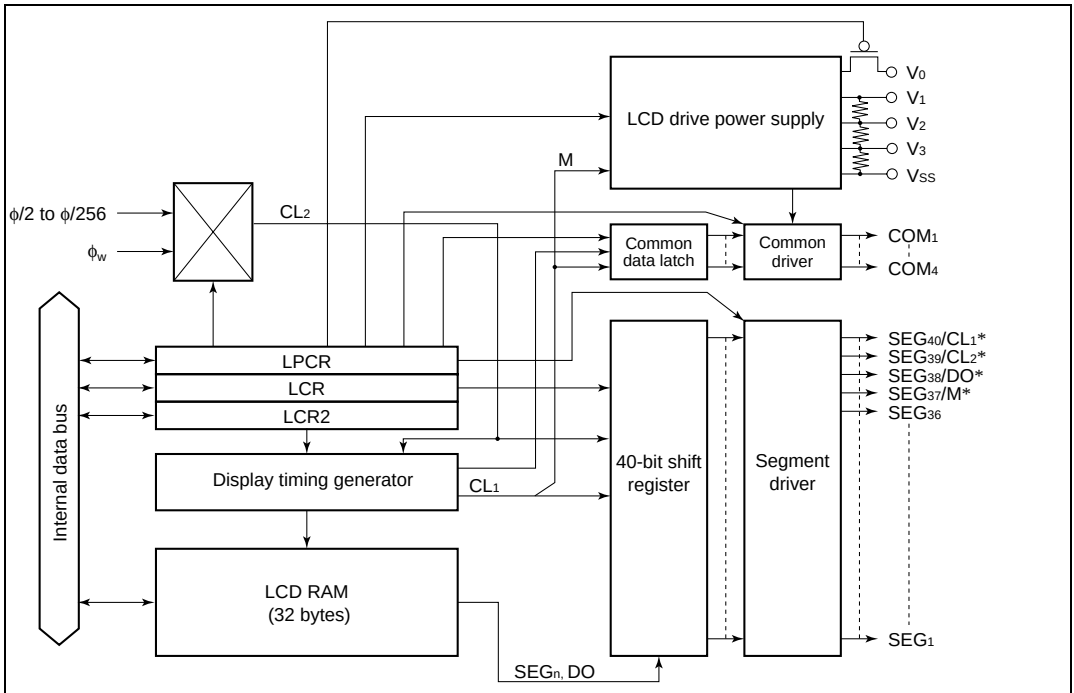
$P4_0/SCK_{32}$ — The pin function depends on bits CKE1 and CKE0 in SCR3-2, bit COM32 in SMR32, and bit $PCR4_0$ in PCR4.

CKE1	0			1
CKE0	0		1	*
COM32	0		1	*	*
$PCR4_0$	0	1	*		*
Pin function	$P4_0$ input pin	$P4_0$ output pin	SCK_{32} output pin		SCK_{32} input pin

*: Don't care

13.1.2 Block Diagram

Figure 13.1 shows a block diagram of the LCD controller/driver.



Legend:
LPCR: LCD port control register
LCR: LCD control register
LCR2: LCD control register 2

Note: * The external expansion function for LCD segments is not implemented in the H8/38347 Group and H8/38447 Group.

Figure 13.1 Block Diagram of LCD Controller/Driver

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Active mode current consumption	I_{OPE2}	V_{CC}	—	0.4	—	mA	Active (medium-speed) mode V_{CC} = 2.7 V, f_{OSC} = 2 MHz, $_{OSC}$/128	*1 *3 *4 Approx. max. value = 1.1 Typ.
			—	0.7	—			*2 *3 *4 Approx. max. value = 1.1 Typ.
			—	0.5	—		Active (medium-speed) mode V_{CC} = 5 V, f_{OSC} = 2 MHz, $_{OSC}$/128	*1 *3 *4 Approx. max. value = 1.1 Typ.
			—	1.0	—			*2 *3 *4 Approx. max. value = 1.1 Typ.
			—	0.8	—		Active (medium-speed) mode V_{CC} = 5 V, f_{OSC} = 4 MHz, $_{OSC}$/128	*1 *3 *4 Approx. max. value = 1.1 Typ.
			—	1.2	—			*2 *3 *4 Approx. max. value = 1.1 Typ.
			—	1.2	3.0		Active (medium-speed) mode V_{CC} = 5 V, f_{OSC} = 10 MHz, $_{OSC}$/128	*1 *3 *4
			—	1.7	3.0			*2 *3 *4

IENR2 Interrupt Enable Register 2 H'F4 System control

Bit	7	6	5	4	3	2	1	0
	IENDT	IENAD	—	IENTG	IENTFH	IENTFL	IENTC	IENEC
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Asynchronous event counter interrupt enable

0	Disables asynchronous event counter interrupt requests
1	Enables asynchronous event counter interrupt requests

Timer C interrupt enable

0	Disables timer C interrupt requests
1	Enables timer C interrupt requests

Timer FL interrupt enable

0	Disables timer FL interrupt requests
1	Enables timer FL interrupt requests

Timer FH interrupt enable

0	Disables timer FH interrupt requests
1	Enables timer FH interrupt requests

Timer G interrupt enable

0	Disables timer G interrupt requests
1	Enables timer G interrupt requests

A/D converter interrupt enable

0	Disables A/D converter interrupt requests
1	Enables A/D converter interrupt requests

Direct transition interrupt enable

0	Disables direct transition interrupt requests
1	Enables direct transition interrupt requests

IRR2 Interrupt Request Register 2 H'F7 System control

Bit	7	6	5	4	3	2	1	0
	IRRDT	IRRAD	—	IRRTG	IRRTFH	IRRTFL	IRRTC	IRREC
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/W	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Asynchronous event counter interrupt request flag

0	[Clearing condition] When IRREC = 1, it is cleared by writing 0
1	[Setting condition] When the asynchronous event counter value overflows

Timer C interrupt request flag

0	[Clearing condition] When IRRTC = 1, it is cleared by writing 0
1	[Setting condition] When the timer C counter value overflows (from H'FF to H'00) or underflows (from H'00 to H'FF)

Timer FL interrupt request flag

0	[Clearing condition] When IRRTFL = 1, it is cleared by writing 0
1	[Setting condition] When counter FL and output compare register FL match in 8-bit timer mode

Timer FH interrupt request flag

0	[Clearing condition] When IRRTFH = 1, it is cleared by writing 0
1	[Setting condition] When counter FH and output compare register FH match in 8-bit timer mode, or when 16-bit counters FL and FH and output compare registers FL and FH match in 16-bit timer mode

Timer G interrupt request flag

0	[Clearing condition] When IRRTG = 1, it is cleared by writing 0
1	[Setting condition] When the TMIG pin is designated for TMIG input and the designated signal edge is input

A/D converter interrupt request flag

0	[Clearing condition] When IRRAD = 1, it is cleared by writing 0
1	[Setting condition] When the A/D converter completes conversion and ADSF is reset

Direct transition interrupt request flag

0	[Clearing condition] When IRRDT = 1, it is cleared by writing 0
1	[Setting condition] When a SLEEP instruction is executed while DTON is set to 1, and a direct transition is made

Note: * Bits 7, 6 and 4 to 0 can only be written with 0, for flag clearing.

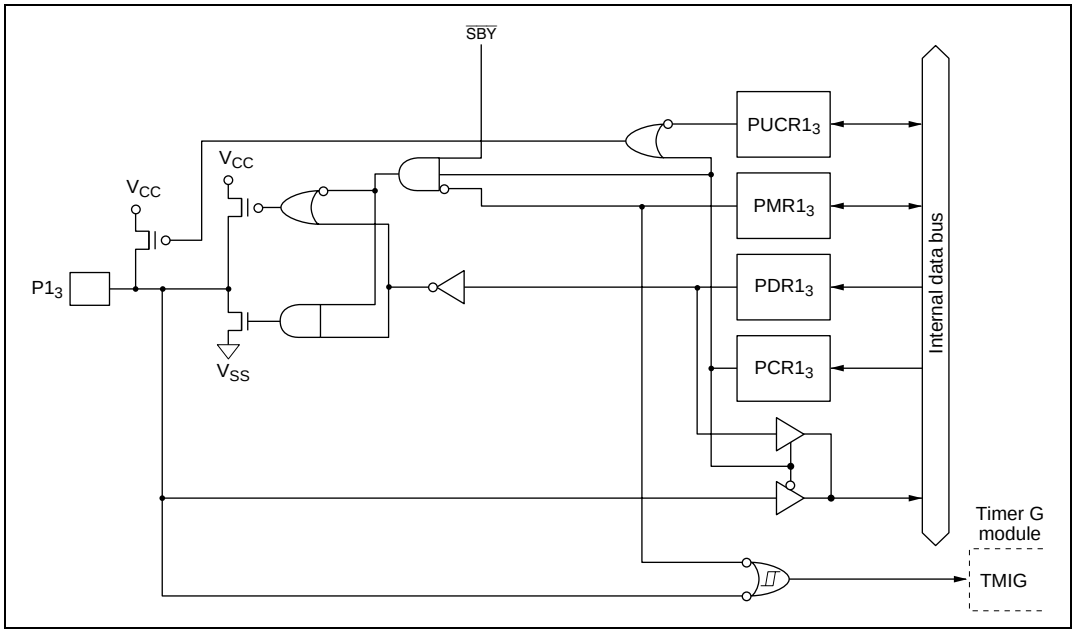
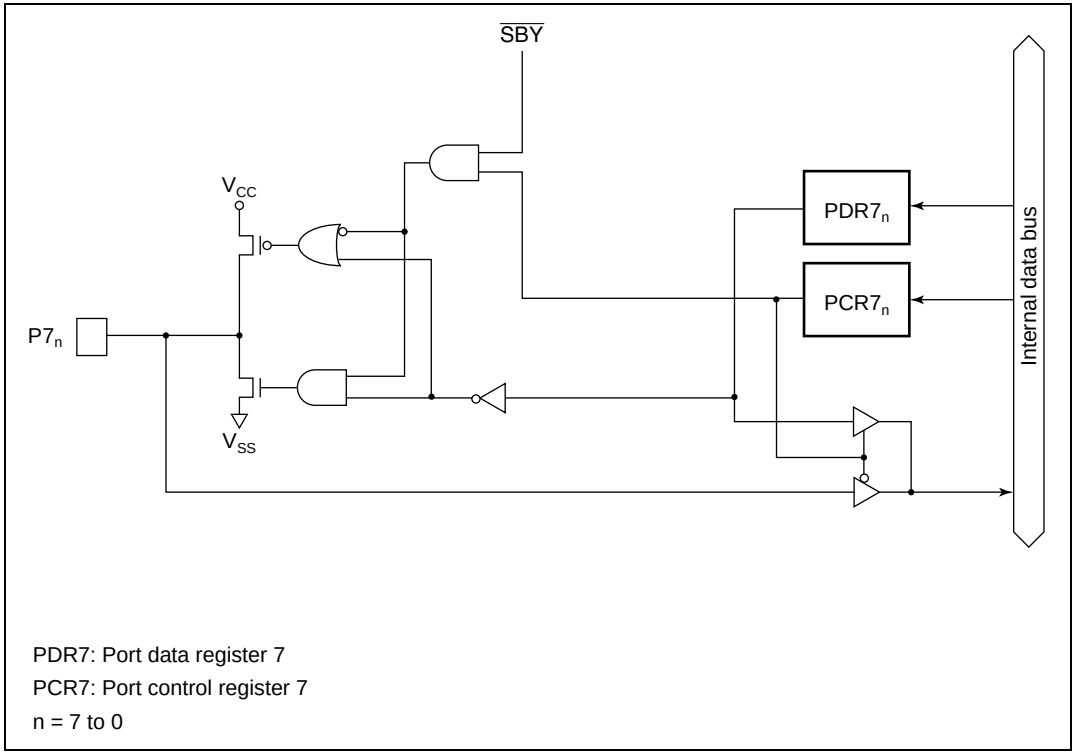


Figure C.1 (b) Port 1 Block Diagram (Pin $P1_3$)

C.7 Block Diagram of Port 7



PDR7: Port data register 7
PCR7: Port control register 7
n = 7 to 0

Figure C.7 Port 7 Block Diagram