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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | H8/300L |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | SCI |
| Peripherals | LCD, PWM, WDT |
| Number of I/O | 71 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 12x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-BFQFP |
| Supplier Device Package | 100-QFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/df38344hwv |

# Section 1 Overview

## 1.1 Overview

The H8/300L Series is a series of single-chip microcomputers (MCU: microcomputer unit), built around the high-speed H8/300L CPU and equipped with peripheral system functions on-chip.

Within the H8/300L Series, the H8/3847R Group, H8/3847S Group, H8/38347 Group, and H8/38447 Group comprise single-chip microcomputers equipped with an LCD (liquid crystal display) controller/driver. Other on-chip peripheral functions include six types of timers, a 14-bit pulse width modulator (PWM), three serial communication interface channels, and an A/D converter. Together, these functions make the H8/3847R Group, H8/3847S Group, H8/38347 Group, and H8/38447 Group ideally suited for embedded applications in systems requiring low power consumption and LCD display. Also available are models incorporating 16 Kbytes to 60 Kbytes of ROM and 1 Kbyte to 2 Kbytes of RAM on-chip.

The H8/3847R is also available in a ZTAT™*1 version with on-chip PROM which can be programmed as required by the user.

The H8/38347 and H8/38447 are available in a F-ZTAT™*2 version with on-chip flash memory that can be programmed on-board.

Table 1.1 summarizes the features of the H8/3847R Group, H8/3847S Group, H8/38347 Group, and H8/38447 Group.

Notes: 1. ZTAT (Zero Turn Around Time) is a trademark of Renesas Technology Corp.
2. F-ZTAT is a trademark of Renesas Technology Corp.

### 5.2.2 Clearing Sleep Mode

Sleep mode is cleared by any interrupt (timer A, timer C, timer F, timer G, asynchronous counter, $IRQ_4$ to $IRQ_0$, $WKP_7$ to $WKP_0$, SCI1, SCI3-1, SCI3-2, or A/D converter), or by input at the $\overline{RES}$ pin.

- Clearing by interrupt

  When an interrupt is requested, sleep mode is cleared and interrupt exception handling starts. A transition is made from sleep (high-speed) mode to active (high-speed) mode, or from sleep (medium-speed) mode to active (medium-speed) mode. Sleep mode is not cleared if the I bit of the condition code register (CCR) is set to 1 or the particular interrupt is disabled in the interrupt enable register.

  To synchronize the interrupt request signal with the system clock, up to 2/ϕ (s) delay may occur after the interrupt request signal occurrence, before the interrupt exception handling start.

- Clearing by $\overline{RES}$ input

  When the $\overline{RES}$ pin goes low, the CPU goes into the reset state and sleep mode is cleared.

### 5.2.3 Clock Frequency in Sleep (Medium-Speed) Mode

Operation in sleep (medium-speed) mode is clocked at the frequency designated by the MA1 and MA0 bits in SYSCR1.

## 5.6 Subactive Mode

### 5.6.1 Transition to Subactive Mode

Subactive mode is entered from watch mode if a timer A, timer F, timer G, $IRQ_0$, or $WKP_7$ to WKP0 interrupt is requested while the LSON bit in SYSCR1 is set to 1. From subsleep mode, subactive mode is entered if a timer A, timer C, timer F, timer G, asynchronous counter, SCI1, SCI3-1, SCI3-2, $IRQ_4$ to $IRQ_0$, or $WKP_7$ to $WKP_0$ interrupt is requested. A transition to subactive mode does not take place if the I bit of CCR is set to 1 or the particular interrupt is disabled in the interrupt enable register.

### 5.6.2 Clearing Subactive Mode

Subactive mode is cleared by a SLEEP instruction or by a low input at the $\overline{\text{RES}}$ pin.

- Clearing by SLEEP instruction
  If a SLEEP instruction is executed while the SSBY bit in SYSCR1 is set to 1 and TMA3 bit in TMA is set to 1, subactive mode is cleared and watch mode is entered. If a SLEEP instruction is executed while SSBY = 0 and LSON = 1 in SYSCR1 and TMA3 = 1 in TMA, subsleep mode is entered. Direct transfer to active mode is also possible; see section 5.8, Direct Transfer, below.

- Clearing by $\overline{\text{RES}}$ pin
  Clearing by $\overline{\text{RES}}$ pin is the same as for standby mode; see 2. Clearing by $\overline{\text{RES}}$ pin in section 5.3.2.

### 5.6.3 Operating Frequency in Subactive Mode

The operating frequency in subactive mode is set in bits SA1 and SA0 in SYSCR2. The choices are $\phi_W/2$, $\phi_W/4$, and $\phi_W/8$.

## 6.2 PROM Mode (H8/3847R)

### 6.2.1 Setting to PROM Mode

If the on-chip ROM is PROM, setting the chip to PROM mode stops operation as a microcontroller and allows the PROM to be programmed in the same way as the standard HN27C101 EPROM. However, page programming is not supported. Table 6.1 shows how to set the chip to PROM mode.

**Table 6.1 Setting to PROM Mode**

| Pin Name | Setting |
|---|---|
| TEST | High level |
| $PB_4/AN_4$ | Low level |
| $PB_5/AN_5$ | |
| $PB_6/AN_6$ | High level |

### 6.2.2 Socket Adapter Pin Arrangement and Memory Map

A standard PROM programmer can be used to program the PROM. A socket adapter is required for conversion to 32 pins, as listed in table 6.2.

Figure 6.2 shows the pin-to-pin wiring of the socket adapter. Figure 6.3 shows a memory map.

**Table 6.2 Socket Adapter**

| Package | Socket Adapter Model (Manufacturer) |
|---|---|
| 100-pin (FP-100B) | ME3887ESHS1H (MINATO)<br>H7388BQ100D3201 (DATA-I/O) |
| 100-pin (FP-100A) | ME3887ESFS1H (MINATO)<br>H7388AQ100D3201 (DATA-I/O) |
| 100-pin (TFP-100B) | ME3887ESNS1H (MINATO)<br>H7388BT100D3201 (DATA-I/O) |
| 100-pin (TFP-100G) | ME3887ESMS1H (MINATO)<br>H7388GT100D3201 (DATA-I/O) |

**Table 6.5 AC Characteristics**

(Conditions: $V_{CC}$ = 6.0 V ±0.25 V, $V_{PP}$ = 12.5 V ±0.3 V, $T_a$ = 25°C ±5°C)

| Item | Symbol | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| Address setup time | $t_{AS}$ | 2 | — | — | µs | Figure 6.5*1 |
| $\overline{OE}$ setup time | $t_{OES}$ | 2 | — | — | µs | |
| Data setup time | $t_{DS}$ | 2 | — | — | µs | |
| Address hold time | $t_{AH}$ | 0 | — | — | µs | |
| Data hold time | $t_{DH}$ | 2 | — | — | µs | |
| Data output disable time | $t_{DF}$*2 | — | — | 130 | µs | |
| $V_{PP}$ setup time | $t_{VPS}$ | 2 | — | — | µs | |
| Programming pulse width | $t_{PW}$ | 0.19 | 0.20 | 0.21 | ms | |
| $\overline{PGM}$ pulse width for overwrite programming | $t_{OPW}$*3 | 0.19 | — | 5.25 | ms | |
| $\overline{CE}$ setup time | $t_{CES}$ | 2 | — | — | µs | |
| $V_{CC}$ setup time | $t_{VCS}$ | 2 | — | — | µs | |
| Data output delay time | $t_{OE}$ | 0 | — | 200 | ns | |

Notes: 1. Input pulse level: 0.45 V to 2.2 V
Input rise time/fall time ≤ 20 ns
Timing reference levels Input: 0.8 V, 2.0 V
Output: 0.8 V, 2.0 V

2. $t_{DF}$ is defined at the point at which the output is floating and the output level cannot be read.
3. $t_{OPW}$ is defined by the value given in figure 6.4, High-Speed, High-Reliability Programming Flow Chart.

**Bit 2—Program-Verify (PV)**

This bit is to set changing to or cancelling program-verify mode (do not set SWE, ESU, PSU, EV, E, and P bits at the same time).

| Bit 2 PV | Description | |
|---|---|---|
| 0 | Program-verify mode is cancelled | (initial value) |
| 1 | The flash memory changes to program-verify mode | |

**Bit 1—Erase (E)**

This bit is to set changing to or cancelling erase mode (do not set SWE, ESU, PSU, EV, PV, and P bits at the same time).

| Bit 1 E | Description | |
|---|---|---|
| 0 | Erase mode is cancelled | (initial value) |
| 1 | When this bit is set to 1, while the SWE = 1 and ESU = 1, the flash memory changes to erase mode. | |

**Bit 0—Program (P)**

This bit is to set changing to or cancelling program mode (do not set SWE, ESU, PSU, EV, PV, and E bits at the same time).

| Bit 0 P | Description | |
|---|---|---|
| 0 | Program mode is cancelled | (initial value) |
| 1 | When this bit is set to 1, while the SWE = 1 and PSU = 1, the flash memory changes to program mode. | |

**Table 6.14 Command Sequence in Programmer Mode**

| Command Name | Number of Cycles | 1st Cycle | | | 2nd Cycle | | |
|---|---|---|---|---|---|---|---|
| | | Mode | Address | Data | Mode | Address | Data |
| Memory read | 1 + n | Write | X | H'00 | Read | RA | Dout |
| Auto-program | 129 | Write | X | H'40 | Write | WA | Din |
| Auto-erase | 2 | Write | X | H'20 | Write | X | H'20 |
| Status read | 2 | Write | X | H'71 | Write | X | H'71 |

n: the number of address write cycles

### 1. Port Data Register 1 (PDR1)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | $P1_7$ | $P1_6$ | $P1_5$ | $P1_4$ | $P1_3$ | $P1_2$ | $P1_1$ | $P1_0$ |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

PDR1 is an 8-bit register that stores data for port 1 pins $P1_7$ to $P1_0$. If port 1 is read while PCR1 bits are set to 1, the values stored in PDR1 are read, regardless of the actual pin states. If port 1 is read while PCR1 bits are cleared to 0, the pin states are read.

Upon reset, PDR1 is initialized to H'00.

### 2. Port Control Register 1 (PCR1)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | $PCR1_7$ | $PCR1_6$ | $PCR1_5$ | $PCR1_4$ | $PCR1_3$ | $PCR1_2$ | $PCR1_1$ | $PCR1_0$ |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | W | W | W | W | W | W | W | W |

PCR1 is an 8-bit register for controlling whether each of the port 1 pins $P1_7$ to $P1_0$ functions as an input pin or output pin. Setting a PCR1 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCR1 and in PDR1 are valid only when the corresponding pin is designated in PMR1 as a general I/O pin.

Upon reset, PCR1 is initialized to H'00.

PCR1 is a write-only register, which is always read as all 1s.

### 3. Port Pull-up Control Register 1 (PUCR1)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | $PUCR1_7$ | $PUCR1_6$ | $PUCR1_5$ | $PUCR1_4$ | $PUCR1_3$ | $PUCR1_2$ | $PUCR1_1$ | $PUCR1_0$ |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

PUCR1 controls whether the MOS pull-up of each of the port 1 pins $P1_7$ to $P1_0$ is on or off. When a PCR1 bit is cleared to 0, setting the corresponding PUCR1 bit to 1 turns on the MOS pull-up for the corresponding pin, while clearing the bit to 0 turns off the MOS pull-up.

Upon reset, PUCR1 is initialized to H'00.

| Pin | Pin Functions and Selection Method |
|---|---|
| $P1_3$/TMIG | The pin function depends on bit TMIG in PMR1 and bit $PCR1_3$ in PCR1. |

| TMIG | 0 | | 1 |
|---|---|---|---|
| $PCR1_3$ | 0 | 1 | * |
| Pin function | $P1_3$ input pin | $P1_3$ output pin | TMIG input pin |

$P1_2$/TMOFH — The pin function depends on bit TMOFH in PMR1 and bit $PCR1_2$ in PCR1.

| TMOFH | 0 | | 1 |
|---|---|---|---|
| $PCR1_2$ | 0 | 1 | * |
| Pin function | $P1_2$ input pin | $P1_2$ output pin | TMOFH output pin |

$P1_1$/TMOFL — The pin function depends on bit TMOFL in PMR1 and bit $PCR1_1$ in PCR1.

| TMOFL | 0 | | 1 |
|---|---|---|---|
| $PCR1_1$ | 0 | 1 | * |
| Pin function | $P1_1$ input pin | $P1_1$ output pin | TMOFL output pin |

$P1_0$/TMOW — The pin function depends on bit TMOW in PMR1 and bit $PCR1_0$ in PCR1.

| TMOW | 0 | | 1 |
|---|---|---|---|
| $PCR1_0$ | 0 | 1 | * |
| Pin function | $P1_0$ input pin | $P1_0$ output pin | TMOW output pin |

*: Don't care

### 8.2.4 Pin States

Table 8.4 shows the port 1 pin states in each operating mode.

**Table 8.4 Port 1 Pin States**

| Pins | Reset | Sleep | Subsleep | Standby | Watch | Subactive | Active |
|---|---|---|---|---|---|---|---|
| $P1_7$/$\overline{IRQ_3}$/TMIF<br>$P1_6$/$\overline{IRQ_2}$<br>$P1_5$/$\overline{IRQ_1}$/TMIC<br>$P1_4$/$IRQ_4$/$\overline{ADTRG}$<br>$P1_3$/TMIG<br>$P1_2$/TMOFH<br>$P1_1$/TMOFL<br>$P1_0$/TMOW | High-impedance | Retains previous state | Retains previous state | High-impedance* | Retains previous state | Functional | Functional |

Note: * A high-level signal is output when the MOS pull-up is in the on state.

**Bit 3:** Timer G module standby mode control (TGCKSTP)

Bit 3 controls setting and clearing of module standby mode for timer G.

| TGCKSTP | Description | |
|---|---|---|
| 0 | Timer G is set to module standby mode | |
| 1 | Timer G module standby mode is cleared | (initial value) |

### 9.5.3 Noise Canceler

The noise canceler consists of a digital low-pass filter that eliminates high-frequency component noise from the pulses input from the input capture input pin. The noise canceler is set by NCS* in PMR3.

Figure 9.9 shows a block diagram of the noise canceler.

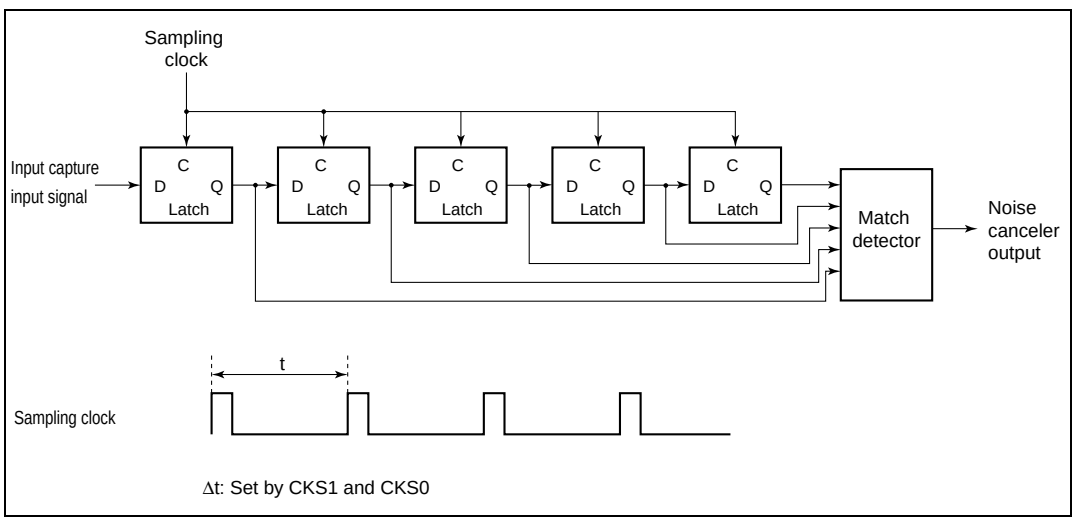


**Figure 9.9 Noise Canceler Block Diagram**

The noise canceler consists of five latch circuits connected in series and a match detector circuit. When the noise cancellation function is not used (NCS = 0), the system clock is selected as the sampling clock. When the noise cancellation function is used (NCS = 1), the sampling clock is the internal clock selected by CKS1 and CKS0 in TMG, the input capture input is sampled on the rising edge of this clock, and the data is judged to be correct when all the latch outputs match. If all the outputs do not match, the previous value is retained. After a reset, the noise canceler output is initialized when the falling edge of the input capture input signal has been sampled five times.

# Section 10 Serial Communication Interface

## 10.1 Overview

This LSI is provided with three serial communication interface (SCI) channels. The functions of the three SCI channels are summarized in table 10.1.

**Table 10.1 Overview of SCI Functions**

| SCI Name | Functions | Features |
|---|---|---|
| SCI1 | Synchronous serial transfer functions<br>•Choice of transfer data length (8 or 16 bits)<br>•Continuous clock output function | •Choice of 8 internal clocks ($\phi$/1024 to $\phi$/4, $\phi_W$/4) or external clock<br>•Open-drain output option<br>•Interrupt generated on completion of transfer |
| SCI31, SCI32 | Synchronous serial transfer functions<br>•8-bit transfer data length<br>•Transmission/reception/simultaneous transmission and reception<br>Asynchronous serial transfer functions<br>•Multiprocessor communication function<br>•Choice of transfer data length (5 or 7 or 8 bits)<br>•Choice of stop bit length (1 or 2 bits)<br>•Parity addition function | •On-chip baud rate generator<br>•Receive error detection<br>•Break detection<br>•Interrupt generated on completion of transfer or in case of error |

**Bit 7:** A/D start flag (ADSF)

Bit 7 controls and indicates the start and end of A/D conversion.

| Bit 7 ADSF | Description | |
|---|---|---|
| 0 | Read: Indicates the completion of A/D conversion | (initial value) |
| | Write: Stops A/D conversion | |
| 1 | Read: Indicates A/D conversion in progress | |
| | Write: Starts A/D conversion | |

**Bits 6 to 0:** Reserved bits

Bits 6 to 0 are reserved; they are always read as 1, and cannot be modified.

### 12.2.4 Clock Stop Register 1 (CKSTPR1)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | S1CKSTP | S31CKSTP | S32CKSTP | ADCKSTP | TGCKSTP | TFCKSTP | TCCKSTP | TACKSTP |
| Initial value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

CKSTPR1 is an 8-bit read/write register that performs module standby mode control for peripheral modules. Only the bit relating to the A/D converter is described here. For details of the other bits, see the sections on the relevant modules.

**Bit 4:** A/D converter module standby mode control (ADCKSTP)

Bit 4 controls setting and clearing of module standby mode for the A/D converter.

| ADCKSTP | Description | |
|---|---|---|
| 0 | A/D converter is set to module standby mode | |
| 1 | A/D converter module standby mode is cleared | (initial value) |

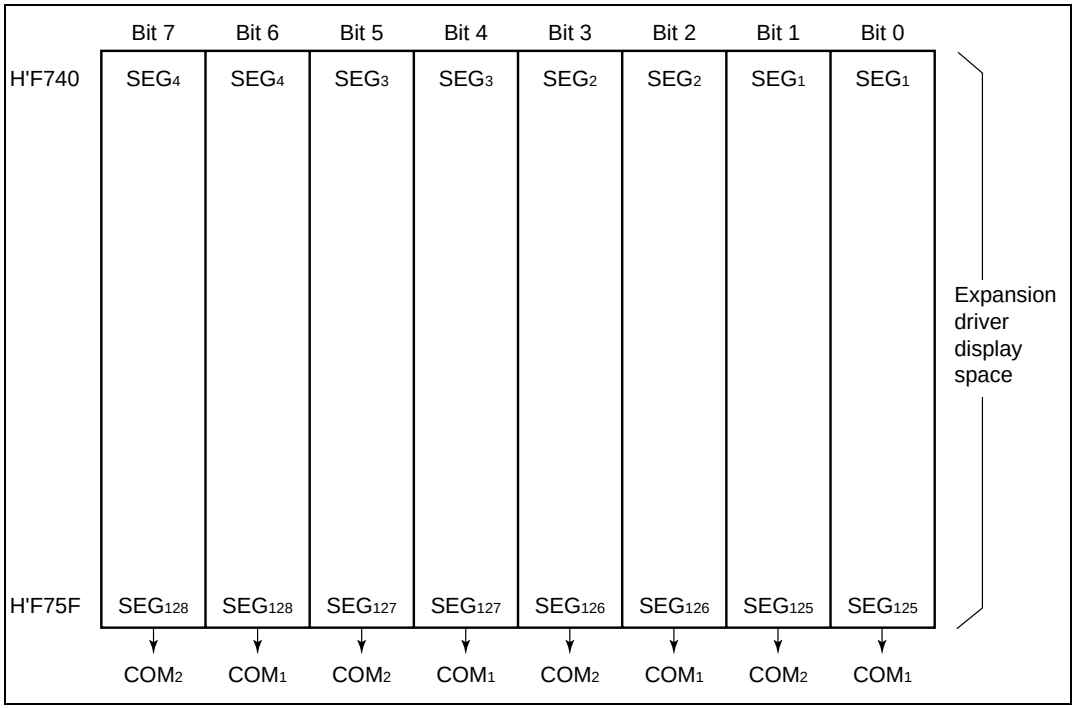


**Figure 13.11 LCD RAM Map with Segment Externally Expanded (SGX = "1", SGS3 to SGS0 = "0000" 1/2 duty)**

**Table A.4 Number of Cycles in Each Instruction**

| Instruction | Mnemonic | Instruction Fetch I | Branch Addr. Read J | Stack Operation K | Byte Data Access L | Word Data Access M | Internal Operation N |
|---|---|---|---|---|---|---|---|
| ADD | ADD.B #xx:8, Rd | 1 | | | | | |
| | ADD.B Rs, Rd | 1 | | | | | |
| | ADD.W Rs, Rd | 1 | | | | | |
| ADDS | ADDS.W #1, Rd | 1 | | | | | |
| | ADDS.W #2, Rd | 1 | | | | | |
| ADDX | ADDX.B #xx:8, Rd | 1 | | | | | |
| | ADDX.B Rs, Rd | 1 | | | | | |
| AND | AND.B #xx:8, Rd | 1 | | | | | |
| | AND.B Rs, Rd | 1 | | | | | |
| ANDC | ANDC #xx:8, CCR | 1 | | | | | |
| BAND | BAND #xx:3, Rd | 1 | | | | | |
| | BAND #xx:3, @Rd | 2 | | | 1 | | |
| | BAND #xx:3, @aa:8 | 2 | | | 1 | | |
| Bcc | BRA d:8 (BT d:8) | 2 | | | | | |
| | BRN d:8 (BF d:8) | 2 | | | | | |
| | BHI d:8 | 2 | | | | | |
| | BLS d:8 | 2 | | | | | |
| | BCC d:8 (BHS d:8) | 2 | | | | | |
| | BCS d:8 (BLO d:8) | 2 | | | | | |
| | BNE d:8 | 2 | | | | | |
| | BEQ d:8 | 2 | | | | | |
| | BVC d:8 | 2 | | | | | |
| | BVS d:8 | 2 | | | | | |
| | BPL d:8 | 2 | | | | | |
| | BMI d:8 | 2 | | | | | |
| | BGE d:8 | 2 | | | | | |
| | BLT d:8 | 2 | | | | | |
| | BGT d:8 | 2 | | | | | |
| | BLE d:8 | 2 | | | | | |
| BCLR | BCLR #xx:3, Rd | 1 | | | | | |
| | BCLR #xx:3, @Rd | 2 | | | 2 | | |
| | BCLR #xx:3, @aa: 8 | 2 | | | 2 | | |
| | BCLR Rn, Rd | 1 | | | | | |
| | BCLR Rn, @Rd | 2 | | | 2 | | |
| | BCLR Rn, @aa:8 | 2 | | | 2 | | |

## SCR32—Serial Control Register 32 H'AA SCI32

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | TIE32 | RIE32 | TE32 | RE32 | MPIE32 | TEIE32 | CKE321 | CKE320 |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Clock enable**

| Bit 1 | Bit 0 | Description | | |
|---|---|---|---|---|
| CKE321 | CKE320 | Communication Mode | Clock Source | $SCK_3$ Pin Function |
| 0 | 0 | Asynchronous | Internal clock | I/O port |
| | | Synchronous | Internal clock | Serial clock output |
| 0 | 1 | Asynchronous | Internal clock | Clock output |
| | | Synchronous | Reserved (Do not specify this combination) | |
| 1 | 0 | Asynchronous | External clock | Clock input |
| | | Synchronous | External clock | Serial clock input |
| 1 | 1 | Asynchronous | Reserved (Do not specify this combination) | |
| | | Synchronous | Reserved (Do not specify this combination) | |

**Transmit end interrupt enable**

| | |
|---|---|
| 0 | Transmit end interrupt request (TEI) disabled |
| 1 | Transmit end interrupt request (TEI) enabled |

**Multiprocessor interrupt enable**

| | |
|---|---|
| 0 | Multiprocessor interrupt request disabled (normal receive operation)<br>[Clearing condition]<br>When data is received in which the multiprocessor bit is set to 1 |
| 1 | Multiprocessor interrupt request enabled<br>The receive interrupt request (RXI), receive error interrupt request (ERI), and setting of the RDRF, FER, and OER flags in the serial status register (SSR), are disabled until data with the multiprocessor bit set to 1 is received. |

**Receive enable**

| | |
|---|---|
| 0 | Receive operation disabled (RXD pin is I/O port) |
| 1 | Receive operation enabled (RXD pin is receive data pin) |

**Transmit enable**

| | |
|---|---|
| 0 | Transmit operation disabled (TXD pin is transmit data pin) |
| 1 | Transmit operation enabled (TXD pin is transmit data pin) |

**Receive interrupt enable**

| | |
|---|---|
| 0 | Receive data full interrupt request (RXI) and receive error interrupt request (ERI) disabled |
| 1 | Receive data full interrupt request (RXI) and receive error interrupt request (ERI) enabled |

**Transmit interrupt enable**

| | |
|---|---|
| 0 | Transmit data empty interrupt request (TXI) disabled |
| 1 | Transmit data empty interrupt request (TXI) enabled |

## LPCR—LCD Port Control Register H'C0 LCD controller/driver

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | DTS1 | DTS0 | CMX | SGX | SGS3 | SGS2 | SGS1 | SGS0 |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Segment driver select**

| Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Function of Pins $SEG_{32}$ to $SEG_1$ | | | | | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| SGX | SGS3 | SGS2 | SGS1 | SGS0 | $SEG_{40}$ to $SEG_{33}$ | $SEG_{32}$ to $SEG_{25}$ | $SEG_{24}$ to $SEG_{17}$ | $SEG_{16}$ to $SEG_9$ | $SEG_8$ to $SEG_1$ | |
| 0 | 0 | 0 | 0 | 0 | Port | Port | Port | Port | Port | (Initial value) |
| 0 | 0 | 0 | 0 | 1 | SEG | Port | Port | Port | Port | |
| 0 | 0 | 0 | 1 | * | SEG | SEG | Port | Port | Port | |
| 0 | 0 | 1 | 0 | * | SEG | SEG | SEG | Port | Port | |
| 0 | 0 | 1 | 1 | * | SEG | SEG | SEG | SEG | Port | |
| 0 | 1 | * | * | * | SEG | SEG | SEG | SEG | SEG | |
| 1 | 0 | 0 | 0 | 0 | Port*1 | Port | Port | Port | Port | |
| 1 | 0 | 0 | 0 | 1 | Do not use | | | | | |
| 1 | 0 | 0 | 1 | * | | | | | | |
| 1 | 0 | 1 | * | * | | | | | | |
| 1 | 1 | * | * | * | | | | | | |

Note: 1. $SEG_{40}$ to $SEG_{37}$ are external expansion pins. *: Don't care

**Expansion signal select**

| | |
|---|---|
| 0 | $SEG_{40}$ to $SEG_{37}$ pin* (Initial value) |
| 1 | $CL_1$, $CL_2$, DO and M pin |

Note: * Functions as ports when SGS3 to SGS0 are set at "0000".
In the case of the H8/38347 Group and H8/38447 Group the initial values of these bits must not be changed.

**Duty select, common function select**

| Bit 7 | Bit 6 | Bit 5 | Duty Cycle | Common Drivers | Notes |
|---|---|---|---|---|---|
| DTS1 | DTS0 | CMX | | | |
| 0 | 0 | 0 | Static | $COM_1$ | Do not use $COM_4$, $COM_3$, and $COM_2$ |
| 0 | 0 | 1 | | $COM_4$ to $COM_1$ | $COM_4$ to $COM_2$ output the same waveform as $COM_1$ |
| 0 | 1 | 0 | 1/2 duty | $COM_2$ to $COM_1$ | Do not use $COM_4$ and $COM_3$ |
| 0 | 1 | 1 | | $COM_4$ to $COM_1$ | $COM_4$ outputs the same waveform as $COM_3$ and $COM_2$ outputs the same waveform as $COM_1$ |
| 1 | 0 | 0 | 1/3 duty | $COM_3$ to $COM_1$ | Do not use $COM_4$ |
| 1 | 0 | 1 | | $COM_4$ to $COM_1$ | Do not use $COM_4$ |
| 1 | 1 | 0 | 1/4 duty | $COM_4$ to $COM_1$ | — |
| 1 | 1 | 1 | | | |

## C.4 Block Diagrams of Port 4

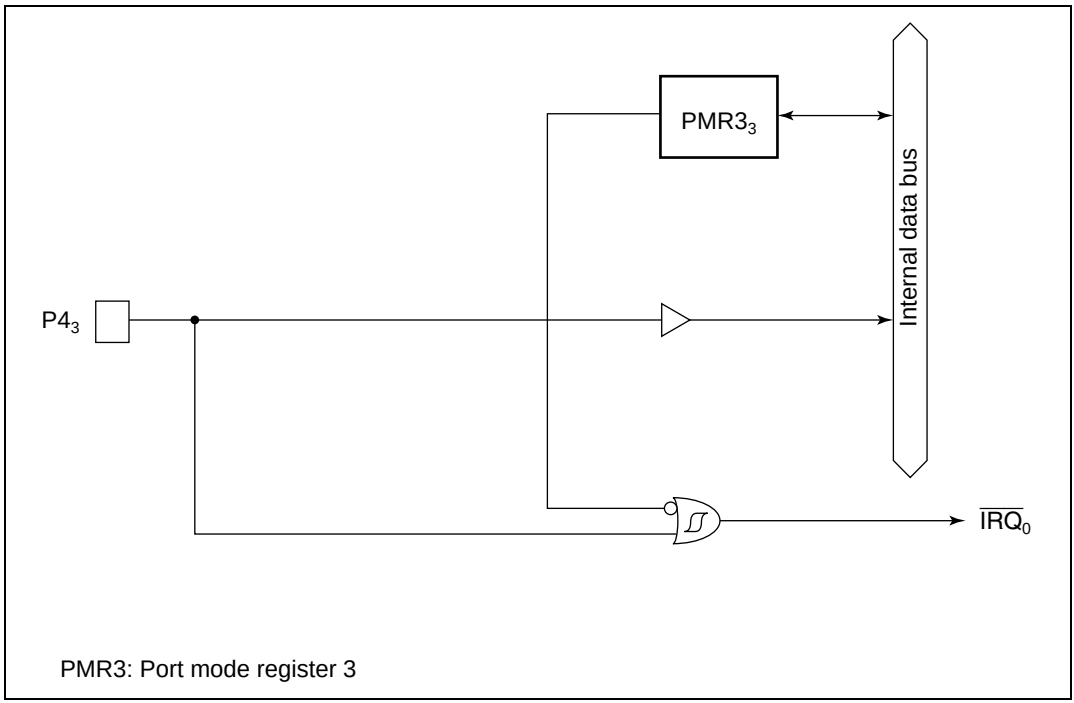


**Figure C.4 (a) Port 4 Block Diagram (Pin P4$_3$)**

## C.12 Block Diagram of Port C

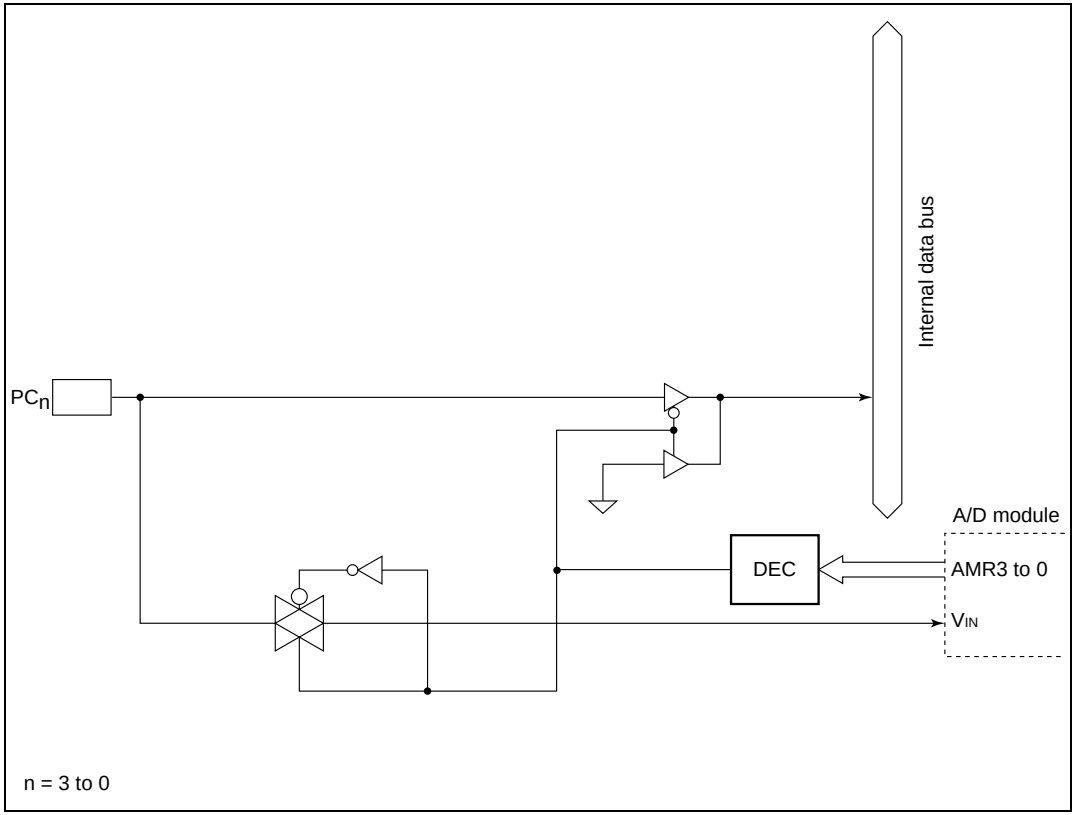


**Figure C.12 Port C Block Diagram**

# Appendix H Form of Bonding Pads

The form of the bonding pads for the HCD6433847R, HCD6433846R, HCD6433845R, HCD6433844R, HCD6433843R, and HCD6433842R is shown in figure H.1.

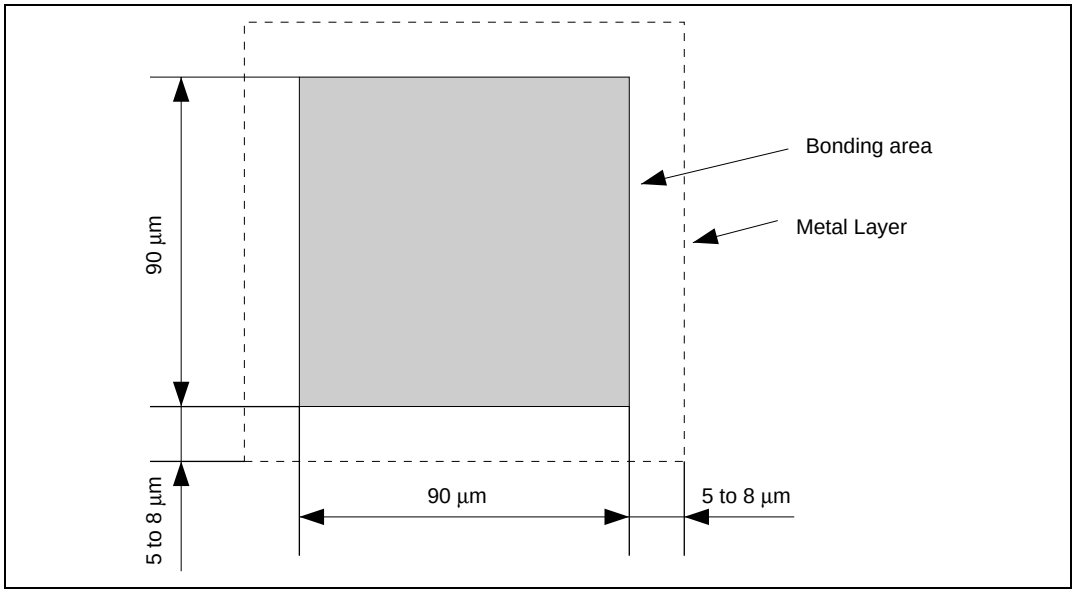


**Figure H.1 Bonding Pad Form**